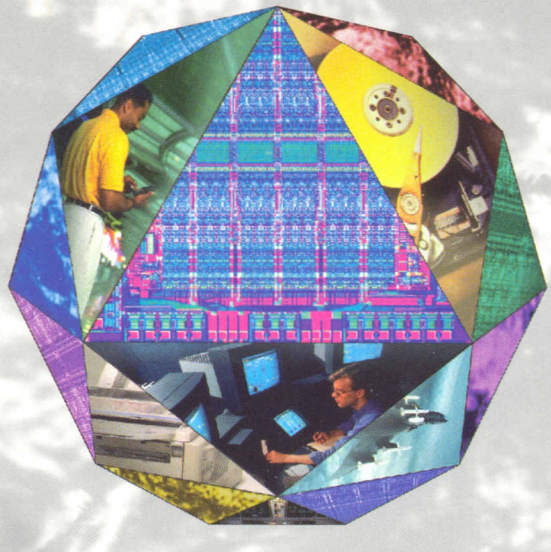


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Atmel's broad line of products provide customers with a variety of solutions to their memory applications. Atmel can offer high-density, high-speed memory and logic *standard* products as well as custom gate arrays.

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CMOS Microcontroller

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CMOS Mixed Signal

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CMOS Microcontroller

Part No.	Memory Size	Description	Page No.
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CMOS Serial E^2PROMs

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CMOS Parallel E^2PROMs

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CMOS EPROMs

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CMOS PROMs

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ATL75	72K	1.0-Micron CMOS Gate Array, 3.3-Volt & 5.0-Volt Operation	8-3
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ATL130	131K	1.0-Micron CMOS Gate Array, 3.3-Volt & 5.0-Volt Operation	8-3
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ATL80/250	242K	0.8-Micron CMOS Gate Array, 3.3-Volt & 5.0-Volt Operation	8-15
ATL80/300	296K	0.8-Micron CMOS Gate Array, 3.3-Volt & 5.0-Volt Operation	8-15
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CMOS Logic

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AT40391B	25-40 MHz	80386DX PC/AT System & Cache Controller	9-3
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AT40493	25-50 MHz	80486 PC/AT System & Cache Controller	9-9
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AT40498	25-50 MHz	80486 Core Logic Controller	9-17
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CMOS Smart Card ICs

Part No.	Memory Size	Description	Page No.
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AT24C16	16K	2-Wire, Serial E^2PROM	10-3
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AT93C56	2K	2-Wire, Serial E^2PROM	10-5
AT93C57	2K	2-Wire, Serial E^2PROM	10-5
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AT88SC06	104 x 1	104-Bit Serial E^2PROM with Security	10-7
AT88SC101	1024 x 1	1K Serial E^2PROM with Security, 1 Memory Zone, 1024 Bits	10-15
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CMOS Mixed Signal

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CMOS Microcontroller

Part No.	Memory Size	Description	Page No.
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CMOS Mixed Signal

Part No.	Frequency	Description	Page No.
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ATT8C12D	98 MHz	Dual Channel 18/18-Bit A/D Converter	11-19

CMOS Microcontroller

Part No.	Memory Size	Description	Page No.
AT89C51	4K x 8	80C31 Microcontroller with 4K Bytes EEPROM	12-3

CMOS Serial E²PROM Product Selection Guide

AT24C01

see page 2-3

Organization: 128 x 8
No. of Pins: DIP 8, SOIC 8

Speed (ms)	Voltage	Package P	Package S	Package W	Temperature Range	I_{SB} (µA)	I_{CC} (µA)	fMAX (kHz)
10	1.8	•	•		C	3.0	800	100
10	1.8	•	•		I	3.0	800	100
10	2.5	•	•		C	4.0	1000	100
10	2.5	•	•		I	4.0	1000	100
10	2.7	•	•		C	4.0	1500	100
10	2.7	•	•		I	4.0	1500	100
10	5.0	•	•	•	C	18.0	3000	100
10	5.0	•	•	•	I	18.0	3000	100

AT24C01A

see page 2-13

Organization: 128 x 8
No. of Pins: DIP 8, SOIC 8

Speed (ms)	Voltage	Package P	Package S	Package W	Temperature Range	I_{SB} (µA)	I_{CC} (µA)	fMAX (kHz)
10	1.8	•	•		C	3.0	800	100
10	1.8	•	•		I	3.0	800	100
10	2.5	•	•		C	4.0	1000	100
10	2.5	•	•		I	4.0	1000	100
10	2.7	•	•		C	4.0	1500	100
10	2.7	•	•		I	4.0	1500	100
10	5.0	•	•	•	C	18.0	3000	100
10	5.0	•	•	•	I	18.0	3000	100

Package Type	
P	8P3, 8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
S	8S1, 8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
W	Die
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
Voltage Range	
1.8	Low Voltage (1.8 V to 6.0 V)
2.5	Low Voltage (2.5 V to 6.0 V)
2.7	Low Voltage (2.7 V to 6.0 V)
5.0	Standard Device (4.5 V to 6.0 V)

AT24C02

see page 2-13

Organization: 256 x 8
No. of Pins: DIP 8, SOIC 14

Speed (ms)	Voltage	Package P	Package S2	Package W	Temperature Range	I_{SB} (µA)	I_{CC} (µA)	fMAX (kHz)
10	1.8	•	•		C	3.0	800	100
10	1.8	•	•		I	3.0	800	100
10	2.5	•	•		C	4.0	1000	100
10	2.5	•	•		I	4.0	1000	100
10	2.7	•	•		C	4.0	1500	100
10	2.7	•	•		I	4.0	1500	100
10	5.0	•	•	•	C	18.0	3000	100
10	5.0	•	•	•	I	18.0	3000	100

AT24C02N

see page 2-13

Organization: 256 x 8
No. of Pins: SOIC 8

Speed (ms)	Voltage	Package S1	Temperature Range	I_{SB} (µA)	I_{CC} (µA)	fMAX (kHz)
10	1.8	•	C	3.0	800	100
10	1.8	•	I	3.0	800	100
10	2.5	•	C	4.0	1000	100
10	2.5	•	I	4.0	1000	100
10	2.7	•	C	4.0	1500	100
10	2.7	•	I	4.0	1500	100
10	5.0	•	C	18.0	3000	100
10	5.0	•	I	18.0	3000	100

Package Type	
P	8P3, 8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
S1	8S1, 8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
S2	14S, 14 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (SOIC)
W	Die
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
Voltage Range	
1.8	Low Voltage (1.8 V to 6.0 V)
2.5	Low Voltage (2.5 V to 6.0 V)
2.7	Low Voltage (2.7 V to 6.0 V)
5.0	Standard Device (4.5 V to 6.0 V)

CMOS Serial E²PROM Product Selection Guide

AT24C04

see page 2-13

Organization: 512 x 8
No. of Pins: DIP 8, SOIC 14

Speed (ms)	Voltage	Package P	Package S2	Package W	Temperature Range	I_{SB} (µA)	I_{CC} (µA)	fMAX (kHz)
10	1.8	•	•		C	3.0	800	100
10	1.8	•	•		I	3.0	800	100
10	2.5	•	•		C	4.0	1000	100
10	2.5	•	•		I	4.0	1000	100
10	2.7	•	•		C	4.0	1500	100
10	2.7	•	•		I	4.0	1500	100
10	5.0	•	•	•	C	18.0	3000	100
10	5.0	•	•	•	I	18.0	3000	100

AT24C04N

see page 2-13

Organization: 512 x 8
No. of Pins: SOIC 8

Speed (ms)	Voltage	Package S1	Temperature Range	I_{SB} (µA)	I_{CC} (µA)	fMAX (kHz)
10	1.8	•	C	3.0	800	100
10	1.8	•	I	3.0	800	100
10	2.5	•	C	4.0	1000	100
10	2.5	•	I	4.0	1000	100
10	2.7	•	C	4.0	1500	100
10	2.7	•	I	4.0	1500	100
10	5.0	•	C	18.0	3000	100
10	5.0	•	I	18.0	3000	100

Package Type	
P	8P3, 8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
S1	8S1, 8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
S2	14S, 14 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (SOIC)
W	Die
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
Voltage Range	
1.8	Low Voltage (1.8 V to 6.0 V)
2.5	Low Voltage (2.5 V to 6.0 V)
2.7	Low Voltage (2.7 V to 6.0 V)
5.0	Standard Device (4.5 V to 6.0 V)

CMOS Serial E²PROM Product Selection Guide

AT24C08

see page 2-13

Organization: 1024 x 8
No. of Pins: DIP 8, SOIC 14

Speed (ms)	Voltage	Package P	Package S2	Package W	Temperature Range	I_{SB} (µA)	I_{CC} (µA)	fMAX (kHz)
10	1.8	•	•		C	3.0	800	100
10	1.8	•	•		I	3.0	800	100
10	2.5	•	•		C	4.0	1000	100
10	2.5	•	•		I	4.0	1000	100
10	2.7	•	•		C	4.0	1500	100
10	2.7	•	•		I	4.0	1500	100
10	5.0	•	•	•	C	18.0	3000	100
10	5.0	•	•	•	I	18.0	3000	100

AT24C08N

see page 2-13

Organization: 1024 x 8
No. of Pins: SOIC 8

Speed (ms)	Voltage	Package S1	Temperature Range	I_{SB} (µA)	I_{CC} (µA)	fMAX (kHz)
10	1.8	•	C	3.0	800	100
10	1.8	•	I	3.0	800	100
10	2.5	•	C	4.0	1000	100
10	2.5	•	I	4.0	1000	100
10	2.7	•	C	4.0	1500	100
10	2.7	•	I	4.0	1500	100
10	5.0	•	C	18.0	3000	100
10	5.0	•	I	18.0	3000	100

Package Type	
P	8P3, 8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
S1	8S1, 8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
S2	14S, 14 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (SOIC)
W	Die
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
Voltage Range	
1.8	Low Voltage (1.8 V to 6.0 V)
2.5	Low Voltage (2.5 V to 6.0 V)
2.7	Low Voltage (2.7 V to 6.0 V)
5.0	Standard Device (4.5 V to 6.0 V)

CMOS Serial E²PROM Product Selection Guide

AT24C16

see page 2-13

Organization: 2048 x 8
No. of Pins: DIP 8, SOIC 14

Speed (ms)	Voltage	Package P	Package S2	Package W	Temperature Range	I_{SB} (µA)	I_{CC} (µA)	fMAX (kHz)
10	1.8	•	•		C	3.0	800	100
10	1.8	•	•		I	3.0	800	100
10	2.5	•	•		C	4.0	1000	100
10	2.5	•	•		I	4.0	1000	100
10	2.7	•	•		C	4.0	1500	100
10	2.7	•	•		I	4.0	1500	100
10	5.0	•	•	•	C	18.0	3000	100
10	5.0	•	•	•	I	18.0	3000	100

AT24C16N

see page 2-13

Organization: 2048 x 8
No. of Pins: SOIC 8

Speed (ms)	Voltage	Package S1	Temperature Range	I_{SB} (µA)	I_{CC} (µA)	fMAX (kHz)
10	1.8	•	C	3.0	800	100
10	1.8	•	I	3.0	800	100
10	2.5	•	C	4.0	1000	100
10	2.5	•	I	4.0	1000	100
10	2.7	•	C	4.0	1500	100
10	2.7	•	I	4.0	1500	100
10	5.0	•	C	18.0	3000	100
10	5.0	•	I	18.0	3000	100

Package Type	
P	8P3, 8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
S1	8S1, 8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
S2	14S, 14 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (SOIC)
W	Die
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
Voltage Range	
1.8	Low Voltage (1.8 V to 6.0 V)
2.5	Low Voltage (2.5 V to 6.0 V)
2.7	Low Voltage (2.7 V to 6.0 V)
5.0	Standard Device (4.5 V to 6.0 V)

CMOS Serial E²PROM Product Selection Guide

AT24C164

see page 2-27

Organization: 2048 x 8
No. of Pins: DIP 8, SOIC 8

Speed (ms)	Voltage	Package P	Package S1	Temperature Range	I_{SB} (µA)	I_{CC} (µA)	f_{MAX} (kHz)
10	1.8	•	•	C	3.0	800	100
10	1.8	•	•	I	3.0	800	100
10	2.5	•	•	C	4.0	1000	100
10	2.5	•	•	I	4.0	1000	100
10	2.7	•	•	C	4.0	1500	100
10	2.7	•	•	I	4.0	1500	100
10	5.0	•	•	C	18.0	3000	100
10	5.0	•	•	I	18.0	3000	100

Package Type	
P	8P3, 8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
S1	8S1, 8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
Voltage Range	
1.8	Low Voltage (1.8 V to 6.0 V)
2.5	Low Voltage (2.5 V to 6.0 V)
2.7	Low Voltage (2.7 V to 6.0 V)
5.0	Standard Device (4.5 V to 6.0 V)

CMOS Serial E²PROM Product Selection Guide

AT93C46

see page 2-37

Organization: 64 x 16 or 128 x 8
No. of Pins: DIP 8, SOIC 8

Speed (ms)	Voltage	Package P	Package S1	Package W	Temperature Range	I_{SB} (µA)	I_{CC} (µA)	fMAX (kHz)
10	1.8	•	•		C	0.1	40	250
10	1.8	•	•		I	0.1	40	250
10	2.5	•	•		C	7.0	300	500
10	2.5	•	•		I	7.0	300	500
10	2.7	•	•		C	10.0	400	1000
10	2.7	•	•		I	10.0	400	1000
10	5.0	•	•	•	C	30.0	1000	1000
10	5.0	•	•	•	I	30.0	1000	1000
10	5.0	•			M	30.0	1000	1000

AT93C46R (Rotated)

see page 2-37

Organization: 64 x 16 or 128 x 8
No. of Pins: SOIC 8

Speed (ms)	Voltage	Package S1	Temperature Range	I_{SB} (µA)	I_{CC} (µA)	fMAX (kHz)
10	1.8	•	C	0.1	40	250
10	1.8	•	I	0.1	40	250
10	2.5	•	C	7.0	300	500
10	2.5	•	I	7.0	300	500
10	2.7	•	C	10.0	400	1000
10	2.7	•	I	10.0	400	1000
10	5.0	•	C	30.0	1000	1000
10	5.0	•	I	30.0	1000	1000

Package Type	
P	8P3, 8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
S1	8S1, 8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
W	Die
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
Voltage Range	
1.8	Low Voltage (1.8 V to 5.5 V)
2.5	Low Voltage (2.5 V to 5.5 V)
2.7	Low Voltage (2.7 V to 5.5 V)
5.0	Standard Device (4.5 V to 5.5 V)

AT93C46W

see page 2-37

Organization: 64 x 16 or 128 x 8
No. of Pins: SOIC 8

Speed (ms)	Voltage	Package S2	Temperature Range	I_{SB} (µA)	I_{CC} (µA)	f_{MAX} (kHz)
10	1.8	•	C	0.1	40	250
10	1.8	•	I	0.1	40	250
10	2.5	•	C	7.0	300	500
10	2.5	•	I	7.0	300	500
10	2.7	•	C	10.0	400	1000
10	2.7	•	I	10.0	400	1000
10	5.0	•	C	30.0	1000	1000
10	5.0	•	I	30.0	1000	1000

Package Type	
S2	8S2, 8 Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
Voltage Range	
1.8	Low Voltage (1.8 V to 5.5 V)
2.5	Low Voltage (2.5 V to 5.5 V)
2.7	Low Voltage (2.7 V to 5.5 V)
5.0	Standard Device (4.5 V to 5.5 V)

CMOS Serial E²PROM Product Selection Guide

AT93C56

see page 2-37

Organization: 128 x 16 or 256 x 8
No. of Pins: DIP 8, SOIC 8

Speed (ms)	Voltage	Package P	Package S1	Package W	Temperature Range	I_{SB} (µA)	I_{CC} (µA)	fMAX (kHz)
10	1.8	•	•		C	0.1	40	250
10	1.8	•	•		I	0.1	40	250
10	2.5	•	•		C	7.0	300	500
10	2.5	•	•		I	7.0	300	500
10	2.7	•	•		C	10.0	400	1000
10	2.7	•	•		I	10.0	400	1000
10	5.0	•	•	•	C	30.0	1000	1000
10	5.0	•	•	•	I	30.0	1000	1000
10	5.0	•			M	30.0	1000	1000

AT93C56W

see page 2-37

Organization: 128 x 16 or 256 x 8
No. of Pins: SOIC 8

Speed (ms)	Voltage	Package S2	Temperature Range	I_{SB} (µA)	I_{CC} (µA)	fMAX (kHz)
10	1.8	•	C	0.1	40	250
10	1.8	•	I	0.1	40	250
10	2.5	•	C	7.0	300	500
10	2.5	•	I	7.0	300	500
10	2.7	•	C	10.0	400	1000
10	2.7	•	I	10.0	400	1000
10	5.0	•	C	30.0	1000	1000
10	5.0	•	I	30.0	1000	1000

Package Type	
P	8P3, 8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
S1	8S1, 8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
S2	8S2, 8 Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
W	Die
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
Voltage Range	
1.8	Low Voltage (1.8 V to 5.5 V)
2.5	Low Voltage (2.5 V to 5.5 V)
2.7	Low Voltage (2.7 V to 5.5 V)
5.0	Standard Device (4.5 V to 5.5 V)

AT93C57

see page 2-37

Organization: 128 x 16 or 256 x 8
No. of Pins: DIP 8, SOIC 8

Speed (ms)	Voltage	Package P	Package S1	Package W	Temperature Range	I_{SB} (µA)	I_{CC} (µA)	fMAX (kHz)
10	1.8	•	•		C	0.1	40	250
10	1.8	•	•		I	0.1	40	250
10	2.5	•	•		C	7.0	300	500
10	2.5	•	•		I	7.0	300	500
10	2.7	•	•		C	10.0	400	1000
10	2.7	•	•		I	10.0	400	1000
10	5.0	•	•	•	C	30.0	1000	1000
10	5.0	•	•	•	I	30.0	1000	1000
10	5.0	•			M	30.0	1000	1000

AT93C57W

see page 2-37

Organization: 128 x 16 or 256 x 8
No. of Pins: SOIC 8

Speed (ms)	Voltage	Package S2	Temperature Range	I_{SB} (µA)	I_{CC} (µA)	fMAX (kHz)
10	1.8	•	C	0.1	40	250
10	1.8	•	I	0.1	40	250
10	2.5	•	C	7.0	300	500
10	2.5	•	I	7.0	300	500
10	2.7	•	C	10.0	400	1000
10	2.7	•	I	10.0	400	1000
10	5.0	•	C	30.0	1000	1000
10	5.0	•	I	30.0	1000	1000

Package Type	
P	8P3, 8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
S1	8S1, 8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
S2	8S2, 8 Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
W	Die
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
Voltage Range	
1.8	Low Voltage (1.8 V to 5.5 V)
2.5	Low Voltage (2.5 V to 5.5 V)
2.7	Low Voltage (2.7 V to 5.5 V)
5.0	Standard Device (4.5 V to 5.5 V)

CMOS Serial E²PROM Product Selection Guide

AT93C66

see page 2-37

Organization: 258 x 16 or 512 x 8
No. of Pins: DIP 8, SOIC 8

Speed (ms)	Voltage	Package P	Package S1	Package W	Temperature Range	I_{SB} (µA)	I_{CC} (µA)	fMAX (kHz)
10	1.8	•	•		C	0.1	40	250
10	1.8	•	•		I	0.1	40	250
10	2.5	•	•		C	7.0	300	500
10	2.5	•	•		I	7.0	300	500
10	2.7	•	•		C	10.0	400	1000
10	2.7	•	•		I	10.0	400	1000
10	5.0	•	•	•	C	30.0	1000	1000
10	5.0	•	•	•	I	30.0	1000	1000
10	5.0	•			M	30.0	1000	1000

AT93C66W

see page 2-37

Organization: 258 x 16 or 512 x 8
No. of Pins: SOIC 8

Speed (ms)	Voltage	Package S2	Temperature Range	I_{SB} (µA)	I_{CC} (µA)	fMAX (kHz)
10	1.8	•	C	0.1	40	250
10	1.8	•	I	0.1	40	250
10	2.5	•	C	7.0	300	500
10	2.5	•	I	7.0	300	500
10	2.7	•	C	10.0	400	1000
10	2.7	•	I	10.0	400	1000
10	5.0	•	C	30.0	1000	1000
10	5.0	•	I	30.0	1000	1000

Package Type	
P	8P3, 8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
S1	8S1, 8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
S2	8S2, 8 Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
W	Die
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
Voltage Range	
1.8	Low Voltage (1.8 V to 5.5 V)
2.5	Low Voltage (2.5 V to 5.5 V)
2.7	Low Voltage (2.7 V to 5.5 V)
5.0	Standard Device (4.5 V to 5.5 V)

AT59C11

see page 2-51

Organization: 64 x 16 or 128 x 8
No. of Pins: DIP 8

Speed (ms)	Voltage	Package P	Temperature Range	I_{SB} (µA)	I_{CC} (µA)	fMAX (kHz)
10	1.8	•	C	0.1	40	250
10	1.8	•	I	0.1	40	250
10	2.5	•	C	7.0	300	500
10	2.5	•	I	7.0	300	500
10	2.7	•	C	10.0	400	1000
10	2.7	•	I	10.0	400	1000
10	5.0	•	C	30.0	1000	1000
10	5.0	•	I	30.0	1000	1000

AT59C11W

see page 2-51

Organization: 64 x 16 or 128 x 8
No. of Pins: SOIC 8

Speed (ms)	Voltage	Package S2	Temperature Range	I_{SB} (µA)	I_{CC} (µA)	fMAX (kHz)
10	1.8	•	C	0.1	40	250
10	1.8	•	I	0.1	40	250
10	2.5	•	C	7.0	300	500
10	2.5	•	I	7.0	300	500
10	2.7	•	C	10.0	400	1000
10	2.7	•	I	10.0	400	1000
10	5.0	•	C	30.0	1000	1000
10	5.0	•	I	30.0	1000	1000

Package Type	
P	8P3, 8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
S2	8S2, 8 Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
Voltage Range	
1.8	Low Voltage (1.8 V to 5.5 V)
2.5	Low Voltage (2.5 V to 5.5 V)
2.7	Low Voltage (2.7 V to 5.5 V)
5.0	Standard Device (4.5 V to 5.5 V)

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AT59C22

see page 2-51

Organization: 128 x 16 or 256 x 8
No. of Pins: DIP 8

Speed (ms)	Voltage	Package P	Temperature Range	I_{SB} (µA)	I_{CC} (µA)	fMAX (kHz)
10	1.8	•	C	0.1	40	250
10	1.8	•	I	0.1	40	250
10	2.5	•	C	7.0	300	500
10	2.5	•	I	7.0	300	500
10	2.7	•	C	10.0	400	1000
10	2.7	•	I	10.0	400	1000
10	5.0	•	C	30.0	1000	1000
10	5.0	•	I	30.0	1000	1000

AT59C22W

see page 2-51

Organization: 128 x 16 or 256 x 8
No. of Pins: SOIC 8

Speed (ms)	Voltage	Package S2	Temperature Range	I_{SB} (µA)	I_{CC} (µA)	fMAX (kHz)
10	1.8	•	C	0.1	40	250
10	1.8	•	I	0.1	40	250
10	2.5	•	C	7.0	300	500
10	2.5	•	I	7.0	300	500
10	2.7	•	C	10.0	400	1000
10	2.7	•	I	10.0	400	1000
10	5.0	•	C	30.0	1000	1000
10	5.0	•	I	30.0	1000	1000

Package Type	
P	8P3, 8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
S2	8S2, 8 Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
Voltage Range	
1.8	Low Voltage (1.8 V to 5.5 V)
2.5	Low Voltage (2.5 V to 5.5 V)
2.7	Low Voltage (2.7 V to 5.5 V)
5.0	Standard Device (4.5 V to 5.5 V)

AT59C13

see page 2-51

Organization: 256 x 16 or 512 x 8
No. of Pins: DIP 8

Speed (ms)	Voltage	Package P	Temperature Range	I_{SB} (µA)	I_{CC} (µA)	fMAX (kHz)
10	1.8	•	C	0.1	40	250
10	1.8	•	I	0.1	40	250
10	2.5	•	C	7.0	300	500
10	2.5	•	I	7.0	300	500
10	2.7	•	C	10.0	400	1000
10	2.7	•	I	10.0	400	1000
10	5.0	•	C	30.0	1000	1000
10	5.0	•	I	30.0	1000	1000

AT59C13W

see page 2-51

Organization: 256 x 16 or 512 x 8
No. of Pins: SOIC 8

Speed (ms)	Voltage	Package S2	Temperature Range	I_{SB} (µA)	I_{CC} (µA)	fMAX (kHz)
10	1.8	•	C	0.1	40	250
10	1.8	•	I	0.1	40	250
10	2.5	•	C	7.0	300	500
10	2.5	•	I	7.0	300	500
10	2.7	•	C	10.0	400	1000
10	2.7	•	I	10.0	400	1000
10	5.0	•	C	30.0	1000	1000
10	5.0	•	I	30.0	1000	1000

Package Type	
P	8P3, 8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
S2	8S2, 8 Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
Voltage Range	
1.8	Low Voltage (1.8 V to 5.5 V)
2.5	Low Voltage (2.5 V to 5.5 V)
2.7	Low Voltage (2.7 V to 5.5 V)
5.0	Standard Device (4.5 V to 5.5 V)

CMOS Parallel E²PROM Product Selection Guide

AT28C04

see page 2-63

Organization: 512 x 8
No. of Pins: DIP 24, LCC 32

Speed (ns)	Package D	Package P	Package W	Temperature Range	Option	Icc (mA) Active	Icc (mA) Standby
150	•	•		C	E, F	30	0.1
150	•	•		I	E, F	45	0.1
150	•			M/883	E, F	45	0.1
200	•	•		C	E, F	30	0.1
200	•	•		I	E, F	45	0.1
200	•			M/883	E, F	45	0.1
250	•	•	•	C	E, F	30	0.1
250	•	•		I	E, F	45	0.1
250	•			M/883	E, F	45	0.1

Package Type	
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
W	Die
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 1 ms
E	High Endurance Option: Endurance = 100K Write Cycles; Write Time = 200 µs
F	Fast Write Option: Write Time = 200 µs

AT28C16

see page 2-71

Organization: 2K x 8
No. of Pins: DIP 28, LCC 32, SOIC 24

Speed (ns)	Package D	J	L	P	S	W	Temperature Range	Option	Icc (mA) Active	Standby
150	•	•		•	•		C	E, F	30	0.1
150	•	•		•	•		I	E, F	45	0.1
150	•		•				M/883	E, F	45	0.1
200	•	•		•	•		C	E, F	30	0.1
200	•	•		•	•		I	E, F	45	0.1
200	•		•				M/883	E, F	45	0.1
250	•	•		•	•	•	C	E, F	30	0.1
250	•	•		•	•		I	E, F	45	0.1
250	•		•				M/883	E, F	45	0.1

AT28HC16

- Not recommended for new designs. Use AT28HC191 or AT28HC291.

AT28HC16L

- Not recommended for new designs. Use AT28HC191 or AT28HC291.

Package Type	
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
L	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
S	24S, 24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
W	Die
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 1 ms
E	High Endurance Option: Endurance = 100K Write Cycles; Write Time = 200 µs
F	Fast Write Option: Write Time = 200 µs

CMOS Parallel E²PROM Product Selection Guide

AT28C17

see page 2-81

Organization: 2K x 8
No. of Pins: DIP 28, LCC 32, SOIC 24

Speed (ns)	Package D	J	L	P	S	W	Temperature Range	Option	Icc (mA) Active	Standby
150	•	•		•	•		C	E, F	30	0.1
150	•	•		•	•		I	E, F	45	0.1
150	•		•				M/883	E, F	45	0.1
200	•	•		•	•		C	E, F	30	0.1
200	•	•		•	•		I	E, F	45	0.1
200	•		•				M/883	E, F	45	0.1
250	•	•		•	•	•	C	E, F	30	0.1
250	•	•		•	•		I	E, F	45	0.1
250	•		•				M/883	E, F	45	0.1

Package Type	
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
L	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
S	24S, 24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
W	Die
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms
E	High Endurance Option: Endurance = 100K Write Cycles; Write Time = 200 µs
F	Fast Write Option: Write Time = 200 µs

AT28C64

see page 2-91

Organization: 8K x 8
No. of Pins: DIP 28, LCC 32, SOIC 28, TSOP 28

Speed (ns)	Package D	F	J	L	P	S	T	W	Temperture Range	Option	Icc (mA) Active	Standby
120	•		•		•	•			C	E, F	30	0.1
120	•		•		•	•			I	E, F	45	0.1
120	•	•		•					M/883	E, F	45	0.1
150	•		•		•	•	•		C	E, F	30	0.1
150	•		•		•	•	•		I	E, F	45	0.1
150	•	•		•					M/883	E, F	45	0.1
200	•		•		•	•			C	E, F	30	0.1
200	•		•		•	•			I	E, F	45	0.1
200	•	•		•					M/883	E, F	45	0.1
250	•		•		•	•		•	C	E, F	30	0.1
250	•		•		•	•			I	E, F	45	0.1
250	•	•		•					M/883	E, F	45	0.1
300	•	•		•					M/883	E, F	45	0.1
350	•	•		•					M/883	E, F	45	0.1
SMD Number for AT28C64												
150	•			•					M/883		45	0.1
200	•			•					M/883		45	0.1
250	•	•		•					M/883		45	0.1
300	•			•					M/883		45	0.1
350	•	•		•					M/883		45	0.1

Package Type	
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
F	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
L	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
S	28S, 28 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
T	28T, 28 Lead, Plastic Thin Small Outline Package (TSOP)
W	Die
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 1 ms
E	High Endurance Option: Endurance = 100K Write Cycles; Write Time = 200 µs
F	Fast Write Option: Write Time = 200 µs

CMOS Parallel E²PROM Product Selection Guide

AT28C64X

see page 2-91

Organization: 8K x 8 No. of Pins: DIP 28, LCC 32, SOIC 28	Speed (ns)	Package D	F	J	L	P	S	Temperature Range	Icc (mA) Active	Standby
	150	•	•	•		•	•	C	30	0.1
	150	•	•	•		•	•	I	45	0.1
	150	•	•		•			M/883	45	0.1
	200	•	•	•		•	•	C	30	0.1
	200	•	•	•		•	•	I	45	0.1
	200	•	•		•			M/883	45	0.1
	250	•	•	•		•	•	C	30	0.1
	250	•	•	•		•	•	I	45	0.1
	250	•	•		•			M/883	45	0.1
	300	•	•		•			M/883	45	0.1
	350	•	•		•			M/883	45	0.1
	450	•	•		•			M/883	45	0.1
SMD Number for AT28C64X										
5962-87514 22	150	•			•			M/883	45	0.1
5962-87514 21	200	•			•			M/883	45	0.1
5962-87514 20	250	•	•		•			M/883	45	0.1
5962-87514 19	300	•			•			M/883	45	0.1
5962-87514 18	350	•			•			M/883	45	0.1

Package Type	
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
F	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
L	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
S	28S, 28 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

AT28HC64

see page 2-103

Organization: 8K x 8
No. of Pins: DIP 28, LCC 32, TSOP 28

Speed (ns)	Package D	J	L	P	T	Temperature Range	Option	Icc (mA) Active	Standby
55	•	•		•		C	E	80	60
55	•	•		•		I	E	80	60
70	•	•		•		C	E	80	60
70	•	•		•		I	E	80	60
70	•		•			M/883	E	80	60
90	•	•		•	•	C	E	80	60
90	•	•		•	•	I	E	80	60
90	•		•			M/883	E	80	60
120	•	•		•		C	E	80	60
120	•	•		•		I	E	80	60
120	•		•			M/883	E	80	60

Package Type	
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
L	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
T	28T, 28 Lead, Plastic Thin Small Outline Package (TSOP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 2 ms
E	High Endurance Option: Endurance = 100K Write Cycles

CMOS Parallel E²PROM Product Selection Guide

AT28HC64L

see page 2-103

Organization: 8K x 8
No. of Pins: DIP 28, LCC 32

Speed (ns)	Package D	J	L	P	W	Temperature Range	Option	Icc (mA) Active	Standby
70	•	•		•		C	E	80	0.1
70	•	•		•		I	E	80	0.1
90	•	•		•		C	E	80	0.1
90	•	•		•		I	E	80	0.1
90	•		•			M/883	E	80	0.2
120	•	•		•	•	C	E	80	0.1
120	•	•		•		I	E	80	0.1
120	•		•			M/883	E	80	0.2

SMD Number for AT28HC64L

5962-87514 12	70	•		•			M/883		80	0.2
5962-87514 11	90	•		•			M/883		80	0.2
5962-87514 10	120	•		•			M/883		80	0.2

Package Type	
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
L	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
W	Die
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 2 ms
E	High Endurance Option: Endurance = 100K Write Cycles

AT28LV64

see page 2-115

Organization: 8K x 8 No. of Pins: DIP 28, LCC 32, SOIC 28, TSOP 28	Speed (ns)	Operating Voltage Range	Package J	P	S	T	Temperature Range	Icc (mA) Active	Standby
	200	3.0 V to 3.6 V	•	•	•	•	C	8	0.05
	200	3.0 V to 3.6 V	•	•	•	•	I	8	0.05
	300	2.7 V to 3.6 V	•	•	•	•	C	8	0.05
	300	2.7 V to 3.6 V	•	•	•	•	I	8	0.05

Package Type	
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
S	28S, 28 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
T	28T, 28 Lead, Plastic Thin Small Outline Package (TSOP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)

CMOS Parallel E²PROM Product Selection Guide

AT28C64B

see page 2-123

Organization: 8K x 8
No. of Pins: DIP 28, LCC 32, SOIC 28, TSOP 28, PGA 28

Speed (ns)	Package D	J	P	S	T	U	Temperature Range	Icc (mA) Active	Standby
150	•	•	•	•	•		C	60	0.1
150	•	•	•	•	•		I	60	0.1
150	•					•	M/883	80	0.2
200	•	•	•	•	•		C	60	0.1
200	•	•	•	•	•		I	60	0.1
200	•					•	M/883	80	0.2
250	•	•	•	•	•		C	60	0.1
250	•	•	•	•	•		I	60	0.1
250	•					•	M/883	80	0.2

Package Type	
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
S	28S, 28 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
T	28T, 28 Lead, Plastic Thin Small Outline Package (TSOP)
U	28U, 28 Pin, Ceramic Pin Grid Array (PGA)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

AT28PC64

see page 2-135

Organization: 8K x 8
No. of Pins: DIP 28, LCC 32, TSOP 28

Speed (ns)	Package D	J	L	P	T	W	Temperature Range	Option	Icc (mA) Active	Standby
150	•	•		•	•		C	E	80	0.1
150	•	•		•	•		I	E	80	0.1
150	•		•				M/883	E	80	0.2
200	•	•		•			C	E	80	0.1
200	•	•		•			I	E	80	0.1
200	•		•				M/883	E	80	0.2
250	•	•		•		•	C	E	80	0.1
250	•	•		•			I	E	80	0.1
250	•		•				M/883	E	80	0.2
300	•		•				M/883	E	80	0.2
350	•		•				M/883	E	80	0.2
SMD Number for AT28PC64										
5962-87514 09	200	•		•				M/883		80	0.2
5962-87514 08	250	•		•				M/883		80	0.2
5962-87514 07	300	•		•				M/883		80	0.2
5962-87514 06	350	•		•				M/883		80	0.2

Package Type	
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
L	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
T	28T, 28 Lead, Plastic Thin Small Outline Package (TSOP)
W	Die
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 2 ms
E	High Endurance Option: Endurance = 100K Write Cycles

CMOS Parallel E²PROM Product Selection Guide

AT28C256

see page 2-147

Organization: 32K x 8 No. of Pins: DIP 28, LCC 32, TSOP 28	Speed (ns)	Package D	F	J	L	P	T	U	W	Temperature Range	Option	Icc (mA) Active	Standby
	150	•		•		•	•	•		C	E, F	80	0.2
	150	•		•		•	•	•		I	E, F	80	0.2
	150	•	•		•			•		M/883	E, F	80	0.3
	200	•		•		•		•		C	E, F	80	0.2
	200	•		•		•		•		I	E, F	80	0.2
	200	•	•		•			•		M/883	E, F	80	0.3
	250	•		•		•		•	•	C	E, F	80	0.2
	250	•		•		•		•		I	E, F	80	0.2
	250	•	•		•			•		M/883	E, F	80	0.3
	300	•	•		•			•		M/883	E, F	80	0.3
	350	•	•		•			•		M/883	E, F	80	0.3
SMD Number for AT28C256													
5962-88525 06	150	•	•		•			•		M/883		80	0.35
5962-88525 07	150	•	•		•			•		M/883	F	80	0.35
5962-88525 04	200	•	•		•			•		M/883		80	0.35
5962-88525 03	250	•	•		•			•		M/883		80	0.35
5962-88525 05	250	•	•		•			•		M/883	E	80	0.35
5962-88525 02	300	•	•		•			•		M/883		80	0.35
5962-88525 01	350	•	•		•			•		M/883		80	0.35

Package Type	
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
F	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
L	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
T	28T, 28 Lead, Plastic Thin Small Outline Package (TSOP)
U	28U, 28 Pin, Ceramic Pin Grid Array (PGA)
W	Die
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 2 ms
E	High Endurance Option: Endurance = 100K Write Cycles
F	Fast Write Option: Write Time = 3ms

CMOS Parallel E²PROM Product Selection Guide

AT28HC256

see page 2-159

Organization: 32K x 8
No. of Pins: DIP 28, LCC 32, TSOP 28, PGA 28

Speed (ns)	Package D	F	J	L	P	T	U	Temperature Range	Option	Icc (mA) Active	Standby
70	•		•		•			C	E, F	80	60
70	•		•		•			I	E, F	80	60
90	•		•		•		•	C	E, F	80	60
90	•		•		•		•	I	E, F	80	60
90	•	•		•			•	M/883	E, F	80	60
120	•		•		•	•	•	C	E, F	80	60
120	•		•		•	•	•	I	E, F	80	60
120	•	•		•			•	M/883	E, F	80	60
SMD Number for AT28HC256											
5962-88634 03	90	•	•		•			•	M/883		80	60
5962-88634 04	90	•	•		•			•	M/883	F	80	60

Package Type	
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
F	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
L	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
T	28T, 28 Lead, Plastic Thin Small Outline Package (TSOP)
U	28U, 28 Pin, Ceramic Pin Grid Array (PGA)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms
E	High Endurance Option: Endurance = 100K Write Cycles
F	Fast Write Option: Write Time = 3 ms

CMOS Parallel E²PROM Product Selection Guide

AT28HC256L

see page 2-159

Organization: 32K x 8
No. of Pins: DIP 28, LCC 32, PGA 28

Speed (ns)	Package D	F	J	L	P	U	W	Temperature Range	Option	Icc (mA) Active	Standby
90	•		•		•	•		C	E, F	80	0.3
90	•		•		•	•		I	E, F	80	0.3
120	•		•		•	•	•	C	E, F	80	0.3
120	•		•		•	•		I	E, F	80	0.3
120	•	•		•		•		M/883	E, F	80	0.3
SMD Number for AT28HC256L											
5962-88634 01 120	•	•		•		•		M/883		80	0.3
5962-88634 02 120	•	•		•		•		M/883	F	80	0.3

Package Type	
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
F	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
L	32L, 32 Pad, Non Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
U	28U, 28 Pin, Ceramic Pin Grid Array (PGA)
W	Die
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms
E	High Endurance Option: Endurance = 100K Write Cycles
F	Fast Write Option: Write Time = 3 ms

AT28C1024

see page 2-173

Organization: 64K x 16
No. of Pins: DIP 40, LCC 44

Speed (ns)	Package B	Package L	Package W	Temperature Range	Icc (mA) Active	Icc (mA) Standby
120	•	•		C	100	0.4
120	•	•		I	100	0.4
150	•	•		C	100	0.4
150	•	•		I	100	0.4
150	•	•		M	100	0.4
150	•	•		M/883	100	0.4
200	•	•		C	100	0.4
200	•	•		I	100	0.4
200	•	•		M	100	0.4
200	•	•		M/883	100	0.4
250	•	•	•	C	100	0.4
250	•	•		I	100	0.4
250	•	•		M	100	0.4
250	•	•		M/883	100	0.4

Package Type	
B	40B, 40 Lead, 0.600" Wide, Ceramic Side Braze Dual Inline (Side Braze)
L	44L, 44 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
W	Die
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS Parallel E²PROM Product Selection Guide

AT28C010

see page 2-183

Organization: 128K x 8
No. of Pins: DIP 32, LCC 44

Speed (ns)	Package B	F	L	U	V	W	Temperature Range	Option	Icc (mA) Active	Standby
120	•	•	•				C	E	80	0.3
120	•	•	•				I	E	80	0.3
120	•	•	•				M	E	80	0.3
120	•	•	•				M/883	E	80	0.3
150	•	•	•	•	•		C	E	80	0.3
150	•	•	•	•	•		I	E	80	0.3
150	•	•	•	•	•		M	E	80	0.3
150	•	•	•	•			M/883	E	80	0.3
200	•	•	•	•	•		C	E	80	0.3
200	•	•	•	•	•		I	E	80	0.3
200	•	•	•	•	•		M	E	80	0.3
200	•	•	•	•			M/883	E	80	0.3
250	•	•	•	•	•	•	C	E	80	0.3
250	•	•	•	•	•		I	E	80	0.3
250	•	•	•	•	•		M	E	80	0.3
250	•	•	•	•			M/883	E	80	0.3

SMD Number for AT28C010

5962-38267 07 M	120	•	•	•				M/883		80	0.3
5962-38267 05 M	150	•	•	•				M/883		80	0.3
5962-38267 03 M	200	•	•	•				M/883		80	0.3
5962-38267 01 M	250	•	•	•				M/883		80	0.3

Package Type	
B	32B, 32 Lead, 0.600" Wide Ceramic Side Braze Dual Inline (Side Braze)
F	32F, 32 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
L	44L, 44 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
U	30U, 30 Pin, Ceramic Pin Grid Array (PGA)
V	Tape Automated Bond (TAB) Carrier
W	Die
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 2 ms
E	High Endurance Option: Endurance = 100K Write Cycles

CMOS Parallel E²PROM Product Selection Guide

AT28MC010

- Not recommended for new designs. Use AT28C010

AT28MC020

see page 2-195

Organization: 256K x 8
No. of Pins: DIP 32

Speed (ns)	Package Z	Temperature Range	Icc (mA) Active	Icc (mA) Standby
150	•	C	80	0.5
150	•	I	80	0.5
150	•	M	80	0.5
150	•	MB	80	0.5
200	•	C	80	0.5
200	•	I	80	0.5
200	•	M	80	0.5
200	•	MB	80	0.5
250	•	C	80	0.5
250	•	I	80	0.5
250	•	M	80	0.5
250	•	MB	80	0.5

Package Type	
Z	32Z, 32 Lead, Non-Windowed, Ceramic Dual Inline 32D6 Compatible Multi-Chip Module (MCM)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
MB	Screened IAW M5004, MIL-STD-883C, Class B Components (-55°C to 125°C)

CMOS Parallel E²PROM Product Selection Guide

AT28MC040

see page 2-205

Organization: 512K x 8
No. of Pins: DIP 32

Speed (ns)	Package M[1]	Package Z[2]	Temperature Range	Icc (mA) Active	Icc (mA) Standby
150	•	•	C	80	0.5
150	•	•	I	80	0.5
150	•	•	M	80	0.5
150	•	•	MB	80	0.5
200	•	•	C	80	0.5
200	•	•	I	80	0.5
200	•	•	M	80	0.5
200	•	•	MB	80	0.5
250	•	•	C	80	0.5
250	•	•	I	80	0.5
250	•	•	M	80	0.5
250	•	•	MB	80	0.5

Package Type	
M	32M2, 32 Lead, Non-Windowed, Ceramic Dual Inline 32D6 Compatible Flatpack Module (Module)
Z	32Z, 32 Lead, Non-Windowed, Ceramic Dual Inline 32D6 Compatible Multi-Chip Module (MCM)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
MB[1,2]	High Reliability Military (-55°C to 125°C)

Notes: 1. Device package and temperature combinations designated MMB are modules comprised of individual microcircuits compliant with MIL-STD-883, for Class B components.
2. Device package and temperature combinations designated ZMB are multichip microcircuits that have been screened in accordance with Method 5004 of MIL-STD-883.

AT29C256

see page 3-3

Organization: 32K x 8
No. of Pins: DIP 28, LCC 32, TSOP 28

Speed (ns)	Package D	J	L	P	T	Temperature Range	Power Supply	Icc (mA) Active	Standby
90	•	•		•		C	10%	80	0.3
120	•	•	•	•	•	C	10%	80	0.3
120	•	•	•	•		I	10%	80	0.3
120	•		•			M	10%	80	0.3
120	•		•			M/883	10%	80	0.3
150	•	•	•	•	•	C	10%	80	0.3
150	•	•	•	•		I	10%	80	0.3
150	•		•			M	10%	80	0.3
150	•		•			M/883	10%	80	0.3
200	•	•	•	•		C	10%	80	0.3
200	•	•	•	•		I	10%	80	0.3
200	•		•			M	10%	80	0.3
200	•		•			M/883	10%	80	0.3
250	•	•	•	•		C	10%	80	0.3
250	•	•	•	•		I	10%	80	0.3
250	•		•			M	10%	80	0.3
250	•		•			M/883	10%	80	0.3

Package Type	
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
L	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package PDIP)
T	28T, 28 Lead, Plastic Thin Small Outline Package (TSOP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

AT29LV256

see page 3-17

Organization: 32K x 8
No. of Pins: DIP 28, LCC 32, TSOP 28

Speed (ns)	Package D	J	P	T	Temperature Range	Power Supply	Icc (mA) Active	Standby
200	•	•	•	•	C	10%	15	0.02
200	•	•	•		I	10%	15	0.02
250	•	•	•	•	C	10%	15	0.02
250	•	•	•		I	10%	15	0.02

Package Type	
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
T	28T, 28 Lead, Plastic Thin Small Outline Package (TSOP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)

AT29C257

see page 3-27

Organization: 32K x 8
No. of Pins: DIP 32, LCC 32

Speed (ns)	Package D	J	L	P	Temperature Range	Power Supply	Icc (mA) Active	Standby
90	•	•		•	C	10%	80	0.3
120	•	•	•	•	C	10%	80	0.3
120	•	•	•	•	I	10%	80	0.3
150	•	•	•	•	C	10%	80	0.3
150	•	•	•	•	I	10%	80	0.3
200	•	•	•	•	C	10%	80	0.3
200	•	•	•	•	I	10%	80	0.3
250	•	•	•	•	C	10%	80	0.3
250	•	•	•	•	I	10%	80	0.3

Package Type	
D	32D6, 32 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
L	32L, 32 Pad, Non Windowed, Ceramic Leadless Chip Carrier (LCC)
P	32P6, 32 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)

CMOS PEROM Product Selection Guide

AT29C512

see page 3-39

Organization: 64K x 8
No. of Pins: DIP 32, LCC 32, TSOP 32

Speed (ns)	Package D	Package J	Package P	Package T	Temperature Range	Power Supply	Icc (mA) Active	Icc (mA) Standby
90	•	•	•		C	10%	50	0.1
90	•	•	•		I	10%	50	0.3
120	•	•	•	•	C	10%	50	0.1
120	•	•	•		I	10%	50	0.3
120	•				M	10%	50	0.3
120	•				M/883	10%	50	0.3
150	•	•	•	•	C	10%	50	0.1
150	•	•	•		I	10%	50	0.3
150	•				M	10%	50	0.3
150	•				M/883	10%	50	0.3
200	•	•	•		C	10%	50	0.1
200	•	•	•		I	10%	50	0.3
200	•				M	10%	50	0.3
200	•				M/883	10%	50	0.3

Package Type	
D	32D6, 32 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
P	32P6, 32 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
T	32T, 32 Lead, Plastic Thin Small Outline Package (TSOP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

AT29LV512

see page 3-53

Organization: 64K x 8
No. of Pins: DIP 32, LCC 32, TSOP 32

Speed (ns)	Package D	J	P	T	Temperature Range	Power Supply	Icc (mA) Active	Standby
200	•	•	•	•	C	10%	15	0.02
200	•	•	•		I	10%	15	0.05
250	•	•	•	•	C	10%	15	0.02
250	•	•	•		I	10%	15	0.05

Package Type	
D	32D6, 32 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
P	32P6, 32 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
T	32T, 32 Lead, Plastic Thin Small Outline Package (TSOP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Idustrial (-40°C to 85°C)

CMOS PEROM Product Selection Guide

AT29C010

see page 3-63

Organization: 128K x 8
No. of Pins: DIP 32, LCC 32, TSOP 32

Speed (ns)	Package D	J	L	P	T	Temperature Range	Power Supply	Icc (mA) Active	Standby
90	•	•	•	•		C	10%	50	0.1
90	•	•	•	•		I	10%	50	0.3
120	•	•	•	•	•	C	10%	50	0.1
120	•	•	•	•		I	10%	50	0.3
120	•		•			M	10%	50	0.3
120	•		•			M/883	10%	50	0.3
150	•	•	•	•	•	C	10%	50	0.1
150	•	•	•	•		I	10%	50	0.3
150	•		•			M	10%	50	0.3
150	•		•			M/883	10%	50	0.3
200	•	•	•	•		C	10%	50	0.1
200	•	•	•	•		I	10%	50	0.3
200	•		•			M	10%	50	0.3
200	•		•			M/883	10%	50	0.3

Package Type	
D	32D6, 32 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
L	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
P	32P6, 32 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
T	32T, 32 Lead, Plastic Thin Small Outline Package (TSOP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

AT29LV010

see page 3-77

Organization: 128K x 8
No. of Pins: DIP 32, LCC 32, TSOP 32

Speed (ns)	Package D	Package J	Package P	Package T	Temperature Range	Power Supply	Icc (mA) Active	Icc (mA) Standby
200	•	•	•	•	C	10%	15	0.02
200	•	•	•		I	10%	15	0.02
250	•	•	•	•	C	10%	15	0.02
250	•	•	•		I	10%	15	0.02

Package Type	
D	32D6, 32 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
P	32P6, 32 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
T	32T, 32 Lead, Plastic Thin Small Outline Package (TSOP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)

CMOS EPROM Product Selection Guide

AT27C256R

see page 4-3

Organization: 32K x 8
No. of Pins: DIP 28, LCC 32, TSOP 28

Speed (ns)	Package D	J	K	L	P	R	T	Temperature Range	Power Supply	Icc (mA) Active	Standby
70	•		•	•				C	10%	20	0.1
70	•		•	•				I	10%	25	0.2
90	•	•	•	•	•	•	•	C	10%	20	0.1
90	•	•	•	•	•	•		I	10%	25	0.2
90	•		•	•				M	10%	25	0.2
90	•		•	•				M/883	10%	25	0.2
120	•	•	•	•	•	•	•	C	10%	20	0.1
120	•	•	•	•	•	•		I	10%	25	0.2
120	•		•	•				M	10%	25	0.2
120	•		•	•				M/883	10%	25	0.2
150	•	•	•	•	•	•	•	C	10%	20	0.1
150	•	•	•	•	•	•		I	10%	25	0.2
150	•		•	•				M	10%	25	0.2
150	•		•	•				M/883	10%	25	0.2
200	•	•	•	•	•	•	•	C	10%	20	0.1
200	•	•	•	•	•	•		I	10%	25	0.2
200	•		•	•				M	10%	25	0.2
200	•		•	•				M/883	10%	25	0.2
250	•	•	•	•	•	•	•	C	10%	20	0.1
250	•	•	•	•	•	•		I	10%	25	0.2
250	•		•	•				M	10%	25	0.2
250	•		•	•				M/883	10%	25	0.2

Continued on next page

Package Type	
D	28DW6, 28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	32KW, 32 Lead, Windowed, Ceramic J-Leaded Chip Carrier OTP (JLCC)
L	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
R	28R, 28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline OTP (SOIC)
T	28T, 28 Lead, Plastic Thin Small Outline Package OTP (TSOP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

AT27C256R (Continued)

see page 4-3

Organization: 32K x 8	Speed (ns)	Package							Temperature Range	Power Supply	Icc (mA)	
		D	J	K	L	P	R	T			Active	Standby
SMD Number for part AT27C256R												
5962-86063 07	90	•		•	•				M/883	10%	25	0.2
5962-86063 06	120	•		•	•				M/883	10%	25	0.2
5962-86063 05	150	•		•	•				M/883	10%	25	0.2
5962-86063 04	170	•		•	•				M/883	10%	25	0.2
5962-86063 01	200	•		•	•				M/883	10%	25	0.2
5962-86063 02	250	•		•	•				M/883	10%	25	0.2
5962-86063 03	300	•		•	•				M/883	10%	25	0.2

Package Type	
D	28DW6, 28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	32KW, 32 Lead, Windowed, Ceramic J-Leaded Chip Carrier OTP (JLCC)
L	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
R	28R, 28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline OTP (SOIC)
T	28T, 28 Lead, Plastic Thin Small Outline Package OTP (TSOP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPROM Product Selection Guide

AT27LV256R

see page 4-13

Organization: 32K x 8
No. of Pins: DIP 28, LCC 32, SOIC 28, TSOP 28

Speed (ns)	Package							Temperature Range	I_{CC} (mA)[1]	
	D	J	K	L	P	R	T		Active	Standby
200	•	•	•	•	•	•	•	C	8	0.1
200	•		•	•				I	10	0.1
250	•	•	•	•	•	•	•	C	8	0.1
250	•		•	•				I	10	0.1

Note: 1. V_{CC} = 3.3 V

Package Type	
D	28DW6, 28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	32KW, 32 Lead, Windowed Ceramic J-Leaded Chip Carrier (JLCC)
L	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
R	28R, 28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline OTP (SOIC)
T	28T, 28 Lead, Plastic Thin Small Outline Package OTP (TSOP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)

AT27HC256R Refer to AT27C256R for new designs.

see page 4-21

Organization: 32K x 8 No. of Pins: DIP 28, LCC 32	Speed (ns)	Package D	K	L	Temperature Range	Power Supply	Icc (mA) Active	Standby
	55	•	•	•	C	10%	50	30
	55	•	•	•	I	10%	55	30
	70	•	•	•	I	10%	55	30
	70	•	•	•	M	10%	55	30
	70	•	•	•	M/883	10%	55	30
SMD Number for AT27HC256R								
5962-86063 08	70	•		•	M/883	10%	55	30

AT27HC256RL - Not recommended for new designs. Use AT27C256R

Package Type	
D	28DW6, 28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
K	32KW, 32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPROM Product Selection Guide

AT27C512R

see page 4-27

Organization: 64K x 8
No. of Pins: DIP 28, LCC 32, SOIC 28, TSOP 28

Speed (ns)	Package D	J	K	L	P	R	T	Temperature Range	Power Supply	Icc (mA) Active	Standby
90	•	•	•	•	•	•	•	C	10%	20	0.1
90	•	•	•	•	•	•		I	10%	25	0.2
90	•		•	•				M	10%	25	0.2
120	•	•	•	•	•	•	•	C	10%	20	0.1
120	•	•	•	•	•	•		I	10%	25	0.2
120	•		•	•				M	10%	25	0.2
120	•		•	•				M/883	10%	25	0.2
150	•	•	•	•	•	•	•	C	10%	20	0.1
150	•	•	•	•	•	•		I	10%	25	0.2
150	•		•	•				M	10%	25	0.2
150	•		•	•				M/883	10%	25	0.2
200	•	•	•	•	•	•		C	10%	20	0.1
200	•	•	•	•	•	•		I	10%	25	0.2
200	•		•	•				M	10%	25	0.2
200	•		•	•				M/883	10%	25	0.2
250	•	•	•	•	•	•		C	10%	20	0.1
250	•	•	•	•	•	•		I	10%	25	0.2
250	•		•	•				M	10%	25	0.2
250	•		•	•				M/883	10%	25	0.2
SMD Number for AT27C512R											
120	•		•	•				M/883	10%	25	0.2
150	•		•	•				M/883	10%	25	0.2
200	•		•	•				M/883	10%	25	0.2
250	•		•	•				M/883	10%	25	0.2

Package Type	
D	28DW6, 28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	32KW, 32 Lead, Windowed, Ceramic J-Leaded Chip Carrier OTP (JLCC)
L	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
R	28R, 28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline OTP (SOIC)
T	28T, 28 Lead, Plastic Thin Small Outline Package OTP (TSOP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

AT27LV512R

see page 4-35

Organization: 64K x 8
No. of Pins: DIP 28, LCC 32, SOIC 28, TSOP 28

Speed (ns)	Package							Temperature Range	I_{CC} (mA)[1]	
	D	J	K	L	P	R	T		Active	Standby
200	•	•	•	•	•	•	•	C	8	0.1
200	•		•	•				I	10	0.1
250	•	•	•	•	•	•	•	C	8	0.1
250	•		•	•				I	10	0.1

Note: 1. $V_{CC} = 3.3$ V

	Package Type
D	28DW6, 28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	32KW, 32 Lead, Windowed Ceramic J-Leaded Chip Carrier (JLCC)
L	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
R	28R, 28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline OTP (SOIC)
T	28T, 28 Lead, Plastic Thin Small Outline Package OTP (TSOP)
	Temperature Range
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)

CMOS EPROM Product Selection Guide

AT27C010

see page 4-43

Organization: 128K x 8
No. of Pins: DIP 32, LCC 32, SOIC 32, TSOP 32

Speed (ns)	Package D	J	K	L	P	R	T	Temperature Range	Power Supply	Icc (mA) Active	Standby
100	•		•	•				C	5%	40	0.1
120	•	•	•	•	•	•	•	C	10%	40	0.1
120	•	•	•	•	•	•		I	10%	50	0.1
120	•		•	•				M	10%	50	0.1
120	•		•	•				M/883	10%	50	0.1
150	•	•	•	•	•	•	•	C	10%	40	0.1
150	•	•	•	•	•	•		I	10%	50	0.1
150	•		•	•				M	10%	50	0.1
150	•		•	•				M/883	10%	50	0.1
200	•	•	•	•	•	•		C	10%	40	0.1
200	•	•	•	•	•	•		I	10%	50	0.1
200	•		•	•				M	10%	50	0.1
200	•		•	•				M/883	10%	50	0.1
250	•	•	•	•	•			C	10%	40	0.1
250	•	•	•	•	•			I	10%	50	0.1
250	•		•	•				M	10%	50	0.1
250	•		•	•				M/883	10%	50	0.1
SMD Number for AT27C010											
120	•			•				M/883	10%	50	0.1
150	•							M/883	10%	50	0.1
170	•			•				M/883	10%	50	0.1
200	•			•				M/883	10%	50	0.1
250	•			•				M/883	10%	50	0.1
300	•			•				M/883	10%	50	0.1

Package Type	
D	32DW6, 32 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	32KW, 32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	32P6, 32 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
R	32R, 32 Lead, 0.440" Wide, Plastic Gull Wing Small Outline OTP (SOIC)
T	32T, 32 Lead, Plastic Thin Small Outline Package OTP (TSOP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

AT27C010L

see page 4-43

Organization: 128K x 8
No. of Pins: DIP 32, LCC 32, SOIC 32, TSOP 32

Speed (ns)	Package D	J	K	L	P	R	T	Temperature Range	Power Supply	Icc (mA) Active	Standby
100	•		•	•				C	5%	25	0.1
120	•	•	•	•	•	•	•	C	10%	25	0.1
120	•	•	•	•	•	•		I	10%	30	0.1
120	•		•	•				M	10%	30	0.1
120	•		•	•				M/883	10%	30	0.1
150	•	•	•	•	•	•	•	C	10%	25	0.1
150	•	•	•	•	•	•		I	10%	30	0.1
150	•		•	•				M	10%	30	0.1
150	•		•	•				M/883	10%	30	0.1
200	•	•	•	•	•	•		C	10%	25	0.1
200	•	•	•	•	•	•		I	10%	30	0.1
200	•		•	•				M	10%	30	0.1
200	•		•	•				M/883	10%	30	0.1
250	•	•	•	•	•			C	10%	25	0.1
250	•	•	•	•	•			I	10%	30	0.1
250	•		•	•				M	10%	30	0.1
250	•		•	•				M/883	10%	30	0.1

AT27CL010

- Not recommended for new designs. Use AT27C010L

Package Type	
D	32DW6, 32 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	32KW, 32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	32P6, 32 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
R	32R, 32 Lead, 0.440" Wide, Plastic Gull Wing Small Outline OTP (SOIC)
T	32T, 32 Lead, Plastic Thin Small Outline Package OTP (TSOP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPROM Product Selection Guide

AT27LV010

see page 4-55

Organization: 128K x 8
No. of Pins: DIP 32, LCC 32

Speed (ns)	Package D	J	K	L	P	R	Temperature Range	Icc (mA)(1) Active	Standby
250	•		•	•			C	8	0.1
250	•			•			I	10	0.1
300	•	•	•	•	•	•	C	8	0.1
300	•			•			I	10	0.1

Note: 1. V_{CC} = 3.3 V

Package Type	
D	32DW6, 32 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	32KW, 32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	32P6, 32 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
R	32R, 32 Lead, 0.450" Wide, Plastic Gull Wing Small Outline OTP (SOIC)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)

AT27C1024

see page 4-63

Organization: 64K x 16
No. of Pins: DIP 40, LCC 44

Speed (ns)	Package D	J	K	L	P	Temperature Range	Power Supply	Icc (mA) Active	Standby
100	•		•	•		C	5%	30	0.1
120	•	•	•	•	•	C	10%	30	0.1
120	•	•	•	•	•	I	10%	40	0.1
120	•		•	•		M	10%	40	0.1
120	•		•	•		M/883	10%	40	0.1
150	•	•	•	•	•	C	10%	30	0.1
150	•	•	•	•	•	I	10%	40	0.1
150	•		•	•		M	10%	40	0.1
150	•		•	•		M/883	10%	40	0.1
200	•	•	•	•	•	C	10%	30	0.1
200	•	•	•	•	•	I	10%	40	0.1
200	•		•	•		M	10%	40	0.1
200	•		•	•		M/883	10%	40	0.1
250	•	•	•	•	•	C	10%	30	0.1
250	•	•	•	•	•	I	10%	40	0.1
250	•		•	•		M	10%	40	0.1
250	•		•	•		M/883	10%	40	0.1
SMD Number for AT27C1024									
5962-86805 06	120	•			•		M/883	10%	40	0.1
5962-86805 05	150	•			•		M/883	10%	40	0.1
5962-86805 04	170	•			•		M/883	10%	40	0.1
5962-86805 03	200	•			•		M/883	10%	40	0.1
5962-86805 02	250	•			•		M/883	10%	40	0.1
5962-86805 01	300	•			•		M/883	10%	40	0.1

Package Type	
D	40DW6, 40 Lead, 0.600" Wide, Windowed Ceramic Dual Inline Package (Cerdip)
J	44J, 44 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	44KW, 44 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	44LW, 44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	40P6, 40 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPROM Product Selection Guide

AT27HC1024

see page 4-71

Organization: 64K x 16 No. of Pins: DIP 40, LCC 44	Speed (ns)	Package D	J	K	L	P	Temperature Range	Power Supply	Icc (mA) Active	Standby
	55	•	•	•	•	•	C	5%	80	8
	70	•	•	•	•	•	C	10%	80	8
	70	•	•	•	•	•	I	10%	90	10
	70	•		•	•		M	10%	90	10
	70	•		•	•		M/883	10%	90	10
	90	•	•	•	•	•	C	10%	80	8
	90	•	•	•	•	•	I	10%	90	10
	90	•		•	•		M	10%	90	10
	90	•		•	•		M/883	10%	90	10
SMD Number for AT27HC1024										
5962-86805 08	70	•			•		M/883	10%	90	10
5962-86805 07	90	•			•		M/883	10%	90	10

Package Type	
D	40DW6, 40 Lead, 0.600" Wide, Windowed Ceramic Dual Inline Package (Cerdip)
J	44J, 44 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	44KW, 44 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	44LW, 44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	40P6, 40 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPROM Product Selection Guide

AT27LV1024

see page 4-79

Organization: 64K x 16
No. of Pins: DIP 40, LCC 44

Speed (ns)	Package D	J	K	L	P	Temperature Range	Icc (mA)[1] Active	Standby
250	•	•	•	•	•	C	8	0.1
250	•		•	•		I	10	0.1
300	•	•	•	•	•	C	8	0.1
300	•		•	•		I	10	0.1

Note: 1. V_{CC} = 3.3 V

Package Type	
D	40DW6, 40 Lead, 0.600" Wide, Windowed Ceramic Dual Inline Package (Cerdip)
J	44J, 44 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	44KW, 44 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	44LW, 44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	40P6, 40 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)

CMOS EPROM Product Selection Guide

AT27C040

see page 4-87

Organization: 512K x 8
No. of Pins: DIP 32, LCC 32, TSOP 40

Speed (ns)	Package D	J	L	P	T	Temperature Range	Power Supply	Icc (mA) Active	Standby
100	•		•			C	5%	25	0.1
120	•	•	•	•	•	C	10%	25	0.1
120	•	•	•	•		I	10%	30	0.1
150	•	•	•	•	•	C	10%	25	0.1
150	•	•	•	•		I	10%	30	0.1
150	•		•			M	10%	30	0.1
150	•		•			M/883	10%	30	0.1
200	•	•	•	•		C	10%	25	0.1
200	•	•	•	•		I	10%	30	0.1
200	•		•			M	10%	30	0.1
200	•		•			M/883	10%	30	0.1

Package Type	
D	32DW6, 32 Lead, 0.600" Wide, Windowed Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
L	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	32P6, 32 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
T	40T, 40 Lead, Plastic Thin Small Outline Package OTP (TSOP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

AT27LV040

see page 4-95

Organization: 512K x 8
No. of Pins: DIP 32, LCC 32, TSOP 40

Speed (ns)	Package D	J	L	P	T	Temperature Range	Icc (mA)[1] Active	Standby
200	•		•			C	8	0.1
200	•		•			I	10	0.1
250	•		•			C	8	0.1
250	•		•			I	10	0.1
300	•	•	•	•	•	C	8	0.1
300	•		•			I	10	0.1

Note: 1. V_{CC} = 3.3 V

	Package Type
D	32DW6, 32 Lead, 0.600" Wide, Windowed Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
L	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	32P6, 32 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
T	40T, 40 Lead, Plastic Thin Small Outline Package OTP (TSOP)
	Temperature Range
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)

CMOS PROM Product Selection Guide

AT28HC191

see page 5-3

Organization: 2K x 8
No. of Pins: DIP 24

Speed (ns)	Package D	Package P	Temperature Range	Power Supply	Icc (mA) Active	Icc (mA) Standby
35	•	•	C	10%	80	60
45	•	•	C	10%	80	60
45	•	•	I	10%	80	60
45	•		M	10%	80	60
45	•		M/883	10%	80	60
55	•	•	C	10%	80	60
55	•	•	I	10%	80	60
55	•		M	10%	80	60
55	•		M/883	10%	80	60

AT28HC191L

see page 5-3

Organization: 2K x 8
No. of Pins: DIP 24

Speed (ns)	Package D	Package P	Temperature Range	Power Supply	Icc (mA) Active	Icc (mA) Standby
45	•	•	C	10%	80	3
45	•	•	I	10%	80	3
45	•		M	10%	80	3
45	•		M/883	10%	80	3
55	•	•	C	10%	80	3
55	•	•	I	10%	80	3
55	•		M	10%	80	3
55	•		M/883	10%	80	3

Package Type	
D	24D6, 24 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
P	24P6, 24 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

AT28HC291

see page 5-11

Organization: 2K x 8
No. of Pins: DIP 24, LCC 28

Speed (ns)	Package D	Package L	Package P	Temperature Range	Power Supply	Icc (mA) Active	Icc (mA) Standby
35	•		•	C	10%	80	60
45	•	•	•	C	10%	80	60
45	•	•	•	I	10%	80	60
45	•	•		M	10%	80	60
45	•	•		M/883	10%	80	60
55	•	•	•	C	10%	80	60
55	•	•	•	I	10%	80	60
55	•	•		M	10%	80	60
55	•	•		M/883	10%	80	60

AT28HC291L

see page 5-11

Organization: 2K x 8
No. of Pins: DIP 24, LCC 28

Speed (ns)	Package D	Package L	Package P	Temperature Range	Power Supply	Icc (mA) Active	Icc (mA) Standby
45	•		•	C	10%	80	3
45	•		•	I	10%	80	3
45	•			M	10%	80	3
45	•			M/883	10%	80	3
55	•	•	•	C	10%	80	3
55	•	•	•	I	10%	80	3
55	•	•		M	10%	80	3
55	•	•		M/883	10%	80	3

Package Type	
D	24D3, 24 Lead, 0.300" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
L	28L, 28 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
P	24P3, 24 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS PROM Product Selection Guide

AT27HC641R

see page 5-19

Organization: 8K x 8
No. of Pins: DIP 24, LCC 28

Speed (ns)	Package D	L	P	Y	Temperature Range	Power Supply	Icc (mA) Active	Standby
35	•	•			C	5%	45	25
45	•	•	•		C	10%	45	25
45	•	•	•		I	10%	50	30
45	•	•			M	10%	50	30
45	•	•			M/883	10%	50	30
55	•	•	•		C	10%	45	25
55	•	•	•		I	10%	50	30
55	•	•			M	10%	50	30
55	•	•			M/883	10%	50	30
70	•	•	•		C	10%	45	25
70	•	•	•		I	10%	50	30
70	•	•			M	10%	50	30
70	•	•			M/883	10%	50	30
90	•	•	•		C	10%	45	25
90	•	•	•		I	10%	50	30
90	•	•			M	10%	50	30
90	•	•			M/883	10%	50	30
SMD Number for AT27HC641R								
5962-87515 01	45	•	•		•	M/883	10%	50	30
5962-87515 02	55	•	•		•	M/883	10%	50	30
5962-87515 03	70	•	•		•	M/883	10%	50	30
5962-87515 04	90	•	•		•	M/883	10%	50	30

Package Type	
D	24DW6, 24 Lead, 0.600" Wide, Windowed Ceramic Dual Inline Package (Cerdip)
L	28LW, 28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	24P6, 24 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
Y	24CW, 24 Lead, Windowed, Ceramic Flat Package (Cerpack)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

AT27HC642R

see page 5-19

Organization: 8K x 8
NO. of Pins: DIP 24

Speed (ns)	Package D	Package P	Temperature Range	Power Supply	Icc (mA) Active	Icc (mA) Standby
35	•		C	5%	45	25
45	•	•	C	10%	45	25
45	•	•	I	10%	50	30
45	•		M	10%	50	30
45	•		M/883	10%	50	30
55	•	•	C	10%	45	25
55	•	•	I	10%	50	30
55	•		M	10%	50	30
55	•		M/883	10%	50	30
70	•	•	C	10%	45	25
70	•	•	I	10%	50	30
70	•		M	10%	50	30
70	•		M/883	10%	50	30
90	•	•	C	10%	45	25
90	•	•	I	10%	50	30
90	•		M	10%	50	30
90	•		M/883	10%	50	30
SMD Number for AT27HC642R						
5962-87515 01	45	•	M/883	10%	50	30
5962-87515 02	55	•	M/883	10%	50	30
5962-87515 03	70	•	M/883	10%	50	30
5962-87515 04	90	•	M/883	10%	50	30

Package Type	
D	24DW3, 24 Lead, 0.300" Wide, Windowed Ceramic Dual Inline Package (Cerdip)
P	24P3, 24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

AT32C16 - Not recommended for new designs. Use AT27C1024

AT3864L

see page 6-3

Organization: 8K x 8
No. of Pins: DIP 28, SOIC 28

Speed (ns)	Package P	Package R	Temperature Range	Icc (mA) Active	Icc (mA) Standby
100	•	•	C	35	0.1
100	•	•	I	35	0.1
120	•	•	C	35	0.1
120	•	•	I	35	0.1
150	•	•	C	35	0.1
150	•	•	I	35	0.1

Package Type	
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
R	28R, 28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline (SOIC)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)

CMOS SRAM Product Selection Guide

AT3864L-15DMB

see page 6-11

Organization: 8K x 8 No. of Pins: DIP 28	Speed (ns)	Package D	Temperature Range	Icc (mA) Active	Icc (mA) Standby
	150	•	M	40	1.0

Package Type	
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Temperature Range	
M	Military (-55°C to 125°C)

AT38H256

see page 6-19

Organization: 32K x 8
No. of Pins: DIP 28, SOIC 28

Speed (ns)	Package N	Package X	Temperature Range	Icc (mA) Active	Icc (mA) Standby
20	•	•	C	100	0.1
20	•	•	I	100	1.0
25	•	•	C	100	0.1
25	•	•	I	100	1.0
35	•	•	C	100	0.1
35	•	•	I	100	1.0

Package Type	
N	28P3, 28 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
X	28S2, 28 Lead, 0.300" Wide, Plastic J-Leaded Small Outline (SOIC)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Idustrial (-40°C to 85°C)

CMOS SRAM Product Selection Guide

AT38LV256

see page 6-27

Organization: 32K x 8 No. of Pins: DIP 28, SOIC 28	Speed (ns)	Package R	Temperature Range	Icc (mA) Active	Icc (mA) Standby
	70	•	C	25	0.03
	120	•	C	25	0.03

Package Type	
R	28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline OTP (SOIC)
Temperature Range	
C	Commercial (0°C to 70°C)

AT18V8Z

see page 7-3

No. of Pins: DIP 20, LCC 20	Speed (ns)	Package D	Package J	Package P	Temperature Range	Power Supply	Icc Active mA (1 MHz)	Icc Standby (µA)
	25	•	•	•	C	5%	2	100
	30	•	•	•	I	10%	2	100
	35	•	•	•	C	5%	2	100
	40	•	•	•	I	10%	2	100

Package Type	
D	20DW3, 20 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
J	20J, 20 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
P	20P3, 20 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)

CMOS EPLD Product Selection Guide

AT22V10

see page 7-19

Approx. Gates: 500 No. of Pins: DIP 24, LCC 28, SOIC 24	Speed (ns)	Package D	F	G	J	K	L	N	P	S	Y	Temperature Range	Power Supply	Icc (mA)
	15	•	•	•	•	•	•	•	•	•	•	C	10%	90
	15	•	•	•	•	•	•	•	•	•	•	I	10%	100
	15	•	•	•		•	•	•			•	M	10%	100
	15	•	•	•		•	•	•			•	M/883	10%	100
	20	•	•	•	•	•	•	•	•	•	•	C	10%	90
	20	•	•	•	•	•	•	•	•	•	•	I	10%	100
	20	•	•	•		•	•	•			•	M	10%	100
	20	•	•	•		•	•	•			•	M/883	10%	100
	25	•	•	•	•	•	•	•	•	•	•	C	10%	55
	25	•	•	•	•	•	•	•	•	•	•	I	10%	55
	25	•	•	•		•	•	•			•	M	10%	55
	25	•	•	•		•	•	•			•	M/883	10%	55
	30	•	•	•		•	•	•			•	M	10%	55
	30	•	•	•		•	•	•			•	M/883	10%	55
	35	•	•	•	•	•	•	•	•	•	•	C	10%	55
	35	•	•	•	•	•	•	•	•	•	•	I	10%	55
SMD Number for AT22V10														
5962-87539 04	20	•					•				•	M/883	10%	100
5962-87539 01	25	•					•				•	M/883	10%	55
5962-87539 02	30	•					•				•	M/883	10%	55
5962-87539 03	40	•					•				•	M/883	10%	55
5962-88670 05	15		•					•				M/883	10%	100
5962-88670 04	20		•	•				•				M/883	10%	100
5962-88670 01	25		•	•				•				M/883	10%	55
5962-88670 02	30		•	•				•				M/883	10%	55
5962-88670 03	40		•	•				•				M/883	10%	55

Package Type	
D	24DW3, 24 Lead, 0.300" Wide, Windowed (OTP) Ceramic Dual Inline Package (Cerdip)
F	24C, 24 Lead, Non-Windowed, Ceramic Flat Package (Cerpack)
G	24D3, 24 Lead, 0.300" Wide, Non-Windowed (OTP) Ceramic Dual Inline Package (Cerdip)
J	28J, 28 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	28KW, 28 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	28LW, 28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
N	28L, 28 Pad, Non-Windowed Ceramic Leadless Chip Carrier OTP (LCC)
P	24P3, 24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
S	24S, 24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
Y	24CW, 24 Lead, Windowed, Ceramic Flat Package (Cerpack)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

AT22V10L

see page 7-19

Approx. Gates: 500 No. of Pins: DIP 24, LCC 28, SOIC 24	Speed (ns)	Package D	F	G	J	K	L	N	P	S	Y	Temperature Range	Power Supply	Icc (mA)
	20	•	•	•	•	•	•	•	•	•	•	C	10%	12
	20	•	•	•	•	•	•	•	•	•	•	I	10%	15
	20	•	•	•		•	•	•			•	M	10%	15
	20	•	•	•		•	•	•			•	M/883	10%	15
	25	•	•	•	•	•	•	•	•	•	•	C	10%	12
	25	•	•	•	•	•	•	•	•	•	•	I	10%	15
	25	•	•	•		•	•	•			•	M	10%	15
	25	•	•	•		•	•	•			•	M/883	10%	15
	30	•	•	•		•	•	•			•	M	10%	15
	30	•	•	•		•	•	•			•	M/883	10%	15
	35	•	•	•	•	•	•	•	•	•	•	C	10%	12
	35	•	•	•	•	•	•	•	•	•	•	I	10%	15
SMD Number for AT22V10L														
5962-89724 04	20	•					•				•	M/883	10%	15
5962-88724 01	25	•					•				•	M/883	10%	15
5962-88724 02	30	•					•				•	M/883	10%	15
5962-88724 03	40	•					•				•	M/883	10%	15
5962-89755 04	20		•	•				•				M/883	10%	15
5962-89755 01	25		•	•				•				M/883	10%	15
5962-89755 02	30		•	•				•				M/883	10%	15
5962-89755 03	40		•	•				•				M/883	10%	15

Package Type	
D	24DW3, 24 Lead, 0.300" Wide, Windowed (OTP) Ceramic Dual Inline Package (Cerdip)
F	24C, 24 Lead, Non-Windowed, Ceramic Flat Package (Cerpack)
G	24D3, 24 Lead, 0.300" Wide, Non-Windowed (OTP) Ceramic Dual Inline Package (Cerdip)
J	28J, 28 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	28KW, 28 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	28LW, 28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
N	28L, 28 Pad, Non-Windowed Ceramic Leadless Chip Carrier OTP (LCC)
P	24P3, 24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
S	24S, 24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
Y	24CW, 24 Lead, Windowed, Ceramic Flat Package (Cerpack)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPLD Product Selection Guide

AT22V10B

see page 7-35

Approx. Gates: 500
No. of Pins: DIP 24, LCC 28, SOIC 24

Speed (ns)	Package D	G	J	K	L	N	P	S	Temperature Range	Power Supply	Icc (mA)
7.5	•	•	•	•	•	•	•	•	C	10%	140
10	•	•	•	•	•	•	•	•	C	10%	140
10	•	•	•	•	•	•	•	•	I	10%	160
10	•	•		•	•	•			M	10%	160
10	•	•		•	•	•			M/883	10%	160
12	•	•	•	•	•	•	•	•	C	10%	140
12	•	•	•	•	•	•	•	•	I	10%	160
12	•	•		•	•	•			M	10%	160
12	•	•		•	•	•			M/883	10%	160

Package Type	
D	24DW3, 24 Lead, 0.300" Wide, Windowed (OTP) Ceramic Dual Inline Package (Cerdip)
G	24D3, 24 Lead, 0.300" Wide, Non-Windowed (OTP) Ceramic Dual Inline Package (Cerdip)
J	28J, 28 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	28KW, 28 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	28LW, 28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
N	28L, 28 Pad, Non-Windowed Ceramic Leadless Chip Carrier OTP (LCC)
P	24P3, 24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
S	24S, 24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

AT22LV10

see page 7-45

Approx. Gates: 500
No. of Pins: DIP 24, LCC 28, SOIC 24

Speed (ns)	Package D	F	G	J	K	L	N	P	S	Y	Temperature Range	Power Supply	I_{CC} (mA) (3.6/5.5 V)
20	•	•	•	•	•	•	•	•	•	•	C	3.0 - 5.5 V	35/90
20	•	•	•	•	•	•	•	•	•	•	I	3.0 - 5.5 V	45/100
20	•	•	•		•	•	•			•	M	3.0 - 5.5 V	45/100
20	•	•	•		•	•	•			•	M/883	3.0 - 5.5 V	45/100
25	•	•	•	•	•	•	•	•	•	•	C	3.0 - 5.5 V	35/90
25	•	•	•	•	•	•	•	•	•	•	I	3.0 - 5.5 V	45/100
25	•	•	•		•	•	•			•	M	3.0 - 5.5 V	45/100
25	•	•	•		•	•	•			•	M/883	3.0 - 5.5 V	45/100
30	•	•	•	•	•	•	•	•	•	•	C	3.0 - 5.5 V	35/90
30	•	•	•	•	•	•	•	•	•	•	I	3.0 - 5.5 V	45/100
30	•	•	•		•	•	•			•	M	3.0 - 5.5 V	45/100
30	•	•	•		•	•	•			•	M/883	3.0 - 5.5 V	45/100

Package Type	
D	24DW3, 24 Lead, 0.300" Wide, Windowed (OTP) Ceramic Dual Inline Package (Cerdip)
F	24C, 24 Lead, Non-Windowed, Ceramic Flat Package (Cerpack)
G	24D3, 24 Lead, 0.300" Wide, Non-Windowed (OTP) Ceramic Dual Inline Package (Cerdip)
J	28J, 28 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	28KW, 28 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	28LW, 28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
N	28L, 28 Pad, Non-Windowed Ceramic Leadless Chip Carrier OTP (LCC)
P	24P3, 24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
S	24S, 24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
Y	24CW, 24 Lead, Windowed, Ceramic Flat Package (Cerpack)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPLD Product Selection Guide

AT22LV10L

see page 7-45

Approx. Gates: 500
No. of Pins: DIP 24, LCC 28, SOIC 24

Speed (ns)	Package D	F	G	J	K	L	N	P	S	Y	Temperature Range	Power Supply	Icc (mA) (3.6/5.5 V)
25	•	•	•	•	•	•	•	•	•	•	C	3.0 - 5.5 V	4/12
25	•	•	•	•	•	•	•	•	•	•	I	3.0 - 5.5 V	5/15
30	•	•	•	•	•	•	•	•	•	•	C	3.0 - 5.5 V	4/12
30	•	•	•	•	•	•	•	•	•	•	I	3.0 - 5.5 V	5/15
30	•	•	•		•	•	•			•	M	3.0 - 5.5 V	5/15
30	•	•	•		•	•	•			•	M/883	3.0 - 5.5 V	5/15
35	•	•	•	•	•	•	•	•	•	•	C	3.0 - 5.5 V	4/12
35	•	•	•	•	•	•	•	•	•	•	I	3.0 - 5.5 V	5/15
35	•	•	•		•	•	•			•	M	3.0 - 5.5 V	5/15
35	•	•	•		•	•	•			•	M/883	3.0 - 5.5 V	5/15

Package Type	
D	24DW3, 24 Lead, 0.300" Wide, Windowed (OTP) Ceramic Dual Inline Package (Cerdip)
F	24C, 24 Lead, Non-Windowed, Ceramic Flat Package (Cerpack)
G	24D3, 24 Lead, 0.300" Wide, Non-Windowed (OTP) Ceramic Dual Inline Package (Cerdip)
J	28J, 28 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	28KW, 28 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	28LW, 28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
N	28L, 28 Pad, Non-Windowed Ceramic Leadless Chip Carrier OTP (LCC)
P	24P3, 24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
S	24S, 24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
Y	24CW, 24 Lead, Windowed, Ceramic Flat Package (Cerpack)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

ATV750

see page 7-59

Approx. Gates: 750
No. of Pins: DIP 24, LCC 28, SOIC 24

Speed (ns)	Package D	F	G	J	K	L	N	P	S	Y	Temperature Range	Power Supply	Icc (mA)
20	•	•	•	•	•	•	•	•	•	•	C	10%	120
20	•	•	•	•	•	•	•	•	•	•	I	10%	140
20	•	•	•		•	•	•			•	M	10%	140
20	•	•	•		•	•	•			•	M/883	10%	140
25	•	•	•	•	•	•	•	•	•	•	C	10%	120
25	•	•	•	•	•	•	•	•	•	•	I	10%	140
25	•	•	•		•	•	•			•	M	10%	140
25	•	•	•		•	•	•			•	M/883	10%	140
30	•	•	•	•	•	•	•	•	•	•	C	10%	120
30	•	•	•	•	•	•	•	•	•	•	I	10%	140
30	•	•	•		•	•	•			•	M	10%	140
30	•	•	•		•	•	•			•	M/883	10%	140
35	•	•	•	•	•	•	•	•	•	•	C	10%	120
35	•	•	•	•	•	•	•	•	•	•	I	10%	140
35	•	•	•		•	•	•			•	M	10%	140
35	•	•	•		•	•	•			•	M/883	10%	140
40	•	•	•	•	•	•	•	•	•	•	I	10%	140
40	•	•	•		•	•	•			•	M	10%	140
40	•	•	•		•	•	•			•	M/883	10%	140

SMD Number for ATV750

5962-88726 04	20	•					•					M/883	10%	140
5962-88726 03	25	•					•					M/883	10%	140
5962-88726 02	35	•					•					M/883	10%	140
5962-88726 01	40	•					•					M/883	10%	140

Package Type	
D	24DW3, 24 Lead, 0.300" Wide, Windowed (OTP) Ceramic Dual Inline Package (Cerdip)
F	24C, 24 Lead, Non-Windowed, Ceramic Flat Package (Cerpack)
G	24D3, 24 Lead, 0.300" Wide, Non-Windowed (OTP) Ceramic Dual Inline Package (Cerdip)
J	28J, 28 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	28KW, 28 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	28LW, 28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
N	28L, 28 Pad, Non-Windowed Ceramic Leadless Chip Carrier OTP (LCC)
P	24P3, 24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
S	24S, 24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
Y	24CW, 24 Lead, Windowed, Ceramic Flat Package (Cerpack)

Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPLD Product Selection Guide

ATV750L

see page 7-59

Approx. Gates: 750
No. of Pins: DIP 24, LCC 28, SOIC 24

Speed (ns)	Package D	F	G	J	K	L	N	P	S	Y	Temperature Range	Power Supply	Icc (mA)
25	•	•	•	•	•	•	•	•	•	•	C	10%	12
25	•	•	•	•	•	•	•	•	•	•	I	10%	15
25	•	•	•		•	•	•			•	M	10%	15
25	•	•	•		•	•	•			•	M/883	10%	15
30	•	•	•	•	•	•	•	•	•	•	C	10%	12
30	•	•	•	•	•	•	•	•	•	•	I	10%	15
30	•	•	•		•	•	•			•	M	10%	15
30	•	•	•		•	•	•			•	M/883	10%	15
SMD Number for ATV750L													
25	•					•					M/883	10%	15
30	•					•					M/883	10%	15

Package Type	
D	24DW3, 24 Lead, 0.300" Wide, Windowed (OTP) Ceramic Dual Inline Package (Cerdip)
F	24C, 24 Lead, Non-Windowed, Ceramic Flat Package (Cerpack)
G	24D3, 24 Lead, 0.300" Wide, Non-Windowed (OTP) Ceramic Dual Inline Package (Cerdip)
J	28J, 28 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	28KW, 28 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	28LW, 28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
N	28L, 28 Pad, Non-Windowed Ceramic Leadless Chip Carrier OTP (LCC)
P	24P3, 24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
S	24S, 24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
Y	24CW, 24 Lead, Windowed, Ceramic Flat Package (Cerpack)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPLD Product Selection Guide

ATV2500H

see page 7-83

Approx. Gates: 2500 No. of Pins: DIP 40, LCC 44	Speed (ns)	Package D	J	K	L	P	Temperature Range	Power Supply	Icc (mA)
	25	•	•	•	•	•	C	10%	160
	25	•	•	•	•	•	I	10%	180
	25	•		•	•		M	10%	180
	25	•		•	•		M/883	10%	180
	30	•	•	•	•	•	C	10%	160
	30	•	•	•	•	•	I	10%	180
	30	•		•	•		M	10%	180
	30	•		•	•		M/883	10%	180
	35	•	•	•	•	•	C	10%	160
	35	•	•	•	•	•	I	10%	180
	35	•		•	•		M	10%	180
	35	•		•	•		M/883	10%	180
SMD Number for ATV2500H									
5962-91545 02 M	25	•		•	•		M/883	10%	180
5962-91545 01 M	35	•		•	•		M/883	10%	180

Package Type	
D	40DW6, 40 Lead, 0.600" Wide, Windowed (OTP) Ceramic Dual Inline Package (Cerdip)
J	44J, 44 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	44KW, 44 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	44LW, 44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	40P6, 40 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPLD Product Selection Guide

ATV2500L

see page 7-83

Approx. Gates: 2500 No. of Pins: DIP 40, LCC 44	Speed (ns)	Package D	J	K	L	P	Temperature Range	Power Supply	Icc (mA)
	30	•	•	•	•	•	C	10%	5
	30	•	•	•	•	•	I	10%	10
	30	•		•	•		M	10%	10
	30	•		•	•		M/883	10%	10
	35	•	•	•	•	•	C	10%	5
	35	•	•	•	•	•	I	10%	10
	35	•		•	•		M	10%	10
	35	•		•	•		M/883	10%	10
	40	•	•	•	•	•	C	10%	5
	40	•	•	•	•	•	I	10%	10
	40	•		•	•		M	10%	10
	40	•		•	•		M/883	10%	10
	45	•	•	•	•	•	I	10%	10
	45	•		•	•		M	10%	10
	45	•		•	•		M/883	10%	10
SMD Number for ATV2500L									
5962-91545 03 M	30	•		•	•		M/883	10%	10

Package Type	
D	40DW6, 40 Lead, 0.600" Wide, Windowed (OTP) Ceramic Dual Inline Package (Cerdip)
J	44J, 44 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	44KW, 44 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	44LW, 44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	40P6, 40 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

ATV5000

see page 7-103

Approx. Gates: 5000
No. of Pins: LCC 68, PGA 68

Speed (ns)	Package J	Package K	Package U	Temperature Range	Power Supply	Icc (mA)
25	•	•	•	C	10%	350
30	•	•	•	C	10%	350
30		•	•	I	10%	400
30		•	•	M	10%	400
30		•	•	M/883	10%	400
35	•	•	•	C	10%	350
35		•	•	I	10%	400
35		•	•	M	10%	400
35		•	•	M/883	10%	400

ATV5000L

see page 7-103

Approx. Gates: 5000
No. of Pins: LCC 68, PGA 68

Speed (ns)	Package J	Package K	Package U	Temperature Range	Power Supply	Icc (mA)
30	•	•	•	C	10%	40
35	•	•	•	C	10%	40
35		•	•	I	10%	50
35		•	•	M	10%	50
35		•	•	M/883	10%	50

Package Type	
J	68J, 68 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	68KW, 68 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
U	68UW, 68 Pin, Windowed, Ceramic Pin Grid Array (PGA)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPLD Product Selection Guide

ATV5100

see page 7-131

Approx. Gates: 5000 No. of Pins: LCC 68, PGA 68	Speed (ns)	Package J	Package K	Package U	Temperature Range	Power Supply	Icc (mA)
	25	•	•	•	C	10%	350
	30	•	•	•	C	10%	350
	30		•	•	I	10%	400
	30		•	•	M	10%	400
	30		•	•	M/883	10%	400
	35	•	•	•	C	10%	350
	35		•	•	I	10%	400
	35		•	•	M	10%	400
	35		•	•	M/883	10%	400

ATV5100L

see page 7-131

Approx. Gates: 5000 No. of Pins: LCC 68, PGA 68	Speed (ns)	Package J	Package K	Package U	Temperature Range	Power Supply	Icc (mA)
	30	•	•	•	C	10%	40
	35	•	•	•	C	10%	40
	35		•	•	I	10%	50
	35		•	•	M	10%	50
	35		•	•	M/883	10%	50

Package Type	
J	68J, 68 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	68KW, 68 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
U	68UW, 68 Pin, Windowed, Ceramic Pin Grid Array (PGA)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPLD Product Selection Guide

ATH3000

see page 7-165

Approx. Gates: 3000
No. of Pins: LCC 68, PGA 68

Speed (ns)	Package J	Package K	Package U	Temperature Range	Power Supply	Icc (mA)	fMAX (MHz)
15	•	•	•	C	10%	225	83.3
15	•	•	•	I	10%	270	83.3
20	•	•	•	C	10%	225	66.7
20	•	•	•	I	10%	270	66.7
20		•	•	M	10%	270	66.7
20		•	•	M/883	10%	270	66.7
25	•	•	•	C	10%	225	50
25	•	•	•	I	10%	270	50
25		•	•	M	10%	270	50
25		•	•	M/883	10%	270	50

ATH3000L

see page 7-165

Approx. Gates: 3000
No. of Pins: LCC 68, PGA 68

Speed (ns)	Package J	Package K	Package U	Temperature Range	Power Supply	Icc (mA)	fMAX (MHz)
20	•	•	•	C	10%	5	66.7
20	•	•	•	I	10%	10	66.7
25	•	•	•	C	10%	5	50
25	•	•	•	I	10%	10	50
25		•	•	M	10%	10	50
25		•	•	M/883	10%	10	50

Package Type	
J	68J, 68 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	68KW, 68 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
U	68UW, 68 Pin, Windowed, Ceramic Pin Grid Array (PGA)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS Logic Product Selection Guide

AT40391B Order as a chip set with the AT40392 in the same speed. see page 9-3

No. of Pins: PQFP 160	CPU Clock (MHz)	Package Q	Temperature Range	Power Supply
	25	•	C	5%
	33	•	C	5%
	40	•	C	5%

Package Type	
Q	160Q, 160 Lead, Plastic Gull Wing Quad Flat Package (PQFP)
Temperature Range	
C	Commercial (0°C to 70°C)

AT40392 To be ordered as a chip set with the AT40391B, AT40493 or the AT40495. see pages 9-3, 9-9, 9-15

No. of Pins: PQFP 160	CPU Clock (MHz)	Package Q	Temperature Range	Power Supply
	25	•	C	5%
	33	•	C	5%
	40	•	C	5%
	50	•	C	5%

Package Type	
Q	160Q, 160 Lead, Plastic Gull Wing Quad Flat Package (PQFP)
Temperature Range	
C	Commercial (0°C to 70°C)

CMOS Logic Product Selection Guide

AT40493 Order as a chip set with the AT40392 in the same speed. see page 9-9

No. of Pins: PQFP 160	CPU Clock (MHz)	Package Q	Temperature Range	Power Supply
	25	•	C	5%
	33	•	C	5%
	50	•	C	5%

Package Type	
Q	160Q, 160 Lead, Plastic Gull Wing Quad Flat Package (PQFP)
Temperature Range	
C	Commercial (0°C to 70°C)

AT40495 Order as a chip set with the AT40392 in the same speed. see page 9-15

No. of Pins: PQFP 160	CPU Clock (MHz)	Package Q	Temperature Range	Power Supply
	25	•	C	5%
	33	•	C	5%
	50	•	C	5%

Package Type	
Q	160Q, 160 Lead, Plastic Gull Wing Quad Flat Package (PQFP)
Temperature Range	
C	Commercial (0°C to 70°C)

CMOS Logic Product Selection Guide

AT40498				see page 9-17
No. of Pins: PQFP 208	CPU Clock (MHz)	Package Q	Temperature Range	Power Supply
	25	•	C	5%
	33	•	C	5%
	50	•	C	5%

Package Type	
Q	208Q, 208 Lead, Plastic Gull Wing Quad Flat Package (PQFP)
Temperature Range	
C	Commercial (0°C to 70°C)

AT40281

see page 9-21

No. of Pins: PQFP 160	CPU Clock (MHz)	Package Q	Temperature Range	Power Supply
	16	•	C	5%
	20	•	C	5%
	25	•	C	5%
	33	•	C	5%
	40	•	C	5%

Package Type	
Q	160Q, 160 Lead, Plastic Gull Wing Quad Flat Package (PQFP)
Temperature Range	
C	Commercial (0°C to 70°C)

CMOS Logic Product Selection Guide

AT40283				see page 9-25
No. of Pins: PQFP 160	CPU Clock (MHz)	Package Q	Temperature Range	Power Supply
	16	•	C	5%
	20	•	C	5%
	25	•	C	5%
	33	•	C	5%

Package Type	
Q	160Q, 160 Lead, Plastic Gull Wing Quad Flat Package (PQFP)
Temperature Range	
C	Commercial (0°C to 70°C)

AT40206

see page 9-29

No. of Pins: PQFP 100, PLCC 84	CPU Clock (MHz)	Package J	Package Q	Temperature Range	Power Supply
	8	•	•	C	5%

Package Type	
J	84J, 84 Lead, Plastic J-Leaded Chip Carrier (PLCC)
Q	100Q2, 100 Lead, Plastic Gull Wing Quad Flat Package (PQFP)
Temperature Range	
C	Commercial (0°C to 70°C)

CMOS Logic Product Selection Guide

AT43216				see page 9-33
No. of Pins: PLCC 84	CPU Clock (MHz)	Package J	Temperature Range	Power Supply
	40	•	C	10%

Package Type	
J	84J, 84 Lead, Plastic J-Leaded Chip Carrier (PLCC)
Temperature Range	
C	Commercial (0°C to 70°C)

AT40957 Order as a chip set with the AT40958 and the AT40959 in the same speed. see page 9-37

No. of Pins: PQFP 184	CPU Clock (MHz)	Package Q2	Temperature Range	Power Supply
	33	•	C	5%
	50	•	C	5%
	66	•	C	5%

AT40958 Order as a chip set with the AT40957 and the AT40959 in the same speed. see page 9-37

No. of Pins: PQFP 184	CPU Clock (MHz)	Package Q2	Temperature Range	Power Supply
	33	•	C	5%
	50	•	C	5%
	66	•	C	5%

AT40959 Order as a chip set with the AT40957 and the AT40958 in the same speed. see page 9-37

No. of Pins: PQFP 160	CPU Clock (MHz)	Package Q1	Temperature Range	Power Supply
	33	•	C	5%
	50	•	C	5%
	66	•	C	5%

Package Type	
Q1	160Q, 160 Lead, Plastic Gull Wing Quad Flat Package (PQFP)
Q2	184Q, 184 Lead, Plastic Gull Wing Quad Flat Package (PQFP)
Temperature Range	
C	Commercial (0°C to 70°C)

CMOS Mixed Signal Product Selection Guide

AT76C10

see page 11-3

Delay (ms): 1.8
Gain (dB): 31.5
No. of Pins: DIP 16, SOIC 16

Bandwidth (kHz)	Package D	Package P	Package S	Temperature Range	Power Supply
4		•	•	C	10%
4		•	•	I	10%
4	•			M	5%

AT76C10E

see page 11-11

Delay (ms): 1.8
Gain (dB): 31.5
No. of Pins: DIP 16, SOIC 16

Bandwidth (kHz)	Package D	Package P	Package S	Temperature Range	Power Supply
4		•	•	C	10%
4		•	•	I	10%
4	•			M	5%

Package Type	
D	16D3, 16 Lead, 0.300" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
P	16P3, 16 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
S	16S, 16 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)

AT76C120

see page 11-19

Organization: Dual 16/18-bit A/D
No. of Pins: DIP 24, SOIC 24

Speed (kHz)	Signal-to-Noise (dB)	Accuracy (%FRS)	Package D	Package P	Package R	Temperature Range	Power Supply
96	90	±0.006		•		C	10%
96	90	±0.006		•		I	10%
96	90	±0.006	•			M	5%
96	84	±0.01		•	•	C	10%
96	84	±0.01		•	•	I	10%
96	84	±0.01	•			M	5%

Package Type	
D	24D6, 24 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
P	24P6, 24 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
R	24R, 24 Lead, 0.330" Wide, Plastic Gull Wing Small Outline (SOIC)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)

CMOS Mixed Signal Product Selection Guide

AD-120

see page 11-27

Organization:	Speed (kHz)	Signal-to-Noise (dB)	Accuracy (%FRS)	Temperature Range	Power Supply
Dual 16/18-bit A/D Development Kit for PC/AT Board, S.W. & Cables	96	84	± 0.1	C	10%

AT76C176

see page 11-31

Organization: D/A: Triple 6-bit RAM: 256 x 18 No. of Pins: DIP 28, LCC 32	Speed (MHz)	Package D	Package L	Package P	Temperature Range	Power Supply
	40			•	C	10%
	40			•	I	10%
	40	•	•		M	5%
	50			•	C	10%
	50			•	I	10%
	66			•	C	5%

Package Type	
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
L	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)

CMOS Mixed Signal Product Selection Guide

AT76C176A

see page 11-43

Organization:
D/A: Triple 6-bit
RAM: 256 x 18
No. of Pins: DIP 28,
LCC 32, 44

Speed (MHz)	Package D	Package J1	Package J2	Package L	Package P	Temperature Range	Power Supply
50		•	•		•	C	10%
50		•	•		•	I	10%
50	•			•		M	5%
66		•	•		•	C	10%
66		•	•		•	I	10%
66	•			•		M	5%
80		•	•		•	C	10%
80		•	•		•	I	10%
110		•	•		•	C	5%
135		•	•		•	C	5%

Package Type	
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
J1	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
J2	44J, 44 Lead, Plastic J-Leaded Chip Carrier (PLCC)
L	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)

		Speed (MHz)	Package					Temperature Range	Power Supply
			D	J1	J2	L	P		
		50		•			•	C	10%
		50		•			•	I	10%
		50	•			•		M	5%
		66		•			•	C	10%
		66		•			•	I	10%
		66	•			•		M	5%
		80		•			•	C	10%
		80		•			•	I	10%
		110		•			•	C	5%
		135		•			•	C	5%

	Package Types
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
J1	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
J2	44J, 44 Lead, Plastic J-Leaded Chip Carrier (PLCC)
L	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
	Temperature Range
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)

Explanation of Atmel's Part Number Code

All Atmel part numbers begin with the prefix "AT." The next four to nine digits are the part number. In addition, Atmel parts can be ordered in particular speeds, in specific packages, for particular temperature ranges and with the option of 883C level B military compliance. The available options for each part are listed at the back of its data sheet in its "Ordering Information" table. These options are designated by the following suffixes placed at the end of the Atmel part number, in the order given:

Prefix	Device -	Suffix			
AT	XXXXX	X	X	X	X

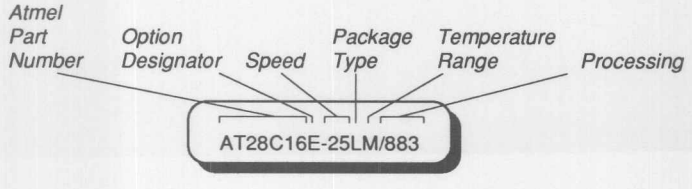
Processing
- Blank = Standard
- /883 = MIL-STD-883, Class B Fully Compliant
- B = MIL-STD-883, Class B Non-Compliant

Temperature Range
- C = Com Temp (0°C to 70°C)
- I = Ind Temp (-40°C to 85°C)
- M = Mil Temp (-55°C to 125°C)

Package
- B = Ceramic Side Braze Dual Inline
- C = Cerpack
- D = Cerdip
- F = Flatpack
- G = Cerdip, One Time Programmable
- J = Plastic J-Lead Chip Carrier
- K = Ceramic J-Lead Chip Carrier
- L = Leadless Chip Carrier
- M = Ceramic Module
- N = Leadless Chip Carrier, One Time Programmable
- P = Plastic DIP
- Q = Plastic Quad Flatpack
- R = SOIC
- S = SOIC
- T = TSOP
- U = PGA
- V = TAB
- W = Die
- Y = Cerpack
- Z = Ceramic Multi-Chip Module

Speed

Here is an example Atmel part number:





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AT93C66	256 x 16 / 512 x 8	3-Wire, 4K Serial E^2PROM	2-37
AT59C11	64 x 16 / 128 x 8	4-Wire, 1K Serial E^2PROM	2-51
AT59C22	128 x 16 / 256 x 8	4-Wire, 2K Serial E^2PROM	2-51
AT59C13	256 x 16 / 512 x 8	4-Wire, 4K Serial E^2PROM	2-51

Parallel E^2PROMs

AT28C04	512 x 8	4K E^2PROM	2-63
AT28C16	2K x 8	16K E^2PROM	2-71
AT28C17	2K x 8	16K E^2PROM	2-81
AT28C64	8K x 8	64K E^2PROM	2-91
AT28C64X	8K x 8	64K E^2PROM without Ready-$\overline{\text{Busy}}$	2-91
AT28HC64/L	8K x 8	High Speed, 64K Paged E^2PROM	2-103
AT28LV64	8K x 8	3-Volt, 64K E^2PROM	2-115
AT28C64B	8K x 8	64K E^2PROM with S/W Data Protection	2-123
AT28PC64	8K x 8	64K E^2PROM with Page Mode Write	2-135
AT28C256	32K x 8	256K E^2PROM	2-147
AT28HC256/L	32K x 8	High Speed, 256K Paged E^2PROM	2-159
AT28C1024	64K x 16	1-Mbit E^2PROM	2-173
AT28C010	128K x 8	1-Mbit E^2PROM with 128-Byte Page	2-183
AT28MC020	256K x 8	2-Mbit Paged Module E^2PROM	2-195
AT28MC040	512K x 8	4-Mbit Paged Module E^2PROM	2-205

E^2PROM Application Notes

Using Atmel's CMOS E^2PROMs 2-215

E^2PROM Data Protection 2-219

Section 2

CMOS E²PROMs

Serial E²PROMs

AT24C01	128 x 8	2-Wire, 1K Serial E²PROM 2-3
AT24C01A	128 x 8	2-Wire, 1K Serial E²PROM 2-13
AT24C02	256 x 8	2-Wire, 2K Serial E²PROM 2-13
AT24C04	512 x 8	2-Wire, 4K Serial E²PROM 2-13
AT24C08	1024 x 8	2-Wire, 8K Serial E²PROM 2-13
AT24C16	2048 x 8	2-Wire, 16K Serial E²PROM 2-13
AT24C164	2048 x 8	2-Wire, 16K Serial E²PROM 2-27
AT93C46	64 x 16 / 128 x 8	3-Wire, 1K Serial E²PROM 2-37
AT93C56	128 x 16 / 256 x 8	3-Wire, 2K Serial E²PROM 2-37
AT93C57	128 x 16 / 256 x 8	3-Wire, 2K Serial E²PROM 2-37
AT93C66	256 x 16 / 512 x 8	3-Wire, 4K Serial E²PROM 2-37
AT59C11	64 x 16 / 128 x 8	4-Wire, 1K Serial E²PROM 2-51
AT59C22	128 x 16 / 256 x 8	4-Wire, 2K Serial E²PROM 2-51
AT59C13	256 x 16 / 512 x 8	4-Wire, 4K Serial E²PROM 2-51

Parallel E²PROMs

AT28C64	512 x 8	4K E²PROM 2-63
AT28C16	2K x 8	16K E²PROM 2-71
AT28C17	2K x 8	16K E²PROM 2-81
AT28C64	8K x 8	64K E²PROM 2-91
AT28C64X	8K x 8	64K E²PROM without Ready-$\overline{\text{Busy}}$ 2-91
AT28HC64L	8K x 8	High Speed, 64K Paged E²PROM 2-103
AT28LV64	8K x 8	3-Volt, 64K E²PROM 2-115
AT28C64B	8K x 8	64K E²PROM with S/W Data Protection ... 2-123
AT28PC64	8K x 8	64K E²PROM with Page Mode Write 2-135
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AT28HC256L	32K x 8	High Speed, 256K Paged E²PROM 2-159
AT28C1024	64K x 16	1-Mbit E²PROM 2-173
AT28C010	128K x 8	1-Mbit E²PROM with 128-Byte Page 2-183
AT28MC020	256K x 8	2-Mbit Paged Module E²PROM 2-195
AT28MC040	512K x 8	4-Mbit Paged Module E²PROM 2-205

E²PROM Application Notes

Using Atmel's CMOS E²PROMs 2-215

E²PROM Data Protection 2-219

Features

- **Low Voltage and Standard Voltage Operation**
  - **5.0 (V_{CC} = 4.5 V to 6.0 V)**
  - **3.0 (V_{CC} = 2.7 V to 6.0 V)**
  - **2.5 (V_{CC} = 2.5 V to 6.0 V)**
  - **2.0 (V_{CC} = 1.8 V to 6.0 V)**
- **Internally Organized 128 x 8**
- **Two-wire Serial Interface**
- **Bidirectional Data Transfer Protocol**
- **Four-byte Page Write Mode**
- **Self-timed Write Cycle (10 ms max)**
- **High Reliability**
  - **Endurance: 100,000 Cycles**
  - **Data Retention: 100 Years**
- **Eight-pin PDIP and JEDEC SOIC Packages**

2-Wire Serial CMOS E²PROM

1K (128 x 8)

Description

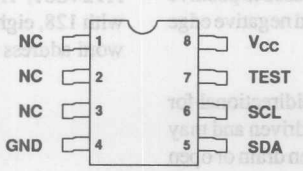
The AT24C01 provides 1024 bits of serial EEPROM (Electrically Erasable and Programmable Read Only Memory) organized as 128 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT24C01 is available in space saving eight-pin PDIP and eight-pin SOIC packages and is accessed via a two-wire serial interface. Atmel's EEPROMs are designed and tested for applications requiring extended endurance. The AT24C01 is guaranteed for 100,000 erase/write cycles and 100 year data retention. In addition, the entire family is available in 5.0 V (4.5 V to 6.0 V), 3.0 V (2.7 V to 6.0 V), 2.5 V (2.5 V to 6.0 V) and 2.0 V (1.8 V to 6.0 V) versions.

Pin Configurations

Pin Name	Function
NC	No Connect
SDA	Serial Data
SCL	Serial Clock
Test	**Test Input (GND or V_{CC})**



8-pin PDIP



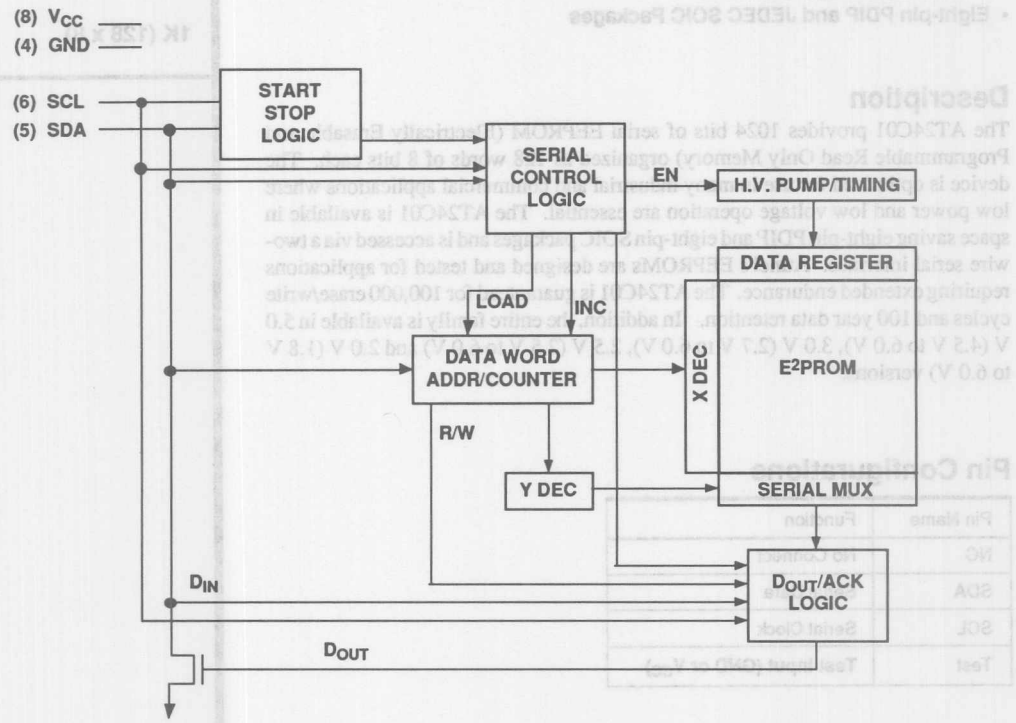
8-pin SOIC

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0 V to +7.0 V
Maximum Operating Voltage	6.6 V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into the E²PROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open drain or open collector devices.

Memory Page Organization

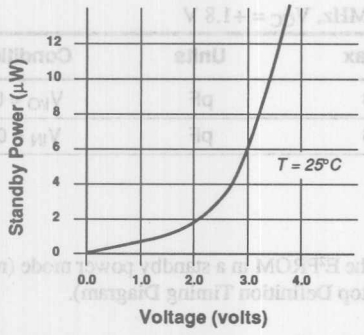
AT24C01, 1K SERIAL E²PROM: Internally organized with 128, eight-bit words, the 1K requires a seven-bit data word address for random word addressing.

DC Characteristics

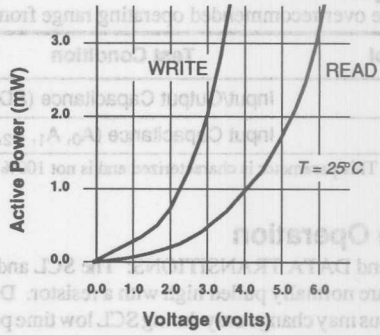
Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +1.8 V to +6.0 V, T_{AC} = 0°C to +70°C, V_{CC} = +1.8 V to +6.0 V (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC1}[1]	Supply Voltage		1.8	5.0	6.0	V
V_{CC2}	Supply Voltage		2.5	5.0	6.0	V
V_{CC3}	Supply Voltage		2.7	5.0	6.0	V
V_{CC4}	Supply Voltage		4.5	5.0	5.5	V
I_{CC}	Supply Current V_{CC} = 5.0 V	READ at 100 KHz		0.4	1.0	mA
I_{CC}	Supply Current V_{CC} = 5.0 V	WRITE at 100 KHz		2.0	3.0	mA
I_{SB1}[1]	Standby Current V_{CC} = 1.8 V	V_{IN} = V_{CC} or V_{SS}		0.6	3.0	µA
I_{SB2}	Standby Current V_{CC} = 2.5 V	V_{IN} = V_{CC} or V_{SS}		1.4	4.0	µA
I_{SB3}	Standby Current V_{CC} = 2.7 V	V_{IN} = V_{CC} or V_{SS}		1.6	4.0	µA
I_{SB4}	Standby Current V_{CC} = 5.0 V	V_{IN} = V_{CC} or V_{SS}		8.0	18.0	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}		0.10	3.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}		0.05	3.0	µA
V_{IL}	Input Low Level[2]		-1.0		V_{CC} x 0.3	V
V_{IH}	Input High Level[2]		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL2}	Output Low Level V_{CC} = 3.0 V	I_{OL} = 2.1 mA			0.40	V
V_{OL1}	Output Low Level V_{CC} = 1.8 V	I_{OL} = 1.5 mA			0.50	V

Typical[3] Standby Power vs. Voltage



Typical[3] Active Power vs. Voltage



Notes: 1. This parameter is preliminary and Atmel may change the specifications upon further characterization.
2. V_{IL} min and V_{IH} max are reference only and are not tested.
3. These graphs are for reference only and are not guaranteed by test.

AC Characteristics

Applicable over recommended operating range from T_A = -40°C to +85°C, V_{CC} = +1.8 V to +6.0 V CL = 1 TTL Gate and 100 pF (unless otherwise noted)

Symbol	Parameter	Min	Typ	Max	Units
f_{SCL}	Clock Frequency, SCL	0		100	kHz
t_{LOW}	Clock Pulse Width Low	4.7			µs
t_{HIGH}	Clock Pulse Width High	4.0			µs
t_I	Noise Suppression Time(2)		60	100	ns
t_{AA}	Clock Low to Data Out Valid	0.1		3.5	µs
t_{BUF}	Time the bus must be free before a new transmission can start	4.7			µs
$t_{HD.STA}$	Start Hold Time	4.0			µs
$t_{SU.STA}$	Start Set-up Time	4.7			µs
$t_{HD.DAT}$	Data In Hold Time	0.0			µs
$t_{SU.DAT}$	Data In Set-up Time	50			ns
t_R	Inputs Rise Time(2)			1.0	µs
t_F	Inputs Fall Time(2)			300	ns
$t_{SU.STO}$	Stop Set-up Time	4.7			µs
t_{DH}	Data Out Hold Time	100	180		ns
t_{WR}	Write Cycle Time		5	10	ms

Pin Capacitance(2)

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +1.8 V

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0 V
C_{IN}	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0 V

Note: 2. This parameter is characterized and is not 100% tested.

Device Operation

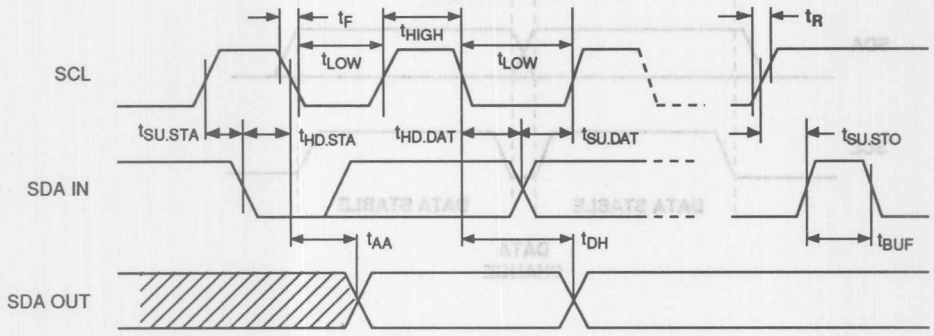
CLOCK and DATA TRANSITIONS: The SCL and SDA bus lines are normally pulled high with a resistor. Data on the SDA bus may change only during SCL low time periods (refer to Data Validity Timing diagram). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Start and Stop Definition Timing diagram).

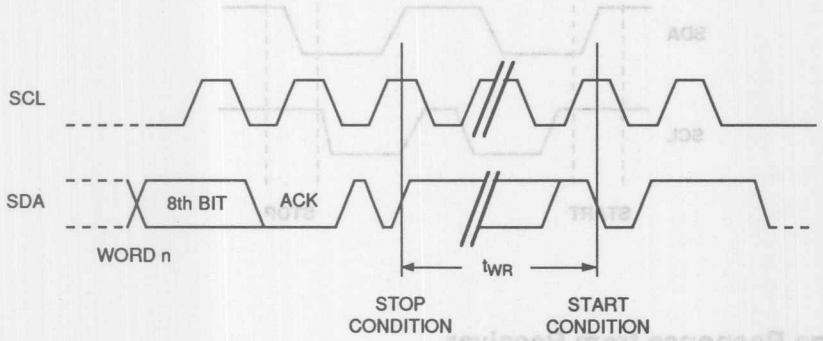
STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition which terminates all communications. After a read sequence, the stop command will place the E²PROM in a standby power mode (refer to Start and Stop Definition Timing Diagram).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the E²PROM in eight-bit words. Any device on the system bus receiving data (when communicating with the E²PROM) must pull the SDA bus low to acknowledge that it has successfully received each word. This must happen during the ninth clock cycle after each word received and after all other system devices have freed the SDA bus. The E²PROM will likewise acknowledge by pulling SDA low after receiving each address or data word (refer to Acknowledge Response from Receiver Timing diagram).

Bus Timing SCL: Serial Clock SDA: Serial Data I/O

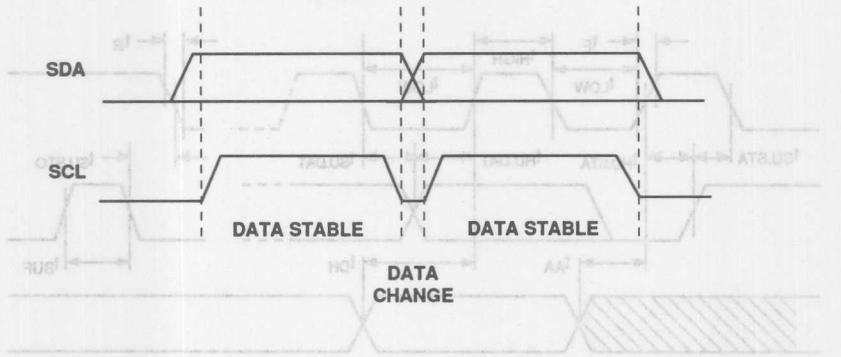


Write Cycle Timing SCL: Serial Clock SDA: Serial Data I/O

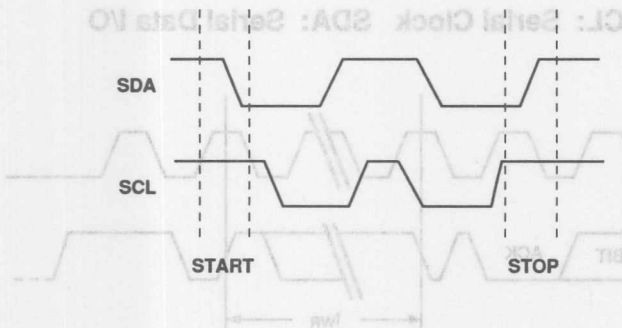


Note: The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

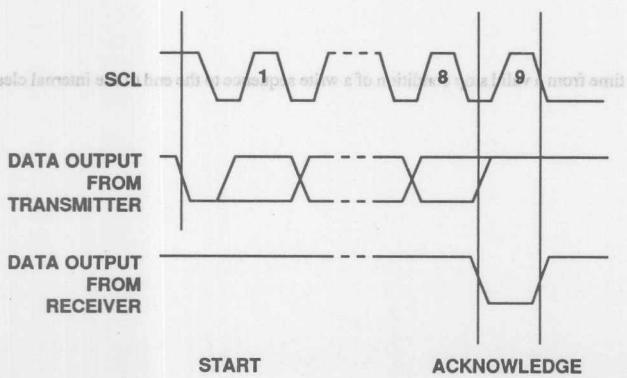
Data Validity



Start and Stop Definition



Acknowledge Response from Receiver



Write Operations

BYTE WRITE: Following a start condition, a write operation requires a seven-bit data word address and a low write bit. Upon receipt of this address, the E²PROM will again respond with an acknowledge on SDA and then clock in the first eight-bit data word. Following receipt of the eight-bit data word, the E²PROM will acknowledge SDA and the data transmitting device must terminate the write sequence with a stop condition. At this time the E²PROM enters an internally-timed write cycle to the nonvolatile memory. All inputs are disabled during this write cycle and the E²PROM will not respond for communication until the write is complete (refer to Figure 1).

PAGE WRITE: The AT24C01 is capable of a four-byte page write.

A page write is initiated the same as a byte write but the data transmitting device does not send a stop condition after the first data word is clocked in. Instead, after the E²PROM acknowledges receipt of the first data word, the data transmitting device can transmit up to three more data words. The E²PROM will respond with an acknowledge on SDA after each data word received. The transmitting device must terminate the page write sequence with a stop condition (refer to Figure 2).

The data word address lower two bits are internally incremented following the receipt of each data word. The higher five data word address bits are not incremented retaining the memory page row location. If more than four data words are transmitted to the E²PROM, the data word address will "roll over" and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally-timed write cycle has started and the E²PROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the E²PROM respond with an acknowledge on the SDA bus allowing the read or write sequence to continue.

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are two read operations: byte read and sequential read.

BYTE READ: A byte read is initiated with a start condition followed by a seven-bit data word address and a high read bit. The AT24C01 will respond with an acknowledge and then serially transmit eight data bits to the SDA bus. The device reading the data does not respond with an acknowledge (leaving the SDA bus high) but does generate a following stop condition (refer to Figure 3).

SEQUENTIAL READ: Sequential reads are initiated the same as a byte read. After the device reading the data receives an eight-bit data word, it responds with an acknowledge. As long as the E²PROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the device reading the data does not respond with an acknowledge (leaving the SDA bus high) but does generate a following stop condition (refer to Figure 4).

Figure 1. Byte Write

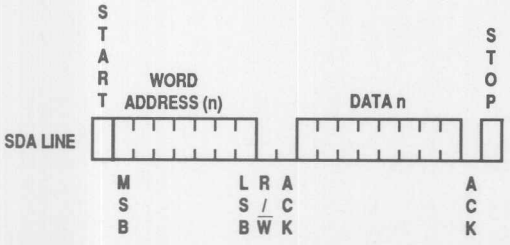


Figure 2. Page Write

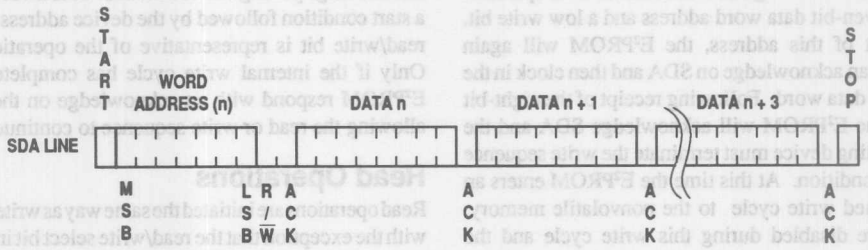


Figure 3. Byte Read

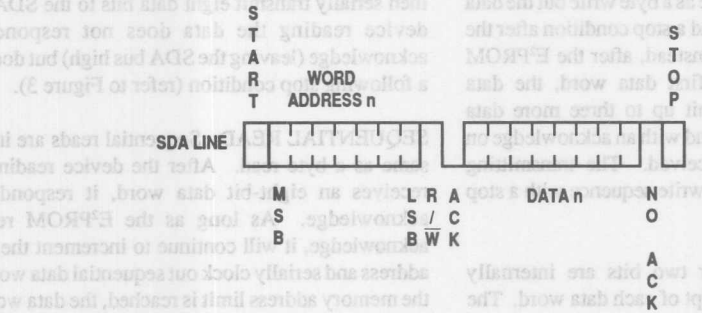
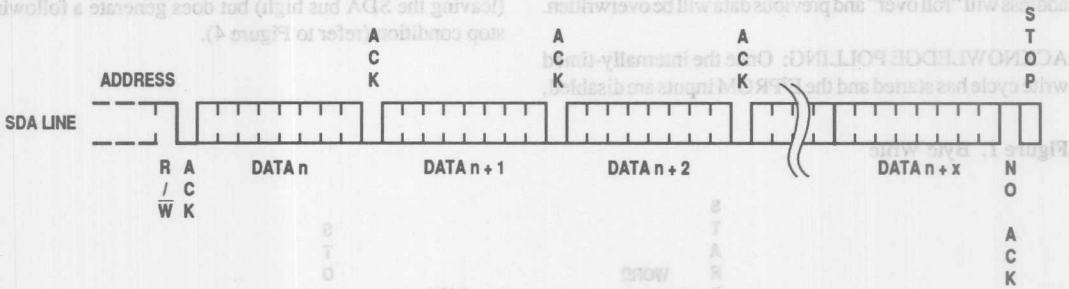


Figure 4. Sequential Read



Ordering Information

t_{WR} (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	18	100	AT24C01-10PC AT24C01-10SC	8P3 8S1	Commercial (0°C to +70°C)
				AT24C01-10PI AT24C01-10SI	8P3 8S1	Industrial (-40°C to +85°C)
10	1500	4	100	AT24C01-10PC-2.7 AT24C01-10SC-2.7	8P3 8S1	Commercial (0°C to +70°C)
				AT24C01-10PI-2.7 AT24C01-10SI-2.7	8P3 8S1	Industrial (-40°C to +85°C)
10	1000	4	100	AT24C01-10PC-2.5 AT24C01-10SC-2.5	8P3 8S1	Commercial (0°C to +70°C)
				AT24C01-10PI-2.5 AT24C01-10SI-2.5	8P3 8S1	Industrial (-40°C to +85°C)
10	800	3	100	AT24C01-10PC-1.8 AT24C01-10SC-1.8	8P3 8S1	Commercial (0°C to +70°C)
				AT24C01-10PI-1.8 AT24C01-10SI-1.8	8P3 8S1	Industrial (-40°C to +85°C)

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
Options	
Blank	Standard Operation (4.5 V to 6.0 V)
-2.7	Low Voltage (2.7 V to 6.0 V)
-2.5	Low Voltage (2.5 V to 6.0 V)
-1.8	Low Voltage (1.8 V to 6.0 V)

t_{WR} (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	I_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	18	100	AT24C01-10PC AT24C01-10SC	8P3 8S1	Commercial (0°C to +70°C)
				AT24C01-10PI AT24C01-10SI	8P3 8S1	Industrial (-40°C to +85°C)
10	1500	4	100	AT24C01-10PC-2.7 AT24C01-10SC-2.7	8P3 8S1	Commercial (0°C to +70°C)
				AT24C01-10PI-2.7 AT24C01-10SI-2.7	8P3 8S1	Industrial (-40°C to +85°C)
10	1000	4	100	AT24C01-10PC-2.5 AT24C01-10SC-2.5	8P3 8S1	Commercial (0°C to +70°C)
				AT24C01-10PI-2.5 AT24C01-10SI-2.5	8P3 8S1	Industrial (-40°C to +85°C)
10	800	3	100	AT24C01-10PC-1.8 AT24C01-10SC-1.8	8P3 8S1	Commercial (0°C to +70°C)
				AT24C01-10PI-1.8 AT24C01-10SI-1.8	8P3 8S1	Industrial (-40°C to +85°C)

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
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-1.8	Low Voltage (1.8 V to 6.0 V)

2-Wire Serial CMOS E²PROMs

1K (128 x 8)
2K (256 x 8)
4K (512 x 8)
8K (1024 x 8)
16K (2048 x 8)

Features

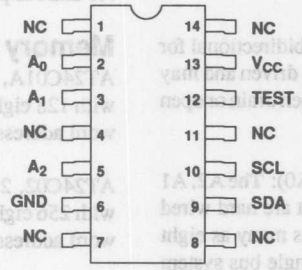
- Low Voltage and Standard Voltage Operation
  - 5.0 (V_{CC} = 4.5 V to 6.0 V)
  - 3.0 (V_{CC} = 2.7 V to 6.0 V)
  - 2.5 (V_{CC} = 2.5 V to 6.0 V)
  - 2.0 (V_{CC} = 1.8 V to 6.0 V)
- Internally Organized 128 x 8 (1K), 256 x 8 (2K), 512 x 8 (4K), 1024 x 8 (8K) or 2048 x 8 (16K)
- Two-wire Serial Interface
- Bidirectional Data Transfer Protocol
- Eight-byte Page (1K, 2K), 16-byte Page (4K, 8K, 16K) Write Modes
- Partial Page Writes Are Allowed
- Self-timed Write Cycle (10 ms max)
- High Reliability
  - Endurance: 100,000 Cycles
  - Data Retention: 100 Years
- Eight and Fourteen-pin JEDEC SOIC and Eight-pin PDIP Packages

Description

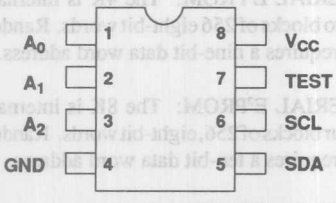
The AT24C01A/02/04/08/16 provides 1024/2048/4096/8192/16384 bits of serial EEPROM (Electrically Erasable and Programmable Read Only Memory) organized as 128/256/512/1024/2048 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT24C01A/02/04/08/16 is available in space saving eight-pin PDIP, eight-pin and fourteen-pin SOIC packages and is accessed via a two-wire serial interface. Atmel's EEPROMs are designed and tested for applications requiring extended endurance. The AT24C01A/02/04/08/16 is guaranteed for 100,000 erase/write cycles and 100 year data retention. In addition, the entire family is available in 5.0 V (4.5 V to 6.0 V), 3.0 V (2.7 V to 6.0 V), 2.5 V (2.5 V to 6.0 V) and 2.0 V (1.8 V to 6.0 V) versions.

Pin Configurations

Pin Name	Function
A_0 to A_2	Address Inputs
SDA	Serial Data
SCL	Serial Clock
Test	Test Input (GND or V_{CC})
NC	No Connect



14-pin SOIC

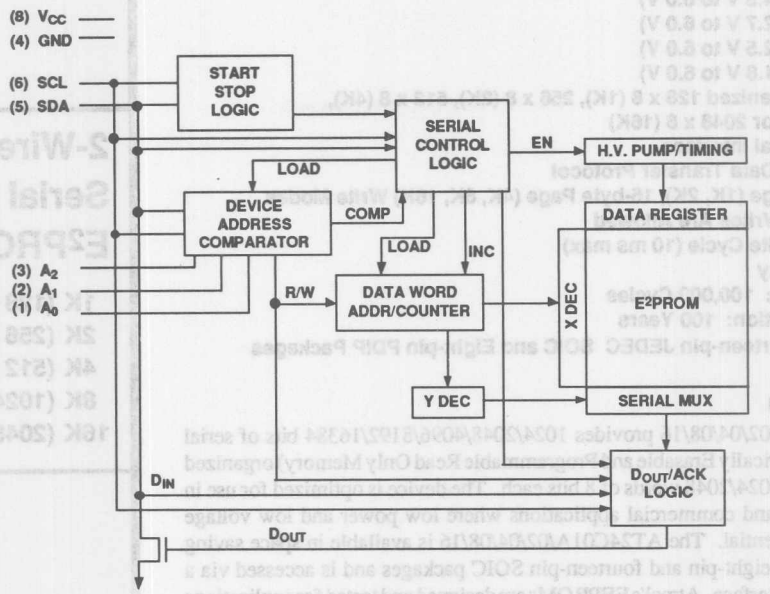


8-pin PDIP



8-pin SOIC

Block Diagram



Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each E²PROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open drain or open collector devices.

DEVICE/PAGE ADDRESSES (A2, A1, A0): The A2, A1 and A0 pins are device address inputs that are hard wired for the AT24C01A and the AT24C02. As many as eight 1K/2K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section).

The AT24C04 uses the A2 and A1 inputs for hard wire addressing and a total of four 4K devices may be addressed on a single bus system. The A0 pin is a no connect.

The AT24C08 only uses the A2 input for hardwire addressing and a total of two 8K devices may be addressed on a single bus system. The A0 and A1 pins are no connects.

The AT24C16 does not use the device address pins which limits the number of devices on a single bus to one. The A0, A1 and A2 pins are no connects.

Memory Organization

AT24C01A, 1K SERIAL E²PROM: Internally organized with 128 eight-bit words, the 1K requires a seven-bit data word address for random word addressing.

AT24C02, 2K SERIAL E²PROM: Internally organized with 256 eight-bit words, the 2K requires an eight-bit data word address for random word addressing.

AT24C04, 4K SERIAL E²PROM: The 4K is internally organized with two blocks of 256 eight-bit words. Random word addressing requires a nine-bit data word address.

AT24C08, 8K SERIAL E²PROM: The 8K is internally organized with four blocks of 256, eight-bit words. Random word addressing requires a ten-bit data word address.

AT24C16, 16K SERIAL E²PROM: The 16K is internally organized with eight blocks of 256, eight-bit words. Random word addressing requires an eleven-bit data word address.

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0 V to +7.0 V
Maximum Operating Voltage	6.6 V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

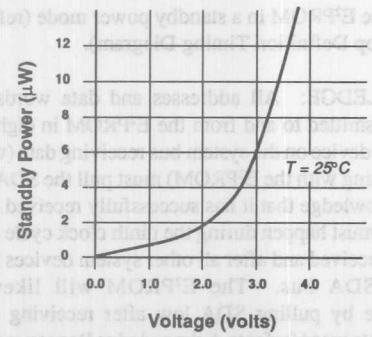
2

DC Characteristics

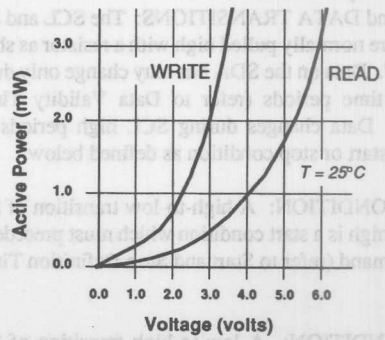
Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +1.8 V to +6.0 V, T_{AC} = 0°C to +70°C, V_{CC} = +1.8 V to +6.0 V (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC1}(1)	Supply Voltage		1.8	5.0	6.0	V
V_{CC2}	Supply Voltage		2.5	5.0	6.0	V
V_{CC3}	Supply Voltage		2.7	5.0	6.0	V
V_{CC4}	Supply Voltage		4.5	5.0	5.5	V
I_{CC}	Supply Current V_{CC} = 5.0 V	READ at 100 KHz		0.4	1.0	mA
I_{CC}	Supply Current V_{CC} = 5.0 V	WRITE at 100 KHz		2.0	3.0	mA
I_{SB1}(1)	Standby Current V_{CC} = 1.8 V	V_{IN} = V_{CC} or V_{SS}		0.6	3.0	µA
I_{SB2}	Standby Current V_{CC} = 2.5 V	V_{IN} = V_{CC} or V_{SS}		1.4	4.0	µA
I_{SB3}	Standby Current V_{CC} = 2.7 V	V_{IN} = V_{CC} or V_{SS}		1.6	4.0	µA
I_{SB4}	Standby Current V_{CC} = 5.0 V	V_{IN} = V_{CC} or V_{SS}		8.0	18.0	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}		0.10	3.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}		0.05	3.0	µA
V_{IL}	Input Low Level(2)		-1.0		V_{CC} x 0.3	V
V_{IH}	Input High Level(2)		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL2}	Output Low Level V_{CC} = 3.0 V	I_{OL} = 2.1 mA			0.40	V
V_{OL1}	Output Low Level V_{CC} = 1.8 V	I_{OL} = 1.5 mA			0.50	V

Typical(3) Standby Power vs. Voltage



Typical(3) Active Power vs. Voltage



Notes:
1. This parameter is preliminary and Atmel may change the specifications upon further characterization.
2. V_{IL} min and V_{IH} max are reference only and are not tested.
3. These graphs are for reference only and are not guaranteed by test.

AC Characteristics

Applicable over recommended operating range from T_A = -40°C to +85°C, V_{CC} = +1.8 V to +6.0 V CL = 1 TTL Gate and 100 pF (unless otherwise noted)

Symbol	Parameter	Min	Typ	Max	Units
f_{SCL}	Clock Frequency, SCL	0		100	kHz
t_{LOW}	Clock Pulse Width Low	4.7			µs
t_{HIGH}	Clock Pulse Width High	4.0			µs
t_I	Noise Suppression Time(2)		60	100	ns
t_{AA}	Clock Low to Data Out Valid	0.1		3.5	µs
t_{BUF}	Time the bus must be free before a new transmission can start	4.7			µs
$t_{HD.STA}$	Start Hold Time	4.0			µs
$t_{SU.STA}$	Start Set-up Time	4.7			µs
$t_{HD.DAT}$	Data In Hold Time	0.0			µs
$t_{SU.DAT}$	Data In Set-up Time	50			ns
t_R	Inputs Rise Time(2)			1.0	µs
t_F	Inputs Fall Time(2)			300	ns
$t_{SU.STO}$	Stop Set-up Time	4.7			µs
t_{DH}	Data Out Hold Time	100	180		ns
t_{WR}	Write Cycle Time		5	10	ms

Pin Capacitance (2)

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +1.8 V

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0 V
C_{IN}	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0 V

Note: 2. This parameter is characterized and is not 100% tested.

Device Operation

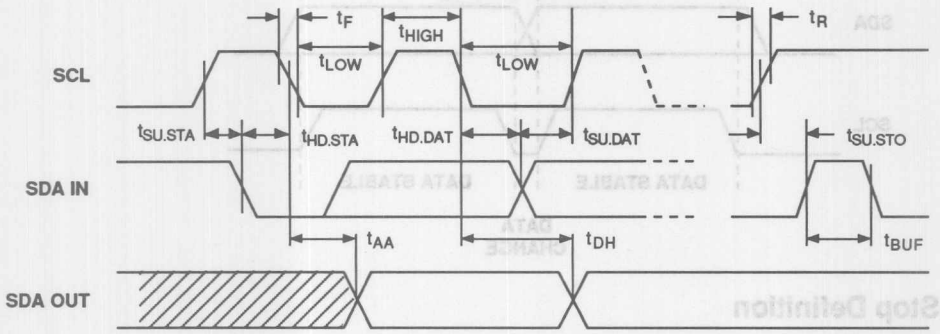
CLOCK and DATA TRANSITIONS: The SCL and SDA bus lines are normally pulled high with a resistor as shown in Figure 7. Data on the SDA bus may change only during SCL low time periods (refer to Data Validity Timing diagram). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Start and Stop Definition Timing diagram).

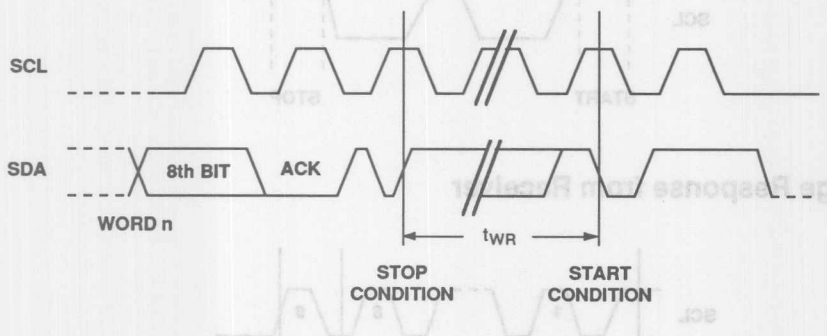
STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition which terminates all communications. After a read sequence, the stop command will place the E²PROM in a standby power mode (refer to Start and Stop Definition Timing Diagram).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the E²PROM in eight-bit words. Any device on the system bus receiving data (when communicating with the E²PROM) must pull the SDA bus low to acknowledge that it has successfully received each word. This must happen during the ninth clock cycle after each word received and after all other system devices have freed the SDA bus. The E²PROM will likewise acknowledge by pulling SDA low after receiving each address or data word (refer to Acknowledge Response from Receiver Timing diagram).

Bus Timing SCL: Serial Clock SDA: Serial Data I/O

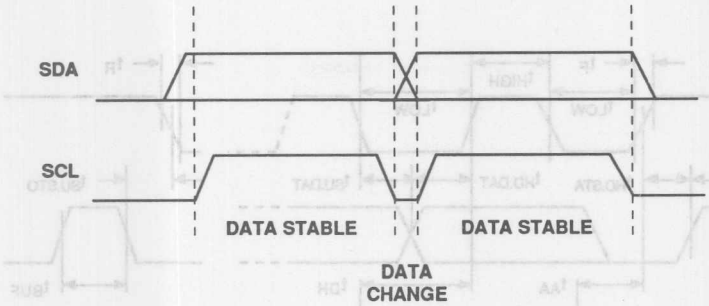


Write Cycle Timing SCL: Serial Clock SDA: Serial Data I/O

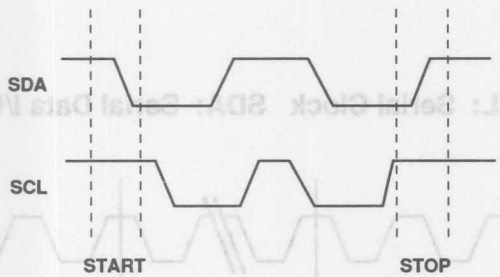


Note: The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

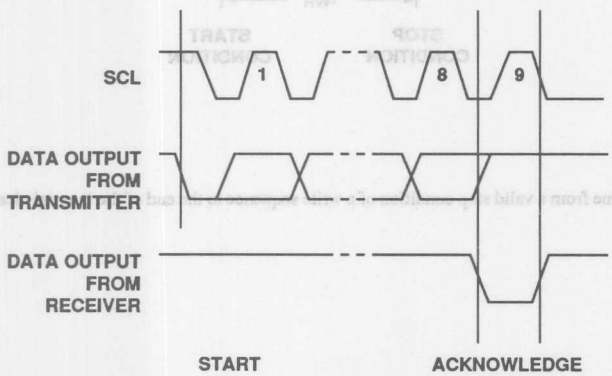
Data Validity



Start and Stop Definition



Acknowledge Response from Receiver



Device Addressing

The 1K, 2K, 4K, 8K and 16K E²PROM devices all require an eight-bit device address word following a start condition to enable the chip for a read or write operation (refer to Figure 1).

The device address word consists of a mandatory one, zero sequence for the first four most significant bits as shown. This is common to all the E²PROM devices.

The next three bits are the A2, A1 and A0 device address bits for the 1K/2K E²PROM. These three bits must compare to their corresponding hard-wired input pins.

The 4K E²PROM only uses the A2 and A1 device address bits with the third bit being a memory page address bit. The two device address bits must compare to their corresponding hard-wired input pins. The A0 pin is no connect.

The 8K E²PROM only uses the A2 device address bit with the next two bits being for memory page addressing. The A2 bit must compare to its corresponding hard-wired input pin. The A1 and A0 pins are no connect.

The 16K does not use any device address bits but instead the three bits are used for memory page addressing. These page addressing bits on the 4K and 16K devices should be considered the most significant bits of the data word address which follows. The A0, A1 and A2 pins are no connect.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the E²PROM will output an acknowledge on the SDA bus. If a compare is not made, the chip will return to a standby state.

Write Operations

BYTE WRITE: A write operation requires an eight-bit data word address following the device address word and acknowledgement. Upon receipt of this address, the E²PROM will again respond with an acknowledge on SDA and then clock in the first eight-bit data word. Following receipt of the eight-bit data word, the E²PROM will acknowledge SDA and the data transmitting device must terminate the write sequence with a stop condition. At this time the E²PROM enters an internally-timed write cycle to the nonvolatile memory. All inputs are disabled during this write cycle and the E²PROM will not respond for communication until the write is complete (refer to Figure 2).

PAGE WRITE: The 1K/2K E²PROM is capable of an eight-byte page write, and the 4K, 8K and 16K devices are capable of sixteen-byte page writes.

A page write is initiated the same as a byte write, but the data transmitting device does not send a stop condition after the first data word is clocked in. Instead, after the E²PROM acknowledges receipt of the first data word, the data transmitting device can transmit up to seven (1K/2K) or fifteen (4K, 8K, 16K) more data words. The E²PROM will respond with an acknowledge on SDA after each data word received. The transmitting device must terminate the page write sequence with a stop condition (refer to Figure 3).

The data word address lower three (1K/2K) or four (4K, 8K, 16K) bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented retaining the memory page row location. If more than eight (1K/2K) or sixteen (4K, 8K, 16K) data words are transmitted to the E²PROM, the data word address will "roll over" and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally-timed write cycle has started and the E²PROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the E²PROM respond with an acknowledge on the SDA bus allowing the read or write sequence to continue.

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. If the last operation was a read at address n, then the current address would be n+1. If the final operation was a write at address n, the current address would again be n+1 with one exception. If address n was the eighth (1K/2K) or sixteenth (4K, 8K, 16K) byte address in the memory row, the incremented address n+1 would "roll over" to the 1st byte address of the same row.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the E²PROM, the current address data word is serially clocked out. The device that is reading the data does not respond with an acknowledge (leaving the SDA bus high) but does generate a following stop condition (refer to Figure 4)

RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the E²PROM, the transmitting device must generate another start condition. The transmitting device now initiates a current address read by

sending a device address with the read/write select bit high. The E²PROM acknowledges the device address and serially clocks out the data word. The device reading the data does not respond with an acknowledge (leaving the SDA bus high) but does generate a following stop condition (refer to Figure 5).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the device reading the data receives a data word, it responds with an acknowledge. As long as the E²PROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the device reading the data does not respond with an acknowledge (leaving the SDA bus high) but does generate a following stop condition (refer to Figure 6).

Figure 1. Device Address

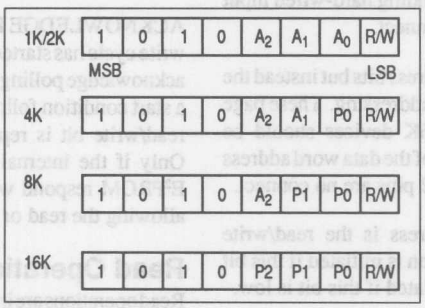


Figure 2. Byte Write

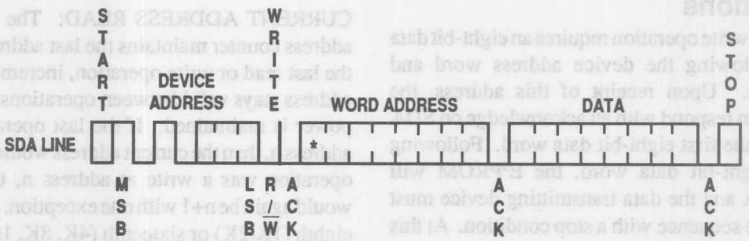
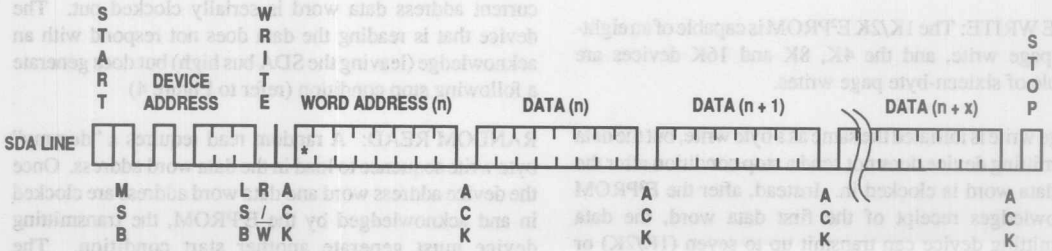


Figure 3. Page Write



(* = Don't care bit for 1K)

Figure 4. Current Address Read

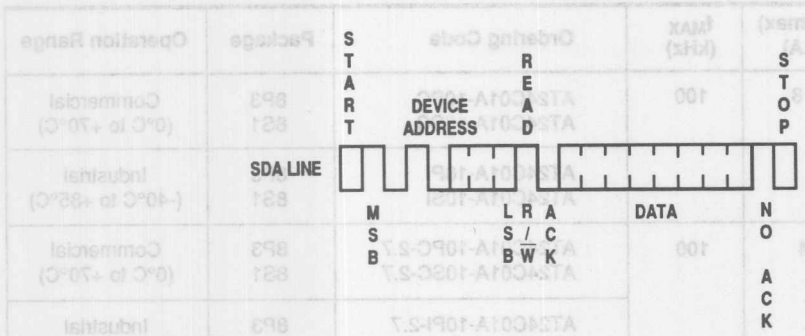


Figure 5. Random Read

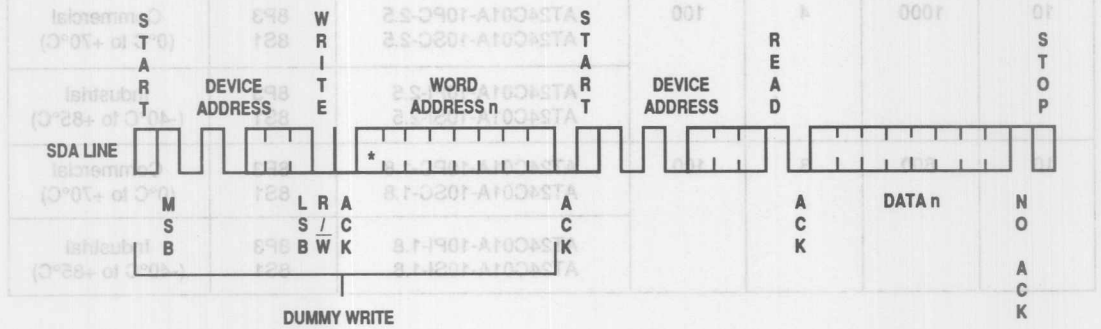


Figure 6. Sequential Read

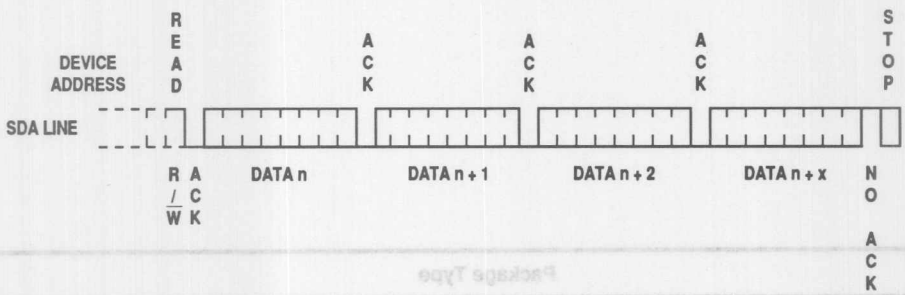
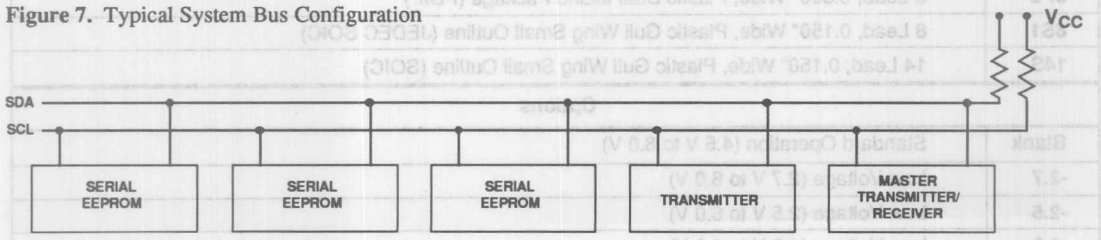


Figure 7. Typical System Bus Configuration



(* = Don't care bit for 1K)

Ordering Information

t_{WR} (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	18	100	AT24C01A-10PC AT24C01A-10SC	8P3 8S1	Commercial (0°C to +70°C)
				AT24C01A-10PI AT24C01A-10SI	8P3 8S1	Industrial (-40°C to +85°C)
10	1500	4	100	AT24C01A-10PC-2.7 AT24C01A-10SC-2.7	8P3 8S1	Commercial (0°C to +70°C)
				AT24C01A-10PI-2.7 AT24C01A-10SI-2.7	8P3 8S1	Industrial (-40°C to +85°C)
10	1000	4	100	AT24C01A-10PC-2.5 AT24C01A-10SC-2.5	8P3 8S1	Commercial (0°C to +70°C)
				AT24C01A-10PI-2.5 AT24C01A-10SI-2.5	8P3 8S1	Industrial (-40°C to +85°C)
10	800	3	100	AT24C01A-10PC-1.8 AT24C01A-10SC-1.8	8P3 8S1	Commercial (0°C to +70°C)
				AT24C01A-10PI-1.8 AT24C01A-10SI-1.8	8P3 8S1	Industrial (-40°C to +85°C)

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual InLine Package (PDIP)
8S1	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
14S	14 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (SOIC)
Options	
Blank	Standard Operation (4.5 V to 6.0 V)
-2.7	Low Voltage (2.7 V to 6.0 V)
-2.5	Low Voltage (2.5 V to 6.0 V)
-1.8	Low Voltage (1.8 V to 6.0 V)

Ordering Information

t_{WR} (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	18	100	AT24C02-10PC AT24C02N-10SC AT24C02-10SC	8P3 8S1 14S	Commercial (0°C to +70°C)
				AT24C02-10PI AT24C02N-10SI AT24C02-10SI	8P3 8S1 14S	Industrial (-40°C to +85°C)
10	1500	4	100	AT24C02-10PC-2.7 AT24C02N-10SC-2.7 AT24C02-10SC-2.7	8P3 8S1 14S	Commercial (0°C to +70°C)
				AT24C02-10PI-2.7 AT24C02N-10SI-2.7 AT24C02-10SI-2.7	8P3 8S1 14S	Industrial (-40°C to +85°C)
10	1000	4	100	AT24C02-10PC-2.5 AT24C02N-10SC-2.5 AT24C02-10SC-2.5	8P3 8S1 14S	Commercial (0°C to +70°C)
				AT24C02-10PI-2.5 AT24C02N-10SI-2.5 AT24C02-10SI-2.5	8P3 8S1 14S	Industrial (-40°C to +85°C)
10	800	3	100	AT24C02-10PC-1.8 AT24C02N-10SC-1.8 AT24C02-10SC-1.8	8P3 8S1 14S	Commercial (0°C to +70°C)
				AT24C02-10PI-1.8 AT24C02N-10SI-1.8 AT24C02-10SI-1.8	8P3 8S1 14S	Industrial (-40°C to +85°C)

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual InLine Package (PDIP)
8S1	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
14S	14 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (SOIC)

Options	
Blank	Standard Operation (4.5 V to 6.0 V)
-2.7	Low Voltage (2.7 V to 6.0 V)
-2.5	Low Voltage (2.5 V to 6.0 V)
-1.8	Low Voltage (1.8 V to 6.0 V)

Ordering Information

t_{WR} (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	18	100	AT24C04-10PC AT24C04N-10SC AT24C04-10SC	8P3 8S1 14S	Commercial (0°C to +70°C)
				AT24C04-10PI AT24C04N-10SI AT24C04-10SI	8P3 8S1 14S	Industrial (-40°C to +85°C)
10	1500	4	100	AT24C04-10PC-2.7 AT24C04N-10SC-2.7 AT24C04-10SC-2.7	8P3 8S1 14S	Commercial (0°C to +70°C)
				AT24C04-10PI-2.7 AT24C04N-10SI-2.7 AT24C04-10SI-2.7	8P3 8S1 14S	Industrial (-40°C to +85°C)
10	1000	4	100	AT24C04-10PC-2.5 AT24C04N-10SC-2.5 AT24C04-10SC-2.5	8P3 8S1 14S	Commercial (0°C to +70°C)
				AT24C04-10PI-2.5 AT24C04N-10SI-2.5 AT24C04-10SI-2.5	8P3 8S1 14S	Industrial (-40°C to +85°C)
10	800	3	100	AT24C04-10PC-1.8 AT24C04N-10SC-1.8 AT24C04-10SC-1.8	8P3 8S1 14S	Commercial (0°C to +70°C)
				AT24C04-10PI-1.8 AT24C04N-10SI-1.8 AT24C04-10SI-1.8	8P3 8S1 14S	Industrial (-40°C to +85°C)

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual InLine Package (PDIP)
8S1	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
14S	14 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (SOIC)

Options	
Blank	Standard Operation (4.5 V to 6.0 V)
-2.7	Low Voltage (2.7 V to 6.0 V)
-2.5	Low Voltage (2.5 V to 6.0 V)
-1.8	Low Voltage (1.8 V to 6.0 V)

Ordering Information

t_{WR} (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	18	100	AT24C08-10PC AT24C08N-10SC AT24C08-10SC	8P3 8S1 14S	Commercial (0°C to +70°C)
				AT24C08-10PI AT24C08N-10SI AT24C08-10SI	8P3 8S1 14S	Industrial (-40°C to +85°C)
10	1500	4	100	AT24C08-10PC-2.7 AT24C08N-10SC-2.7 AT24C08-10SC-2.7	8P3 8S1 14S	Commercial (0°C to +70°C)
				AT24C08-10PI-2.7 AT24C08N-10SI-2.7 AT24C08-10SI-2.7	8P3 8S1 14S	Industrial (-40°C to +85°C)
10	1000	4	100	AT24C08-10PC-2.5 AT24C08N-10SC-2.5 AT24C08-10SC-2.5	8P3 8S1 14S	Commercial (0°C to +70°C)
				AT24C08-10PI-2.5 AT24C08N-10SI-2.5 AT24C08-10SI-2.5	8P3 8S1 14S	Industrial (-40°C to +85°C)
10	800	3	100	AT24C08-10PC-1.8 AT24C08N-10SC-1.8 AT24C08-10SC-1.8	8P3 8S1 14S	Commercial (0°C to +70°C)
				AT24C08-10PI-1.8 AT24C08N-10SI-1.8 AT24C08-10SI-1.8	8P3 8S1 14S	Industrial (-40°C to +85°C)

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual InLine Package (PDIP)
8S1	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
14S	14 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (SOIC)
Options	
Blank	Standard Operation (4.5 V to 6.0 V)
-2.7	Low Voltage (2.7 V to 6.0 V)
-2.5	Low Voltage (2.5 V to 6.0 V)
-1.8	Low Voltage (1.8 V to 6.0 V)

Ordering Information

t_{WR} (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	18	100	AT24C16-10PC AT24C16N-10SC AT24C16-10SC	8P3 8S1 14S	Commercial (0°C to +70°C)
				AT24C16-10PI AT24C16N-10SI AT24C16-10SI	8P3 8S1 14S	Industrial (-40°C to +85°C)
10	1500	4	100	AT24C16-10PC-2.7 AT24C16N-10SC-2.7 AT24C16-10SC-2.7	8P3 8S1 14S	Commercial (0°C to +70°C)
				AT24C16-10PI-2.7 AT24C16N-10SI-2.7 AT24C16-10SI-2.7	8P3 8S1 14S	Industrial (-40°C to +85°C)
10	1000	4	100	AT24C16-10PC-2.5 AT24C16N-10SC-2.5 AT24C16-10SC-2.5	8P3 8S1 14S	Commercial (0°C to +70°C)
				AT24C16-10PI-2.5 AT24C16N-10SI-2.5 AT24C16-10SI-2.5	8P3 8S1 14S	Industrial (-40°C to +85°C)
10	800	3	100	AT24C16-10PC-1.8 AT24C16N-10SC-1.8 AT24C16-10SC-1.8	8P3 8S1 14S	Commercial (0°C to +70°C)
				AT24C16-10PI-1.8 AT24C16N-10SI-1.8 AT24C16-10SI-1.8	8P3 8S1 14S	Industrial (-40°C to +85°C)

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual InLine Package (PDIP)
8S1	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
14S	14 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (SOIC)

Options	
Blank	Standard Operation (4.5 V to 6.0 V)
-2.7	Low Voltage (2.7 V to 6.0 V)
-2.5	Low Voltage (2.5 V to 6.0 V)
-1.8	Low Voltage (1.8 V to 6.0 V)

Features

- **Low Voltage and Standard Voltage Operation**
  - **5.0 (V_{CC} = 4.5 V to 6.0 V)**
  - **3.0 (V_{CC} = 2.7 V to 6.0 V)**
  - **2.5 (V_{CC} = 2.5 V to 6.0 V)**
  - **2.0 (V_{CC} = 1.8 V to 6.0 V)**
- **Internally Organized 2048 x 8 (16K)**
- **Two-wire Serial Interface**
- **Bidirectional Data Transfer Protocol**
- **16-byte Page Write Mode**
- **Partial Page Writes Are Allowed**
- **Self-timed Write Cycle (10 ms max)**
- **High Reliability**
  - **Endurance: 100,000 Cycles**
  - **Data Retention: 100 Years**
- **Eight-pin JEDEC SOIC and Eight-pin PDIP Packages**

2-Wire Serial CMOS E²PROMs

16K (2048 x 8)

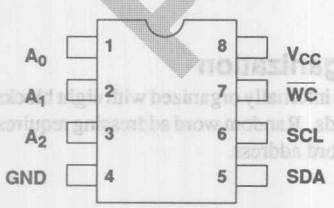
Preliminary

Description

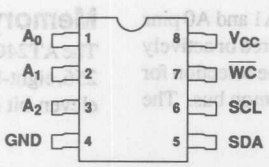
The AT24C164 provides 16384 bits of serial EEPROM (Electrically Erasable and Programmable Read Only Memory) organized as 2048 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT24C164 is available in space saving eight-pin PDIP, and eight-pin SOIC packages and is accessed via a two-wire serial interface. Atmel's EEPROMs are designed and tested for applications requiring extended endurance. The AT24C164 is guaranteed for 100,000 erase/write cycles and 100 year data retention. In addition, this device is available in 5.0 V (4.5 V to 6.0 V), 3.0 V (2.7 V to 6.0 V), 2.5 V (2.5 V to 6.0 V) and 2.0 V (1.8 V to 6.0 V) versions.

Pin Configurations

Pin Name	Function
A_0 to A_2	Address Inputs
SDA	Serial Data
SCL	Serial Clock
$\overline{WC}$	**Write Control**
NC	No Connect



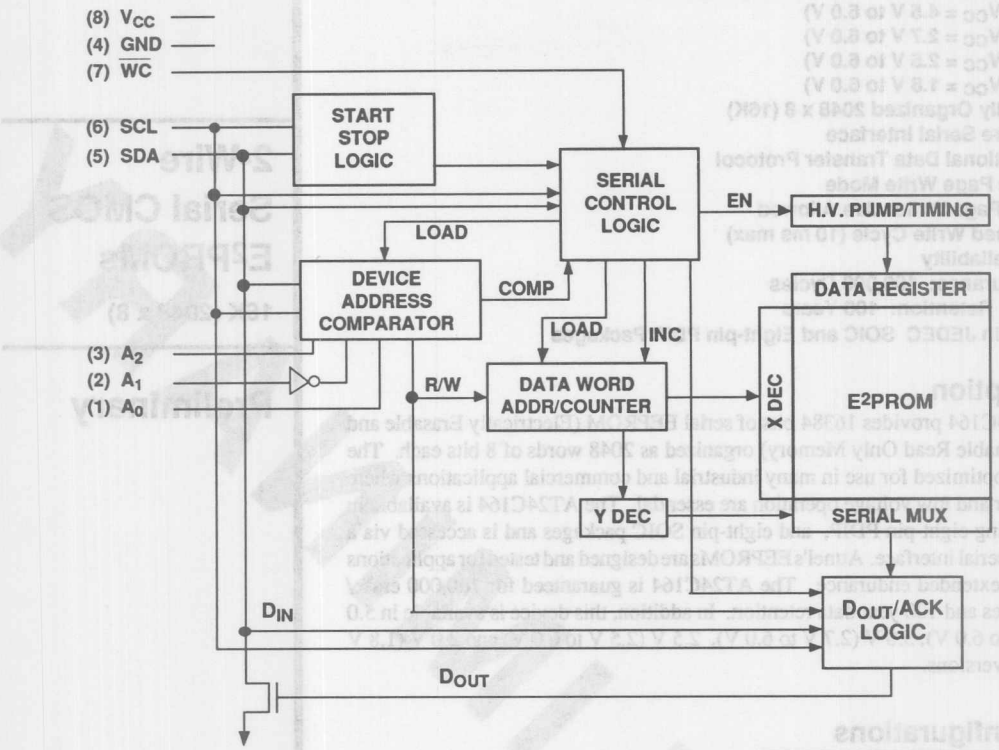
8-pin PDIP



8-pin SOIC

PRELIMINARY

Block Diagram



Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each E²PROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open drain or open collector devices.

DEVICE SELECT (A2, A1, A0): The A2, A1 and A0 pins are device address inputs that may be hardwired or actively driven to V_{DD} or V_{SS}. These inputs allow the selection for one of eight possible devices sharing a common bus. The AT24C164 can be made compatible with the AT24C16 by tying A2, A1 and A0 to V_{SS}. Device addressing is discussed in detail in the device addressing section.

WRITE CONTROL ($\overline{WC}$): The write control input, when tied low to V_{SS}, allows normal write operations. When $\overline{WC}$ is tied high to V_{CC}, all write operations to the memory are inhibited.

Memory Organization

The AT24C164 is internally organized with eight blocks of 256, eight-bit words. Random word addressing requires an eleven-bit data word address.

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0 V to +7.0 V
Maximum Operating Voltage	6.6 V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

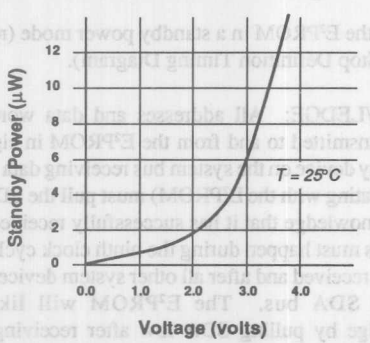
2

DC Characteristics

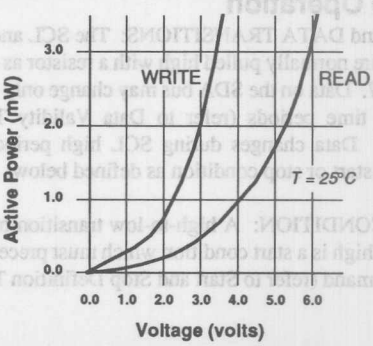
Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +1.8 V to +6.0 V, T_{AC} = 0°C to +70°C, V_{CC} = +1.8 V to +6.0 V (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC1}(1)	Supply Voltage		1.8	5.0	6.0	V
V_{CC2}	Supply Voltage		2.5	5.0	6.0	V
V_{CC3}	Supply Voltage		2.7	5.0	6.0	V
V_{CC4}	Supply Voltage		4.5	5.0	5.5	V
I_{CC}	Supply Current V_{CC} = 5.0 V	READ at 100 KHz		0.4	1.0	mA
I_{CC}	Supply Current V_{CC} = 5.0 V	WRITE at 100 KHz		2.0	3.0	mA
I_{SB1}(1)	Standby Current V_{CC} = 1.8 V	V_{IN} = V_{CC} or V_{SS}		0.6	3.0	µA
I_{SB2}	Standby Current V_{CC} = 2.5 V	V_{IN} = V_{CC} or V_{SS}		1.4	4.0	µA
I_{SB3}	Standby Current V_{CC} = 2.7 V	V_{IN} = V_{CC} or V_{SS}		1.6	4.0	µA
I_{SB4}	Standby Current V_{CC} = 5.0 V	V_{IN} = V_{CC} or V_{SS}		8.0	18.0	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}		0.10	3.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}		0.05	3.0	µA
V_{IL}	Input Low Level(2)		-1.0		V_{CC} x 0.3	V
V_{IH}	Input High Level(2)		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL2}	Output Low Level V_{CC} = 3.0 V	I_{OL} = 2.1 mA			0.40	V
V_{OL1}	Output Low Level V_{CC} = 1.8 V	I_{OL} = 1.5 mA			0.50	V

Typical(3) Standby Power vs. Voltage



Typical(3) Active Power vs. Voltage



Notes:
1. This parameter is preliminary and Atmel may change the specifications upon further characterization.
2. V_{IL} min and V_{IH} max are reference only and are not tested.
3. These graphs are for reference only and are not guaranteed by test.

AC Characteristics

Applicable over recommended operating range from T_A = -40°C to +85°C, V_{CC} = +1.8 V to +6.0 V CL = 1 TTL Gate and 100 pF (unless otherwise noted)

Symbol	Parameter	Min	Typ	Max	Units
f_{SCL}	Clock Frequency, SCL	0		100	kHz
t_{LOW}	Clock Pulse Width Low	4.7			µs
t_{HIGH}	Clock Pulse Width High	4.0			µs
t_I	Noise Suppression Time(2)		60	100	ns
t_{AA}	Clock Low to Data Out Valid	0.1		3.5	µs
t_{BUF}	Time the bus must be free before a new transmission can start	4.7			µs
$t_{HD.STA}$	Start Hold Time	4.0			µs
$t_{SU.STA}$	Start Set-up Time	4.7			µs
$t_{HD.DAT}$	Data In Hold Time	0.0			µs
$t_{SU.DAT}$	Data In Set-up Time	50			ns
t_R	Inputs Rise Time(2)			1.0	µs
t_F	Inputs Fall Time(2)			300	ns
$t_{SU.STO}$	Stop Set-up Time	4.7			µs
t_{DH}	Data Out Hold Time	100	180		ns
t_{WR}	Write Cycle Time		5	10	ms

Pin Capacitance (2)

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +1.8 V

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0 V
C_{IN}	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0 V

Note: 2. This parameter is characterized and is not 100% tested.

Device Operation

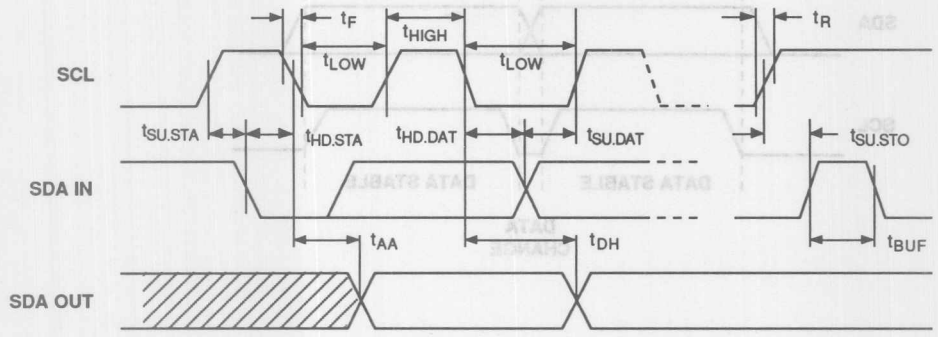
CLOCK and DATA TRANSITIONS: The SCL and SDA bus lines are normally pulled high with a resistor as shown in Figure 7. Data on the SDA bus may change only during SCL low time periods (refer to Data Validity Timing diagram). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Start and Stop Definition Timing diagram).

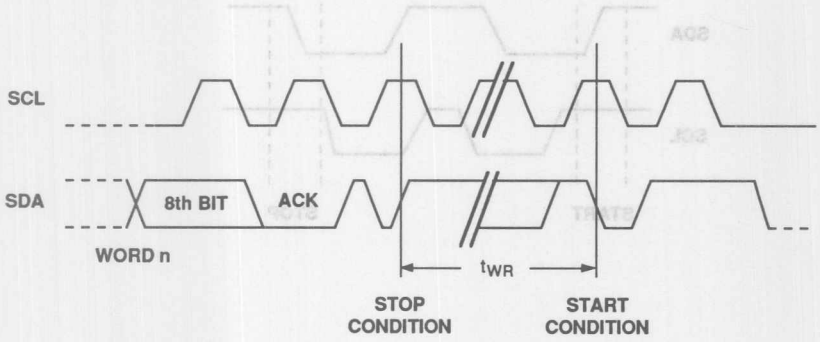
STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition which terminates all communications. After a read sequence, the stop command will place the E²PROM in a standby power mode (refer to Start and Stop Definition Timing Diagram).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the E²PROM in eight-bit words. Any device on the system bus receiving data (when communicating with the E²PROM) must pull the SDA bus low to acknowledge that it has successfully received each word. This must happen during the ninth clock cycle after each word received and after all other system devices have freed the SDA bus. The E²PROM will likewise acknowledge by pulling SDA low after receiving each address or data word (refer to Acknowledge Response from Receiver Timing diagram).

Bus Timing SCL: Serial Clock SDA: Serial Data I/O

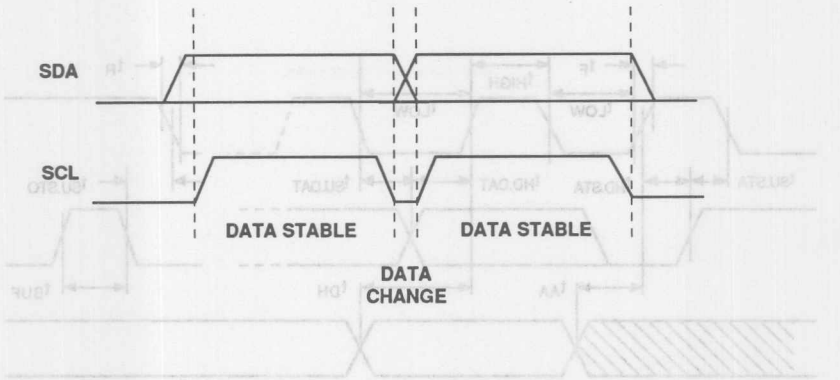


Write Cycle Timing SCL: Serial Clock SDA: Serial Data I/O



Note: The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

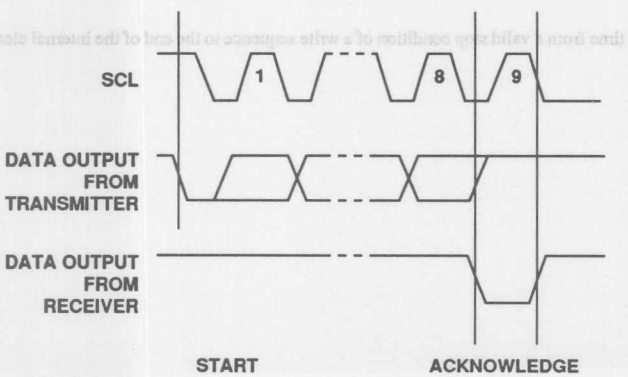
Data Validity



Start and Stop Definition



Acknowledge Response from Receiver



Device Addressing

The AT24C164 requires an eight-bit device address word following a start condition to enable the chip for read or write operations (refer to Figure 1). The most significant bit must be a one followed by the A2, A1 and A0 device select bits (the A1 bit must be the compliment of the A1 input pin signal). The next three bits are used for memory block addressing and select one of the eight 256 x 8 memory blocks. These bits should be considered the three most significant bits of the data word address. The eighth bit of the device address is the read/write select bit. A read operation is selected if this bit is high or a write operation is selected if this bit is low.

Upon a compare of the device address, the E²PROM will output an acknowledge on the SDA bus. If a compare is not made, the chip will return to a standby state.

Write Operations

BYTE WRITE: A write operation requires an eight-bit data word address following the device address word and acknowledgement. Upon receipt of this address, the E²PROM will again respond with an acknowledge on SDA and then clock in the first eight-bit data word. Following receipt of the eight-bit data word, the E²PROM will acknowledge SDA and the data transmitting device must terminate the write sequence with a stop condition. At this time the E²PROM enters an internally-timed write cycle to the nonvolatile memory. All inputs are disabled during this write cycle and the E²PROM will not respond for communication until the write is complete (refer to Figure 2).

PAGE WRITE: The AT24C164 is capable of a sixteen-byte page write. A page write is initiated the same as a byte write, but the data transmitting device does not send a stop condition after the first data word is clocked in. Instead, after the E²PROM acknowledges receipt of the first data word, the data transmitting device can transmit up to fifteen more data words. The E²PROM will respond with an acknowledge on SDA after each data word received. The transmitting device must terminate the page write sequence with a stop condition (refer to Figure 3).

The data word address lower four bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented retaining the memory page row location. If more than sixteen data words are transmitted to the E²PROM, the data word address will "roll over" and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally-timed write cycle has started and the E²PROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the E²PROM respond with an acknowledge on the SDA bus allowing the read or write sequence to continue.

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. If the last operation was a read at address n, then the current address would be n+1. If the final operation was a write at address n, the current address would again be n+1 with one exception. If address n was the sixteenth byte address in the memory row, the incremented address n+1 would "roll over" to the 1st byte address of the same row.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the E²PROM, the current address data word is serially clocked out. The device that is reading the data does not respond with an acknowledge (leaving the SDA bus high) but does generate a following stop condition (refer to Figure 4)

RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the E²PROM, the transmitting device must generate another start condition. The transmitting device now initiates a current address read by sending a device address with the read/write select bit high. The E²PROM acknowledges the device address and serially clocks out the data word. The device reading the data does not respond with an acknowledge (leaving the SDA bus high) but does generate a following stop condition (refer to Figure 5).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the device reading the data receives a data word, it responds with an acknowledge. As long as the E²PROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the device reading the data does not respond with an acknowledge (leaving the SDA bus high) but does generate a following stop condition (refer to Figure 6).

Figure 1. Device Address

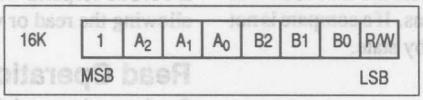


Figure 2. Byte Write

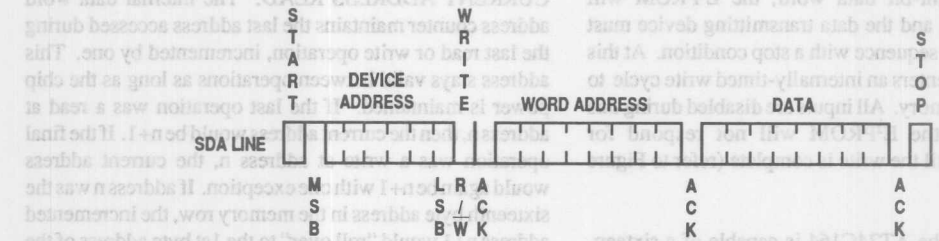


Figure 3. Page Write

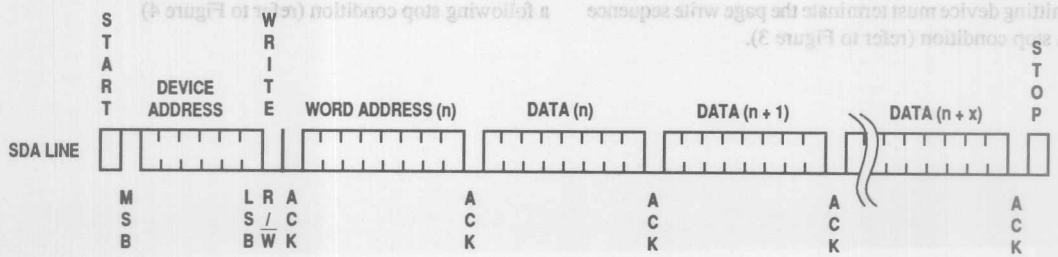


Figure 4. Current Address Read

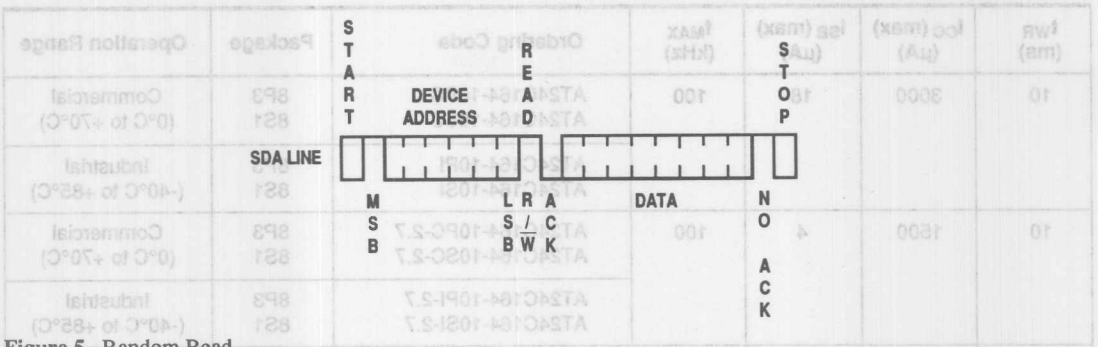


Figure 5. Random Read

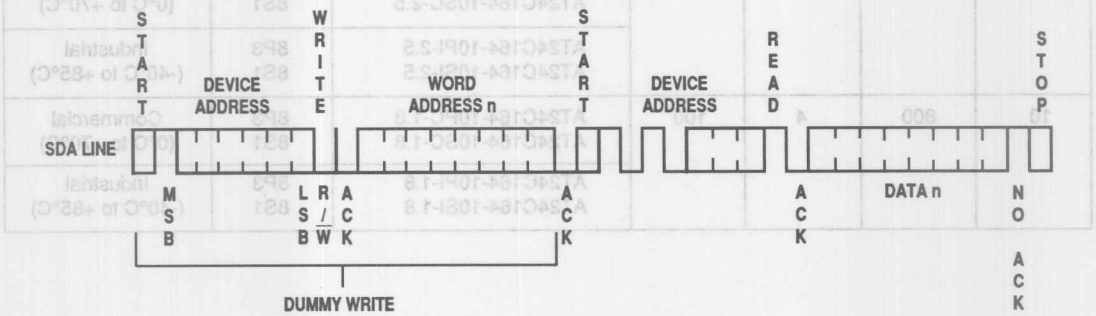


Figure 6. Sequential Read

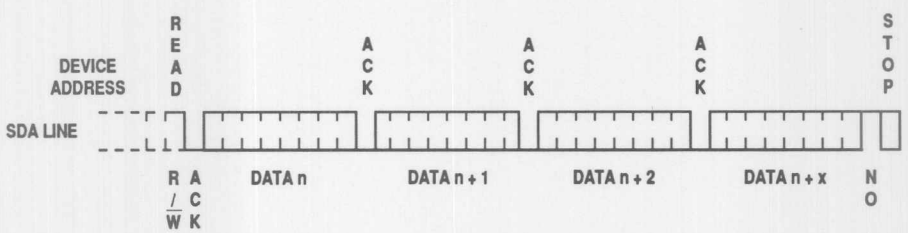
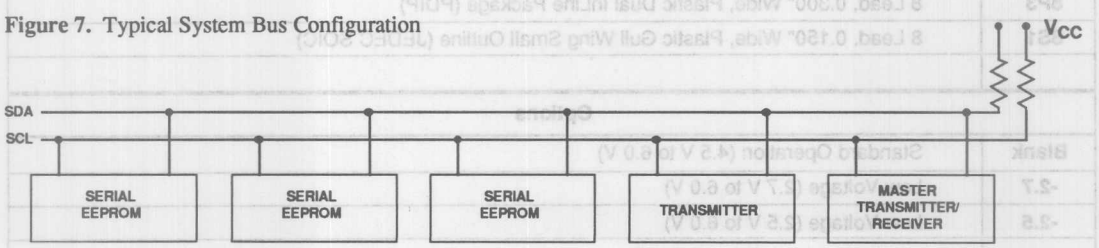


Figure 7. Typical System Bus Configuration



Ordering Information

t_{WR} (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	18	100	AT24C164-10PC AT24C164-10SC	8P3 8S1	Commercial (0°C to +70°C)
				AT24C164-10PI AT24C164-10SI	8P3 8S1	Industrial (-40°C to +85°C)
10	1500	4	100	AT24C164-10PC-2.7 AT24C164-10SC-2.7	8P3 8S1	Commercial (0°C to +70°C)
				AT24C164-10PI-2.7 AT24C164-10SI-2.7	8P3 8S1	Industrial (-40°C to +85°C)
10	1000	4	100	AT24C164-10PC-2.5 AT24C164-10SC-2.5	8P3 8S1	Commercial (0°C to +70°C)
				AT24C164-10PI-2.5 AT24C164-10SI-2.5	8P3 8S1	Industrial (-40°C to +85°C)
10	800	4	100	AT24C164-10PC-1.8 AT24C164-10SC-1.8	8P3 8S1	Commercial (0°C to +70°C)
				AT24C164-10PI-1.8 AT24C164-10SI-1.8	8P3 8S1	Industrial (-40°C to +85°C)

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual InLine Package (PDIP)
8S1	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)

Options	
Blank	Standard Operation (4.5 V to 6.0 V)
-2.7	Low Voltage (2.7 V to 6.0 V)
-2.5	Low Voltage (2.5 V to 6.0 V)
-1.8	Low Voltage (1.8 V to 6.0 V)

3-Wire Serial CMOS E²PROMs

1K (128 x 8 or 64 x 16)

2K (256 x 8 or 128 x 16)

4K (512 x 8 or 256 x 16)

Features

- **Low Voltage and Standard Voltage Operation**
  - **5.0 V (V_{CC} = 4.5 V to 5.5 V)**
  - **3.0 V (V_{CC} = 2.7 V to 5.5 V)**
  - **2.5 V (V_{CC} = 2.5 V to 5.5 V)**
  - **2.0 V (V_{CC} = 1.8 V to 5.5 V)**
- **User Selectable Internal Organization**
  - **1K: 128 x 8 or 64 x 16**
  - **2K: 256 x 8 or 128 x 16**
  - **4K: 512 x 8 or 256 x 16**
- **Three-Wire Serial Interface**
- **Self-Timed Write Cycle (10 ms Max)**
- **High Reliability**
  - **Endurance: 100,000 Cycles**
  - **Data Retention: 100 Years**
- **Eight-Pin PDIP, JEDEC SOIC, and EIAJ SOIC Packages**

Description

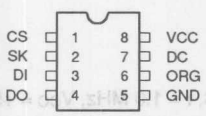
The AT93C46/56/57/66 provides 1024/2048/4096 bits of serial E²PROM (Electrically Erasable Programmable Read Only Memory) organized as 64/128/256 words of 16 bits each, when the ORG Pin is connected to V_{CC} and 128/256/512 words of eight bits each when it is tied to ground. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT93C46/56/57/66 is available in space saving eight-pin PDIP and eight-pin JEDEC and EIAJ SOIC packages.

The AT93C46/56/57/66 is enabled through the Chip Select pin (CS), and accessed via a three-wire serial interface consisting of Data Input (DI), Data Output (DO), and Shift Clock (SK). Upon receiving a READ instruction at DI, the address is decoded and the data is clocked out serially on the data output pin DO. The WRITE cycle is completely self-timed and no separate ERASE cycle is required before WRITE. The WRITE cycle is only enabled when the part is in the ERASE/WRITE ENABLE state. When CS is brought "high" following the initiation of a WRITE cycle, the DO pin outputs the READY/BUSY status of the part.

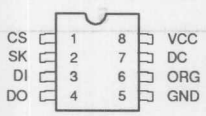
Atmel's E²PROMs are designed and tested for applications requiring extended endurance. Devices in this family are guaranteed for 100,000 ERASE/WRITE cycles and 100-year data retention. The AT93C46/56/57/66 is available in 5.0 V ± 10%, 2.7 V to 5.5 V, 2.5 V to 5.5 V, and 1.8 V to 5.5 V versions.

Pin Configurations

Pin Name	Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply
ORG	Internal Organization
DC	Don't Connect



8-Pin PDIP



8-Pin SOIC

Rotated (R)
(1K JEDEC Only)



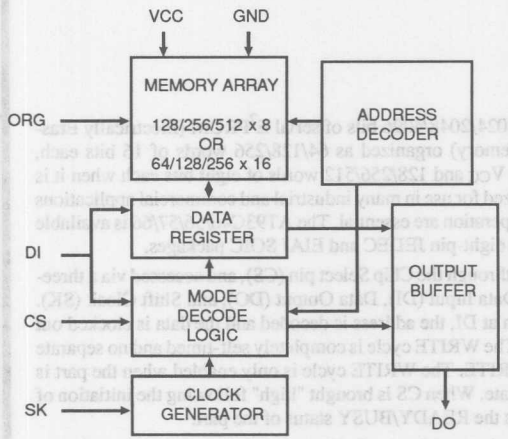
8-Pin SOIC

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0 V to +7.0 V
Maximum Operating Voltage	6.25 V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram (1)



Note:
1. When the ORG pin is connected to V_{CC}, the x 16 organization is selected. When it is connected to ground, the x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the x 16 organization.

Pin Capacitance (1)

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +5.0 V (unless otherwise noted)

	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (DO)	5	pF	V_{OUT} = 0 V
C_{IN}	Input Capacitance (CS, SK, DI)	5	pF	V_{IN} = 0 V

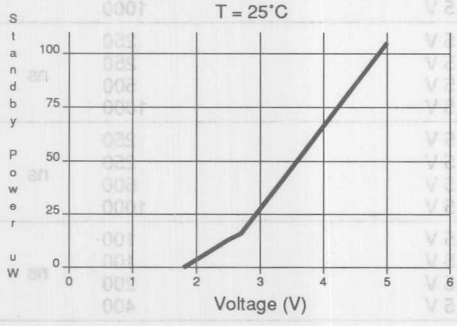
Note: 1. This parameter is characterized and is not 100% tested.

D.C. Characteristics

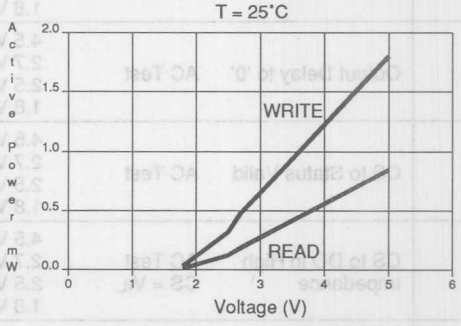
Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +1.8 V to +5.5 V, T_{AC} = 0°C to + 70°C, V_{CC} = +1.8 V to +5.5 V (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC1} (1)	Supply Voltage			1.8	5.0	5.5	V
V_{CC2}	Supply Voltage			2.5	5.0	5.5	V
V_{CC3}	Supply Voltage			2.7	5.0	5.5	V
V_{CC4}	Supply Voltage			4.5	5.0	5.5	V
I_{CC}	Supply Current	V_{CC} = 5.0 V	READ at 1.0 MHz		0.2	0.5	mA
			WRITE at 1.0 MHz		0.4	1.0	mA
I_{SB1} (1)	Standby Current	V_{CC} = 1.8 V	CS = 0 V		0.0	0.1	µA
I_{SB2}	Standby Current	V_{CC} = 2.5 V	CS = 0 V		5.0	7.0	µA
I_{SB3}	Standby Current	V_{CC} = 2.7 V	CS = 0 V		6.0	10.0	µA
I_{SB4}	Standby Current	V_{CC} = 5.0 V	CS = 0 V		21.0	30.0	µA
I_{IL}	Input Leakage	V_{IN} = 0 V to V_{CC}			0.1	1.0	µA
I_{OL}	Output Leakage	V_{IN} = 0 V to V_{CC}			0.1	1.0	µA
V_{IL1} (2) V_{IH1} (2)	Input Low Voltage Input High Voltage	4.5 V ≤ V_{CC} ≤ 5.5 V		-0.1 2.0		0.8 V_{CC}+1	V
V_{IL2} (2) V_{IH2} (2)	Input Low Voltage Input High Voltage	1.8 V ≤ V_{CC} ≤ 5.5 V		0.0 1.4		0.4 V_{CC}+1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage	4.5 V ≤ V_{CC} ≤ 5.5 V		 2.4		0.4	V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage	1.8 V ≤ V_{CC} ≤ 5.5 V		 V_{CC}-0.2		0.2	V

Typical Standby Power vs. Voltage(3)



Typical Active Power vs. Voltage(3)



Notes: 1. This parameter is preliminary and Atmel may change the specifications upon further characterization.
2. V_{IL} min and V_{IH} max are reference only and are not tested.
3. These graphs are for reference only and are not guarenteed by test.

A.C. Characteristics

Applicable over recommended operating range from T_A = -40°C to + 85°C, V_{CC} = As Specified, CL = 1 TTL Gate and 100 pF (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
f_{SK}	SK Clock Frequency		4.5 V ≤ V_{CC} ≤ 5.5 V	0		1	MHz
			2.7 V ≤ V_{CC} ≤ 5.5 V	0		1	
			2.5 V ≤ V_{CC} ≤ 5.5 V	0		0.5	
			1.8 V ≤ V_{CC} ≤ 5.5 V	0		0.25	
t_{SKH}	SK High Time		4.5 V ≤ V_{CC} ≤ 5.5 V	250			ns
			2.7 V ≤ V_{CC} ≤ 5.5 V	250			
			2.5 V ≤ V_{CC} ≤ 5.5 V	500			
			1.8 V ≤ V_{CC} ≤ 5.5 V	1000			
t_{SKL}	SK Low Time		4.5 V ≤ V_{CC} ≤ 5.5 V	250			ns
			2.7 V ≤ V_{CC} ≤ 5.5 V	250			
			2.5 V ≤ V_{CC} ≤ 5.5 V	500			
			1.8 V ≤ V_{CC} ≤ 5.5 V	1000			
t_{CS}	Minimum CS Low Time		4.5 V ≤ V_{CC} ≤ 5.5 V	250			ns
			2.7 V ≤ V_{CC} ≤ 5.5 V	250			
			2.5 V ≤ V_{CC} ≤ 5.5 V	500			
			1.8 V ≤ V_{CC} ≤ 5.5 V	1000			
t_{CSS}	CS Setup Time	Relative to SK	4.5 V ≤ V_{CC} ≤ 5.5 V	50			ns
			2.7 V ≤ V_{CC} ≤ 5.5 V	50			
			2.5 V ≤ V_{CC} ≤ 5.5 V	100			
			1.8 V ≤ V_{CC} ≤ 5.5 V	200			
t_{DIS}	DI Setup Time	Relative to SK	4.5 V ≤ V_{CC} ≤ 5.5 V	100			ns
			2.7 V ≤ V_{CC} ≤ 5.5 V	100			
			2.5 V ≤ V_{CC} ≤ 5.5 V	200			
			1.8 V ≤ V_{CC} ≤ 5.5 V	400			
t_{CSH}	CS Hold Time	Relative to SK		0			ns
t_{DIH}	DI Hold Time	Relative to SK	4.5 V ≤ V_{CC} ≤ 5.5 V	100			ns
			2.7 V ≤ V_{CC} ≤ 5.5 V	100			
			2.5 V ≤ V_{CC} ≤ 5.5 V	200			
			1.8 V ≤ V_{CC} ≤ 5.5 V	400			
t_{PD1}	Output Delay to '1'	AC Test	4.5 V ≤ V_{CC} ≤ 5.5 V			250	ns
			2.7 V ≤ V_{CC} ≤ 5.5 V			250	
			2.5 V ≤ V_{CC} ≤ 5.5 V			500	
			1.8 V ≤ V_{CC} ≤ 5.5 V			1000	
t_{PD0}	Output Delay to '0'	AC Test	4.5 V ≤ V_{CC} ≤ 5.5 V			250	ns
			2.7 V ≤ V_{CC} ≤ 5.5 V			250	
			2.5 V ≤ V_{CC} ≤ 5.5 V			500	
			1.8 V ≤ V_{CC} ≤ 5.5 V			1000	
t_{SV}	CS to Status Valid	AC Test	4.5 V ≤ V_{CC} ≤ 5.5 V			250	ns
			2.7 V ≤ V_{CC} ≤ 5.5 V			250	
			2.5 V ≤ V_{CC} ≤ 5.5 V			500	
			1.8 V ≤ V_{CC} ≤ 5.5 V			1000	
t_{DF}	CS to DO in High Impedance	AC Test CS = V_{IL}	4.5 V ≤ V_{CC} ≤ 5.5 V			100	ns
			2.7 V ≤ V_{CC} ≤ 5.5 V			100	
			2.5 V ≤ V_{CC} ≤ 5.5 V			200	
			1.8 V ≤ V_{CC} ≤ 5.5 V			400	
t_{WP}	Write Cycle Time					10	ms
	Endurance	Number of Data Changes per Bit			100,000		Cycles

Instruction Set for the AT93C46

Instruction	SB	Op Code	Address x 8	Address x 16	Data x 8	Data x 16	Comments
READ	1	10	A_6-A_0	A_5-A_0			Reads data stored in memory, at specified address.
EWEN	1	00	11XXXXX	11XXXX			Write enable must precede all programming modes.
ERASE	1	11	A_6-A_0	A_5-A_0			Erase memory location A_n - A_0.
WRITE	1	01	A_6-A_0	A_5-A_0	D_7-D_0	D_{15}-D_0	Writes memory location A_n - A_0.
ERAL	1	00	10XXXXX	10XXXX			Erases all memory locations. Valid only at V_{CC} = 4.5 V to 5.5 V.
WRAL	1	00	01XXXXX	01XXXX	D_7-D_0	D_{15}-D_0	Writes all memory locations. Valid only at V_{CC} = 4.5 V to 5.5 V.
EWDS	1	00	00XXXXX	00XXXX			Disables all programming instructions.

Instruction Set for the AT93C57

Instruction	SB	Op Code	Address x 8	Address x 16	Data x 8	Data x 16	Comments
READ	1	10	A_7-A_0	A_6-A_0			Reads data stored in memory, at specified address.
EWEN	1	00	11XXXXXX	11XXXXX			Write enable must precede all programming modes.
ERASE	1	11	A_7-A_0	A_6-A_0			Erase memory location A_n - A_0.
WRITE	1	01	A_7-A_0	A_6-A_0	D_7-D_0	D_{15}-D_0	Writes memory location A_n - A_0.
ERAL	1	00	10XXXXXX	10XXXXX			Erases all memory locations. Valid only at V_{CC} = 4.5 V to 5.5 V.
WRAL	1	00	01XXXXXX	01XXXXX	D_7-D_0	D_{15}-D_0	Writes all memory locations. Valid only at V_{CC} = 4.5 V to 5.5 V.
EWDS	1	00	00XXXXXX	00XXXXX			Disables all programming instructions.

Instruction Set for the AT93C56 and AT93C66

Instruction	SB	Op Code	Address x 8	Address x 16	Data x 8	Data x 16	Comments
READ	1	10	A_8-A_0	A_7-A_0			Reads data stored in memory, at specified address.
EWEN	1	00	11XXXXXXX	11XXXXXX			Write enable must precede all programming modes.
ERASE	1	11	A_8-A_0	A_7-A_0			Erases memory location A_n - A_0.
WRITE	1	01	A_8-A_0	A_7-A_0	D_7-D_0	D_{15}-D_0	Writes memory location A_n - A_0.
ERAL	1	00	10XXXXXXX	10XXXXXX			Erases all memory locations. Valid only at V_{CC} = 4.5 V to 5.5 V.
WRAL	1	00	01XXXXXXX	01XXXXXX	D_7-D_0	D_{15}-D_0	Writes all memory locations. Valid when V_{CC} = 5.0 V ± 10% and Disable Register cleared.
EWDS	1	00	00XXXXXXX	00XXXXXX			Disables all programming instructions.

Functional Description

The AT93C46/56/57/66 is accessed via a simple and versatile three-wire serial communication interface. Device operation is controlled by seven instructions issued by the host processor. A valid instruction consists of a Start Bit (logic '1') followed by the appropriate Op Code and the desired memory Address location.

READ (READ): The Read (READ) instruction contains the Address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the serial output pin DO. Output data changes are synchronized with the rising edges of serial clock SK. It should be noted that a dummy bit (logic '0') precedes the 8- or 16-bit data output string.

ERASE/WRITE (EWEN): To assure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out. Please note that once in the Erase/Write Enable state, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or V_{CC} power is removed from the part.

ERASE (ERASE): The Erase (ERASE) instruction programs all bits in the specified memory location to the logical '1' state. The self-timed erase cycle starts once the ERASE instruction and address are decoded. The DO pin outputs the READY / BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). A logic '1' at pin DO indicates that the selected memory location has been erased, and the part is ready for another instruction.

WRITE (WRITE): The Write (WRITE) instruction contains the 8 or 16 bits of data to be written into the specified memory location. The self-timed programming cycle starts after the last bit of data is received at serial data input pin DI. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). A logic '0' at DO indicates that programming is still in progress. A logic '1' indicates that the memory location at the specified address has been written with the data pattern contained in the instruction and the part is ready for further instructions.

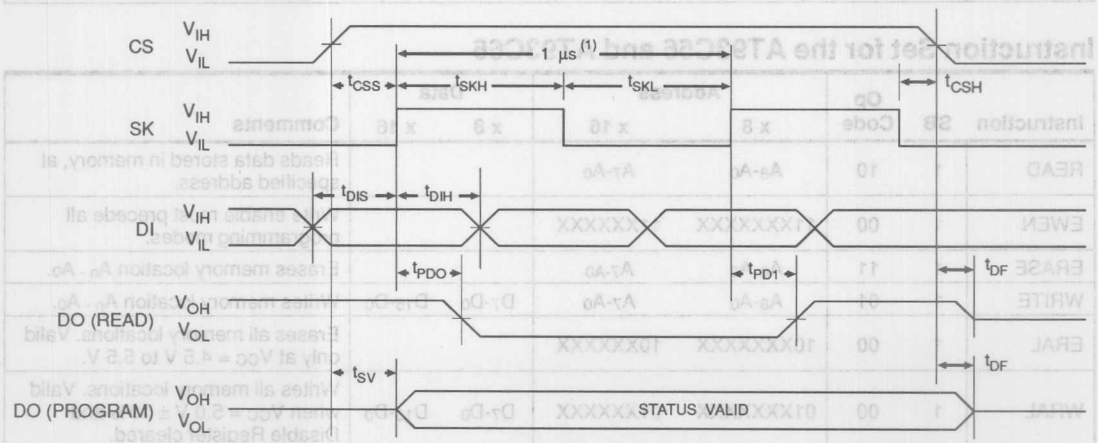
ERASE ALL (ERAL): The Erase All (ERAL) instruction programs every bit in the memory array to the logic '1' state and is primarily used for testing purposes. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). The ERAL instruction is valid only at $V_{CC} = 5.0\ V \pm 10\%$.

WRITE ALL (WRAL): The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). The WRAL instruction is valid only at $V_{CC} = 5.0\ V \pm 10\%$.

ERASE/WRITE DISABLE (EWDS): To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the READ instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

Timing Diagrams

Synchronous Data Timing



Note: 1. This is the minimum SK period.

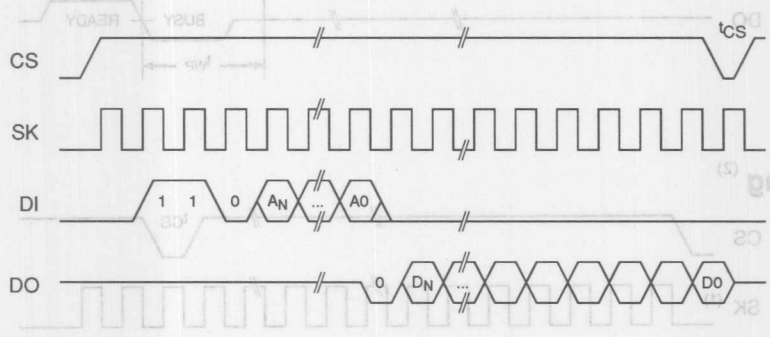
Organization Key for Timing Diagrams

	Density 1K		Density 2K		Density 4K	
I/O	x 8	x 16	x 8	x 16	x 8	x 16
A_N	A_6	A_5	A_8	A_7	A_8	A7
D_N	D_7	D15	D7	D15	D7	D15

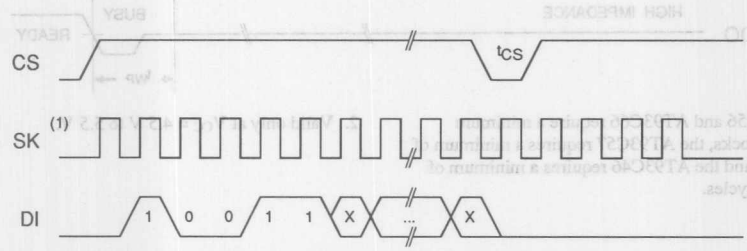
2

Timing Diagrams (Continued)

READ Timing

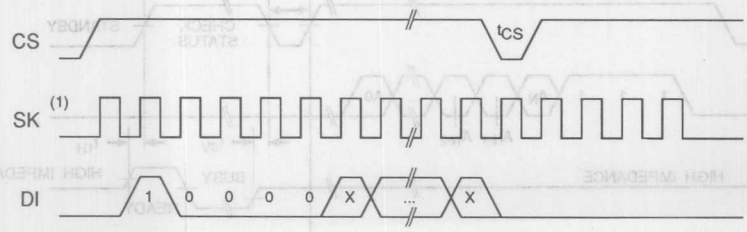


EWEN Timing



Note: 1. The AT93C56 and AT93C66 require a minimum of eleven clocks, the AT93C57 requires a minimum of ten clocks, and the AT93C46 requires a minimum of nine clock cycles.

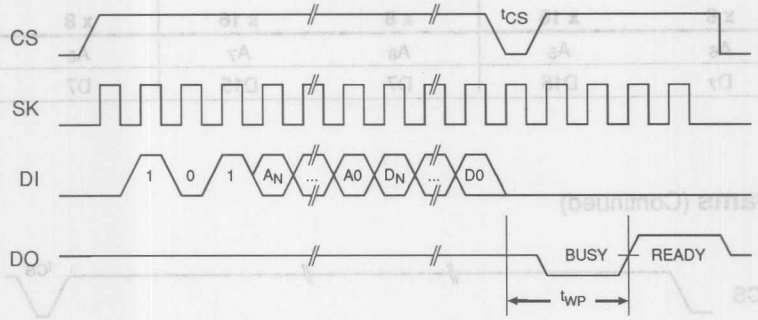
EWDS Timing



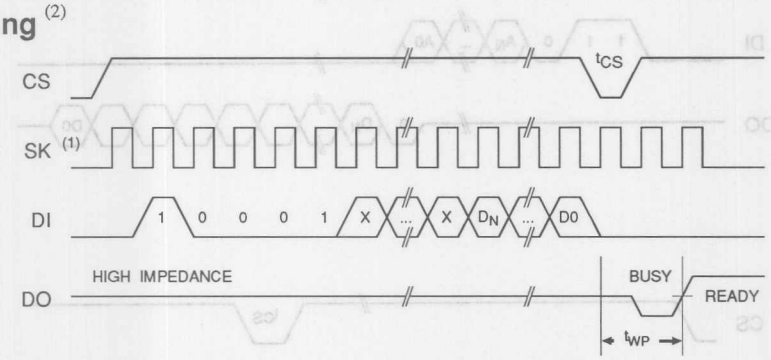
Note: 1. The AT93C56 and AT93C66 require a minimum of eleven clocks, the AT93C57 requires a minimum of ten clocks, and the AT93C46 requires a minimum of nine clock cycles.

Timing Diagrams (Continued)

WRITE Timing



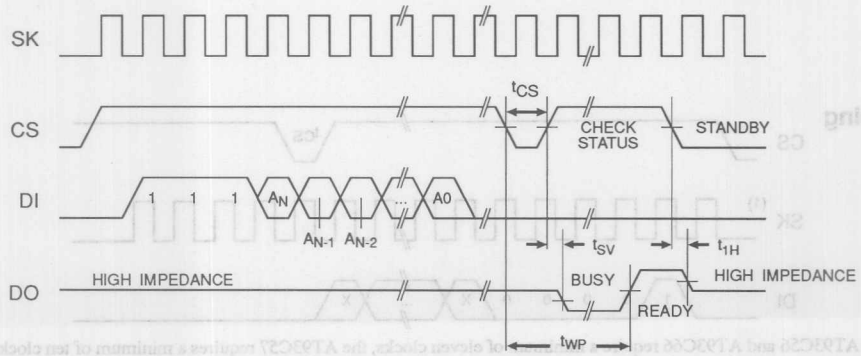
WRAL Timing (2)



Notes: 1. The AT93C56 and AT93C66 require a minimum of eleven clocks, the AT93C57 requires a minimum of ten clocks, and the AT93C46 requires a minimum of nine clock cycles.

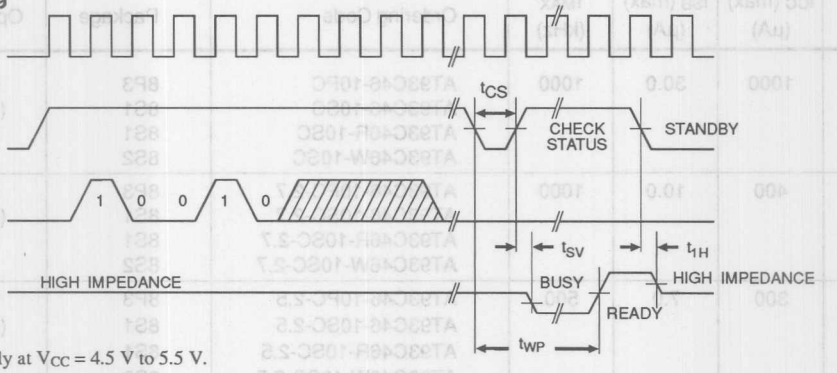
2. Valid only at V_{CC} = 4.5 V to 5.5 V.

ERASE Timing



Timing Diagrams (Continued)

TERAL Timing [1]



Note: 1. Valid only at V_{CC} = 4.5 V to 5.5 V.

Ordering Information

t_{WP} (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	1000	30.0	1000	AT93C46-10PC AT93C46-10SC AT93C46R-10SC AT93C46W-10SC	8P3 8S1 8S1 8S2	Commercial (0°C to 70°C)
10	400	10.0	1000	AT93C46-10PC-2.7 AT93C46-10SC-2.7 AT93C46R-10SC-2.7 AT93C46W-10SC-2.7	8P3 8S1 8S1 8S2	Commercial (0°C to 70°C)
10	300	7.0	500	AT93C46-10PC-2.5 AT93C46-10SC-2.5 AT93C46R-10SC-2.5 AT93C46W-10SC-2.5	8P3 8S1 8S1 8S2	Commercial (0°C to 70°C)
10	40	0.1	250	AT93C46-10PC-1.8 AT93C46-10SC-1.8 AT93C46R-10SC-1.8 AT93C46W-10SC-1.8	8P3 8S1 8S1 8S2	Commercial (0°C to 70°C)
10	1000	30.0	1000	AT93C46-10PI AT93C46-10SI AT93C46R-10SI AT93C46W-10SI	8P3 8S1 8S1 8S2	Industrial (-40°C to 85°C)
10	400	10.0	1000	AT93C46-10PI-2.7 AT93C46-10SI-2.7 AT93C46R-10SI-2.7 AT93C46W-10SI-2.7	8P3 8S1 8S1 8S2	Industrial (-40°C to 85°C)
10	300	7.0	500	AT93C46-10PI-2.5 AT93C46-10SI-2.5 AT93C46R-10SI-2.5 AT93C46W-10SI-2.5	8P3 8S1 8S1 8S2	Industrial (-40°C to 85°C)
10	40	0.1	250	AT93C46-10PI-1.8 AT93C46-10SI-1.8 AT93C46R-10SI-1.8 AT93C46W-10SI-1.8	8P3 8S1 8S1 8S2	Industrial (-40°C to 85°C)
10	1000	30.0	1000	AT93C46-10PM	8P3	Military (-55°C to 125°C)

Ordering Information

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8S2	8 Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
Options	
Blank	Standard Device (4.5 V to 5.5 V)
-2.7	Low Voltage (2.7 V to 5.5 V)
-2.5	Low Voltage (2.5 V to 5.5 V)
-1.8	Low Voltage (1.8 V to 5.5 V)
R	Rotated Pinout

Ordering Information

t_{WP} (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	1000	30.0	1000	AT93C56-10PC AT93C56-10SC AT93C56W-10SC	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	400	10.0	1000	AT93C56-10PC-2.7 AT93C56-10SC-2.7 AT93C56W-10SC-2.7	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	300	7.0	500	AT93C56-10PC-2.5 AT93C56-10SC-2.5 AT93C56W-10SC-2.5	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	40	0.1	250	AT93C56-10PC-1.8 AT93C56-10SC-1.8 AT93C56W-10SC-1.8	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	1000	30.0	1000	AT93C56-10PI AT93C56-10SI AT93C56W-10SI	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	400	10.0	1000	AT93C56-10PI-2.7 AT93C56-10SI-2.7 AT93C56W-10SI-2.7	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	300	7.0	500	AT93C56-10PI-2.5 AT93C56-10SI-2.5 AT93C56W-10SI-2.5	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	40	0.1	250	AT93C56-10PI-1.8 AT93C56-10SI-1.8 AT93C56W-10SI-1.8	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	1000	30.0	1000	AT93C56-10PM	8P3	Military (-55°C to 125°C)

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8S2	8 Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
Options	
Blank	Standard Device (4.5 V to 5.5 V)
-2.7	Low Voltage (2.7 V to 5.5 V)
-2.5	Low Voltage (2.5 V to 5.5 V)
-1.8	Low Voltage (1.8 V to 5.5 V)

Ordering Information

t_{WP} (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	1000	30.0	1000	AT93C57-10PC AT93C57-10SC AT93C57W-10SC	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	400	10.0	1000	AT93C57-10PC-2.7 AT93C57-10SC-2.7 AT93C57W-10SC-2.7	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	300	7.0	500	AT93C57-10PC-2.5 AT93C57-10SC-2.5 AT93C57W-10SC-2.5	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	40	0.1	250	AT93C57-10PC-1.8 AT93C57-10SC-1.8 AT93C57W-10SC-1.8	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	1000	30.0	1000	AT93C57-10PI AT93C57-10SI AT93C57W-10SI	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	400	10.0	1000	AT93C57-10PI-2.7 AT93C57-10SI-2.7 AT93C57W-10SI-2.7	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	300	7.0	500	AT93C57-10PI-2.5 AT93C57-10SI-2.5 AT93C57W-10SI-2.5	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	40	0.1	250	AT93C57-10PI-1.8 AT93C57-10SI-1.8 AT93C57W-10SI-1.8	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	1000	30.0	1000	AT93C57-10PM	8P3	Military (-55°C to 125°C)

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8S2	8 Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
Options	
Blank	Standard Device (4.5 V to 5.5 V)
-2.7	Low Voltage (2.7 V to 5.5 V)
-2.5	Low Voltage (2.5 V to 5.5 V)
-1.8	Low Voltage (1.8 V to 5.5 V)

Ordering Information

t_{WP} (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	1000	30.0	1000	AT93C66-10PC AT93C66-10SC AT93C66W-10SC	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	400	10.0	1000	AT93C66-10PC-2.7 AT93C66-10SC-2.7 AT93C66W-10SC-2.7	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	300	7.0	500	AT93C66-10PC-2.5 AT93C66-10SC-2.5 AT93C66W-10SC-2.5	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	40	0.1	250	AT93C66-10PC-1.8 AT93C66-10SC-1.8 AT93C66W-10SC-1.8	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	1000	30.0	1000	AT93C66-10PI AT93C66-10SI AT93C66W-10SI	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	400	10.0	1000	AT93C66-10PI-2.7 AT93C66-10SI-2.7 AT93C66W-10SI-2.7	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	300	7.0	500	AT93C66-10PI-2.5 AT93C66-10SI-2.5 AT93C66W-10SI-2.5	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	40	0.1	250	AT93C66-10PI-1.8 AT93C66-10SI-1.8 AT93C66W-10SI-1.8	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	1000	30.0	1000	AT93C66-10PM	8P3	Military (-55°C to 125°C)

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8S2	8 Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
Options	
Blank	Standard Device (4.5 V to 5.5 V)
-2.7	Low Voltage (2.7 V to 5.5 V)
-2.5	Low Voltage (2.5 V to 5.5 V)
-1.8	Low Voltage (1.8 V to 5.5 V)

4-Wire Serial CMOS E²PROMs

1K (128 x 8 or 64 x 16)

2K (256 x 8 or 128 x 16)

4K (512 x 8 or 256 x 16)

- **Low Voltage and Standard Voltage Operation**
  - **5.0 V (Vcc = 4.5 V to 5.5 V)**
  - **3.0 V (Vcc = 2.7 V to 5.5 V)**
  - **2.5 V (Vcc = 2.5 V to 5.5 V)**
  - **2.0 V (Vcc = 1.8 V to 5.5 V)**
- **User Selectable Internal Organization**
  - **1K: 128 x 8 or 64 x 16**
  - **2K: 256 x 8 or 128 x 16**
  - **4K: 512 x 8 or 256 x 16**
- **Four-Wire Serial Interface**
- **Self-Timed Write Cycle (10 ms Max)**
- **High Reliability**
  - **Endurance: 100,000 Cycles**
  - **Data Retention: 100 Years**
- **Eight-Pin PDIP and EIAJ SOIC Packages**

Description

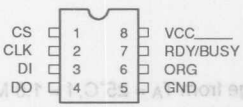
The AT59C11/22/13 provides 1024/2048/4096 bits of serial E²PROM (Electrically Erasable Programmable Read Only Memory) organized as 64/128/256 words of 16 bits each, when the ORG Pin is connected to Vcc and 128/256/512 words of eight bits each when it is tied to ground. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT59C11/22/13 is available in space saving eight-pin PDIP and eight-pin EIAJ SOIC packages.

The AT59C11/22/13 is enabled through the Chip Select pin (CS), and accessed via a four-wire serial interface consisting of Data Input (DI), Data Output (DO), and Clock (CLK). Upon receiving a READ instruction at DI, the address is decoded and the data is clocked out serially on the data output pin DO, the WRITE cycle is completely self-timed and no separate ERASE cycle is required before WRITE. The WRITE cycle is only enabled when the part is in the ERASE/WRITE ENABLE state. Ready/$\overline{\text{Busy}}$ status can be monitered upon completion of a programming operation by polling the Ready/$\overline{\text{Busy}}$ pin.

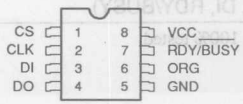
Atmel's E²PROMs are designed and tested for applications requiring extended endurance. Devices in this family are guaranteed for 100,000 ERASE/WRITE cycles and 100-year data retention. The AT59C11/22/13 is available in 5.0 V ± 10%, 2.7 V to 5.5 V, 2.5 V to 5.5 V, and 1.8 V to 5.5 V versions.

Pin Configurations

Pin Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
Vcc	Power Supply
ORG	Internal Organization
RDY/$\overline{\text{BUSY}}$	Status Output



8-Pin PDIP



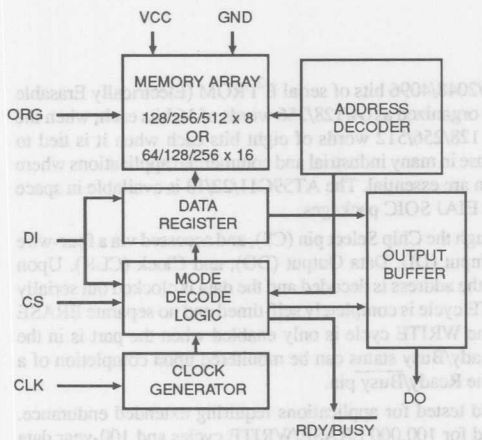
8-Pin SOIC

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0 V to +7.0 V
Maximum Operating Voltage	6.25 V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram (1)



Note:
1. When the ORG pin is connected to V_{CC}, the x 16 organization is selected. When it is connected to ground, the x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the x 16 organization.

Pin Capacitance (1)

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +5.0 V (unless otherwise noted)

	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (DO)	5	pF	V_{OUT} = 0 V
C_{IN}	Input Capacitance (CS, CLK, DI, RDY/$\overline{BUSY}$)	5	pF	V_{IN} = 0 V

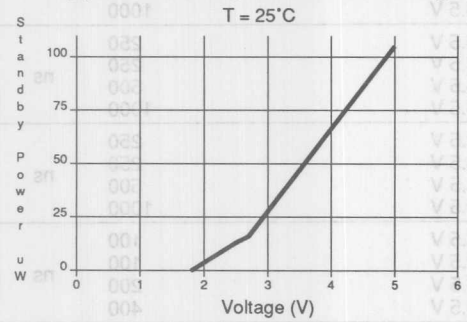
Note: 1. This parameter is characterized and is not 100% tested.

D.C. Characteristics

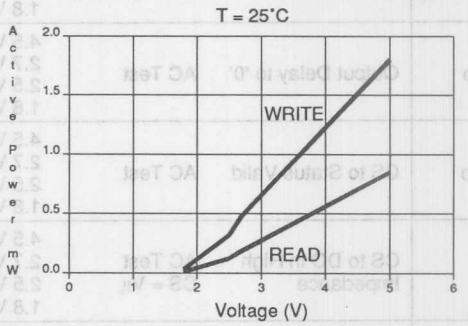
Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +1.8 V to +5.5 V, T_{AC} = 0°C to + 70°C, V_{CC} = +1.8 V to +5.5 V (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC1} (1)	Supply Voltage			1.8	5.0	5.5	V
V_{CC2}	Supply Voltage			2.5	5.0	5.5	V
V_{CC3}	Supply Voltage			2.7	5.0	5.5	V
V_{CC4}	Supply Voltage			4.5	5.0	5.5	V
I_{CC}	Supply Current	V_{CC} = 5.0 V	READ at 1.0 MHz		0.2	0.5	mA
			WRITE at 1.0 MHz		0.4	1.0	mA
I_{SB1} (1)	Standby Current	V_{CC} = 1.8 V	CS = 0 V		0.0	0.1	µA
I_{SB2}	Standby Current	V_{CC} = 2.5 V	CS = 0 V		5.0	7.0	µA
I_{SB3}	Standby Current	V_{CC} = 2.7 V	CS = 0 V		6.0	10.0	µA
I_{SB4}	Standby Current	V_{CC} = 5.0 V	CS = 0 V		21.0	30.0	µA
I_{IL}	Input Leakage	V_{IN} = 0 V to V_{CC}			0.1	1.0	µA
I_{OL}	Output Leakage	V_{IN} = 0 V to V_{CC}			0.1	1.0	µA
V_{IL1} (2) V_{IH1} (2)	Input Low Voltage Input High Voltage	4.5 V ≤ V_{CC} ≤ 5.5 V		-0.1 2.0		0.8 V_{CC}+1	V
V_{IL2} (2) V_{IH2} (2)	Input Low Voltage Input High Voltage	1.8 V ≤ V_{CC} ≤ 5.5 V		0.0 1.4		0.4 V_{CC}+1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage	4.5 V ≤ V_{CC} ≤ 5.5 V				0.4 2.4	V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage	1.8 V ≤ V_{CC} ≤ 5.5 V				0.2 V_{CC}-0.2	V

Typical Standby Power vs. Voltage (3)



Typical Active Power vs. Voltage (3)



Notes: 1. This parameter is preliminary and Atmel may change the specifications upon further characterization.
2. V_{IL} min and V_{IH} max are reference only and are not tested.
3. These graphs are for reference only and are not guarenteed by test.

A.C. Characteristics

Applicable over recommended operating range from T_A = -40°C to + 85°C, V_{CC} = As Specified, CL = 1 TTL Gate and 100 pF (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
f_{CLK}	CLK Clock Frequency		4.5 V ≤ Vcc ≤ 5.5 V	0		1	MHz
			2.7 V ≤ Vcc ≤ 5.5 V	0		1	
			2.5 V ≤ Vcc ≤ 5.5 V	0		0.5	
			1.8 V ≤ Vcc ≤ 5.5 V	0		0.25	
t_{CKH}	CLK High Time		4.5 V ≤ Vcc ≤ 5.5 V	250			ns
			2.7 V ≤ Vcc ≤ 5.5 V	250			
			2.5 V ≤ Vcc ≤ 5.5 V	500			
			1.8 V ≤ Vcc ≤ 5.5 V	1000			
t_{CKL}	CLK Low Time		4.5 V ≤ Vcc ≤ 5.5 V	250			ns
			2.7 V ≤ Vcc ≤ 5.5 V	250			
			2.5 V ≤ Vcc ≤ 5.5 V	500			
			1.8 V ≤ Vcc ≤ 5.5 V	1000			
t_{CS}	Minimum CS Low Time		4.5 V ≤ Vcc ≤ 5.5 V	250			ns
			2.7 V ≤ Vcc ≤ 5.5 V	250			
			2.5 V ≤ Vcc ≤ 5.5 V	500			
			1.8 V ≤ Vcc ≤ 5.5 V	1000			
t_{CSS}	CS Setup Time	Relative to SK	4.5 V ≤ Vcc ≤ 5.5 V	50			ns
			2.7 V ≤ Vcc ≤ 5.5 V	50			
			2.5 V ≤ Vcc ≤ 5.5 V	100			
			1.8 V ≤ Vcc ≤ 5.5 V	200			
t_{DIS}	DI Setup Time	Relative to SK	4.5 V ≤ Vcc ≤ 5.5 V	100			ns
			2.7 V ≤ Vcc ≤ 5.5 V	100			
			2.5 V ≤ Vcc ≤ 5.5 V	200			
			1.8 V ≤ Vcc ≤ 5.5 V	400			
t_{CSH}	CS Hold Time	Relative to SK		0			ns
t_{DIH}	DI Hold Time	Relative to SK	4.5 V ≤ Vcc ≤ 5.5 V	100			ns
			2.7 V ≤ Vcc ≤ 5.5 V	100			
			2.5 V ≤ Vcc ≤ 5.5 V	200			
			1.8 V ≤ Vcc ≤ 5.5 V	400			
t_{PD1}	Output Delay to '1'	AC Test	4.5 V ≤ Vcc ≤ 5.5 V			250	ns
			2.7 V ≤ Vcc ≤ 5.5 V			250	
			2.5 V ≤ Vcc ≤ 5.5 V			500	
			1.8 V ≤ Vcc ≤ 5.5 V			1000	
t_{PD0}	Output Delay to '0'	AC Test	4.5 V ≤ Vcc ≤ 5.5 V			250	ns
			2.7 V ≤ Vcc ≤ 5.5 V			250	
			2.5 V ≤ Vcc ≤ 5.5 V			500	
			1.8 V ≤ Vcc ≤ 5.5 V			1000	
t_{RBD}	CS to Status Valid	AC Test	4.5 V ≤ Vcc ≤ 5.5 V			250	ns
			2.7 V ≤ Vcc ≤ 5.5 V			250	
			2.5 V ≤ Vcc ≤ 5.5 V			500	
			1.8 V ≤ Vcc ≤ 5.5 V			1000	
t_{CZ}	CS to DO in High Impedance	AC Test CS = V_{IL}	4.5 V ≤ Vcc ≤ 5.5 V			100	ns
			2.7 V ≤ Vcc ≤ 5.5 V			100	
			2.5 V ≤ Vcc ≤ 5.5 V			200	
			1.8 V ≤ Vcc ≤ 5.5 V			400	
t_{WC}	Write Cycle Time					10	ms
	Endurance	Number of Data Changes per Bit			100,000		Cycles

Instruction Set for the AT59C11

Instruction	SB	Op Code	Address x 8	Address x 16	Data x 8	Data x 16	Comments
READ	1	10XX	A_6-A_0	A_5-A_0			Reads data stored in memory, at specified address.
EWEN	1	0011	XXXXXXX	XXXXXX			Write enable must precede all programming modes.
WRITE	1	X1XX	A_6-A_0	A_5-A_0	D_7-D_0	D_{15}-D_0	Writes memory location A_n - A_0.
ERAL	1	0010	XXXXXXX	XXXXXX			Erases all memory locations. Valid only at V_{CC} = 4.5 V to 5.5 V.
WRAL	1	0001	XXXXXXX	XXXXXX	D_7-D_0	D_{15}-D_0	Writes all memory locations. Valid only at V_{CC} = 4.5 V to 5.5 V.
EWDS	1	0000	XXXXXXX	XXXXXX			Disables all programming instructions.

Instruction Set for the AT59C22

Instruction	SB	Op Code	Address x 8	Address x 16	Data x 8	Data x 16	Comments
READ	1	10XX	A_7-A_0	A_6-A_0			Reads data stored in memory, at specified address.
EWEN	1	0011	XXXXXXXX	XXXXXXX			Write enable must precede all programming modes.
WRITE	1	X1XX	A_7-A_0	A_6-A_0	D_7-D_0	D_{15}-D_0	Writes memory location A_n - A_0.
ERAL	1	0010	XXXXXXXX	XXXXXXX			Erases all memory locations. Valid only at V_{CC} = 4.5 V to 5.5 V.
WRAL	1	0001	XXXXXXXX	XXXXXXX	D_7-D_0	D_{15}-D_0	Writes all memory locations. Valid when V_{CC} = 5.0 V ± 10% and Disable Register cleared.
EWDS	1	0000	XXXXXXXX	XXXXXXX			Disables all programming instructions.

Instruction Set for the AT59C13

Instruction	SB	Op Code	Address x 8	Address x 16	Data x 8	Data x 16	Comments
READ	1	10XX	A_8-A_0	A_7-A_0			Reads data stored in memory, at specified address.
EWEN	1	0011	XXXXXXXXX	XXXXXXXX			Write enable must precede all programming modes.
WRITE	1	X1XX	A_8-A_0	A_7-A_0	D_7-D_0	D_{15}-D_0	Writes memory location A_n - A_0.
ERAL	1	0010	XXXXXXXXX	XXXXXXXX			Erases all memory locations. Valid only at V_{CC} = 4.5 V to 5.5 V.
WRAL	1	0001	XXXXXXXXX	XXXXXXXX	D_7-D_0	D_{15}-D_0	Writes all memory locations. Valid when V_{CC} = 5.0 V ± 10% and Disable Register cleared.
EWDS	1	0000	XXXXXXXXX	XXXXXXXX			Disables all programming instructions.

Functional Description

The AT59C11/22/13 are accessed via a simple and versatile four-wire serial communication interface. Device operation is controlled by six instructions issued by the host processor. A valid instruction consists of a Start Bit (logic '1') followed by the appropriate Op Code and the desired memory Address location.

READ (READ): The Read (READ) instruction contains the Address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the serial output pin DO. Output data changes are synchronized with the rising edges of serial clock CLK. It should be noted that a dummy bit (logic '0') precedes the 8- or 16-bit data output string.

ERASE/WRITE (EWEN): To assure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out. Please note that once in the Erase/Write Enable state, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or V_{CC} power is removed from the part.

WRITE (WRITE): The Write (WRITE) instruction contains the 8 or 16 bits of data to be written into the specified memory location. The self-timed programming cycle starts after the last bit of data is received at serial data input pin DI. The Ready/$\overline{\text{Busy}}$ status of the AT59C11/22/13 can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin. A logic '0' at RDY/$\overline{\text{BUSY}}$ indicates that programming is still in progress. A logic '1' indicates that the memory location at the specified address has been written with the data pattern contained in the instruction and the part is ready for further instructions.

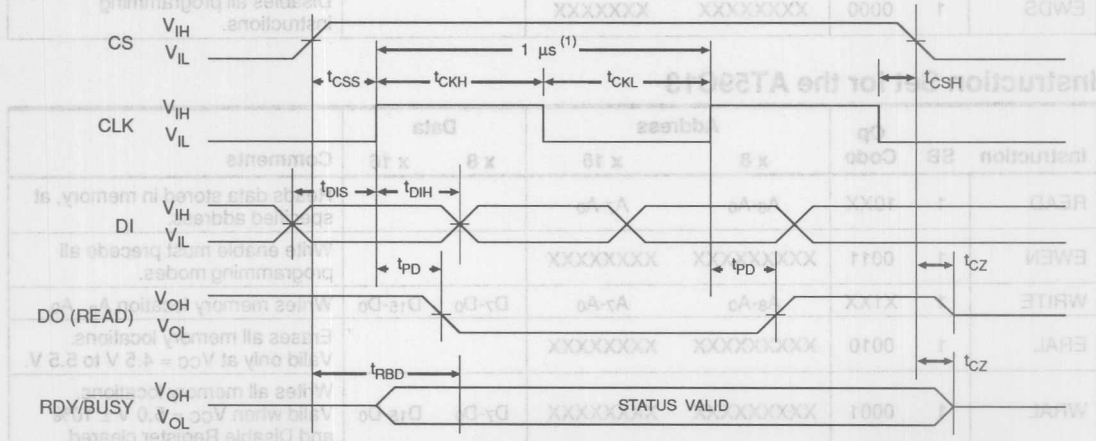
ERASE ALL (ERAL): The Erase All (ERAL) instruction programs every bit in the memory array to the logic '1' state and is primarily used for testing purposes. The Ready/$\overline{\text{Busy}}$ status of the AT59C11/22/13 can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin. The ERAL instruction is valid only at V_{CC} = 5.0 V ± 10%.

WRITE ALL (WRAL): The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The Ready/$\overline{\text{Busy}}$ status of the AT59C11/22/13 can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin. The WRAL instruction is valid only at V_{CC} = 5.0 V ± 10%.

ERASE/WRITE DISABLE (EWDS): To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the READ in-

Timing Diagrams

Synchronous Data Timing

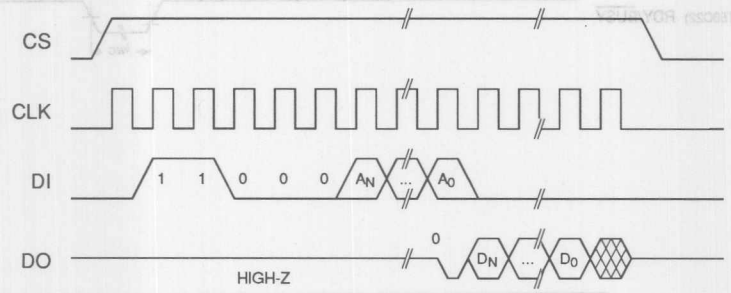


Note: 1. This is the minimum CLK period.

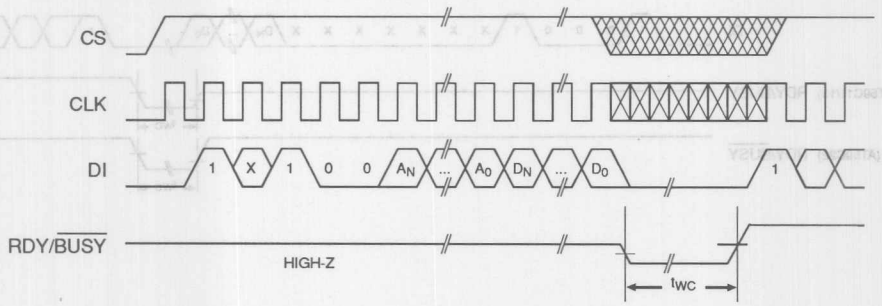
Organization Key for Timing Diagrams

	Density 1K		Density 2K		Density 4K	
I/O	x 8	x 16	x 8	x 16	x 8	x 16
A_N	A_6	A_5	A_8	A_7	A_8	A7
D_N	D_7	D15	D7	D15	D7	D15

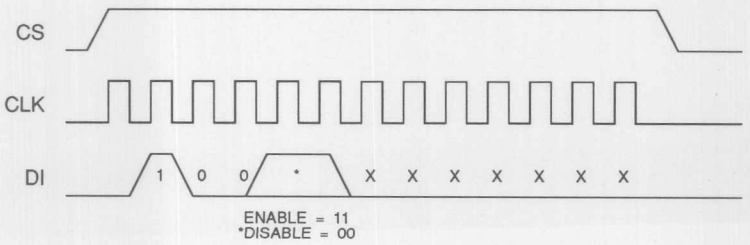
READ Timing



WRITE Timing

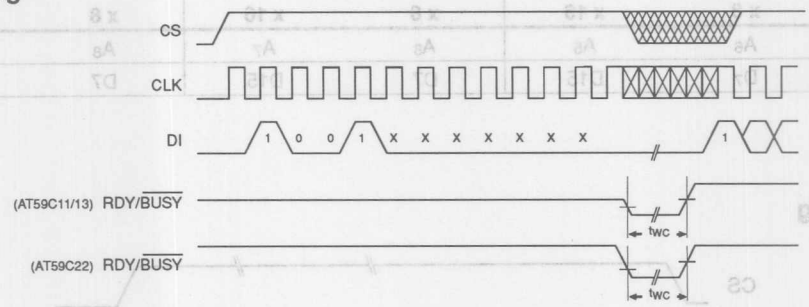


EWEN/EWDS Timing

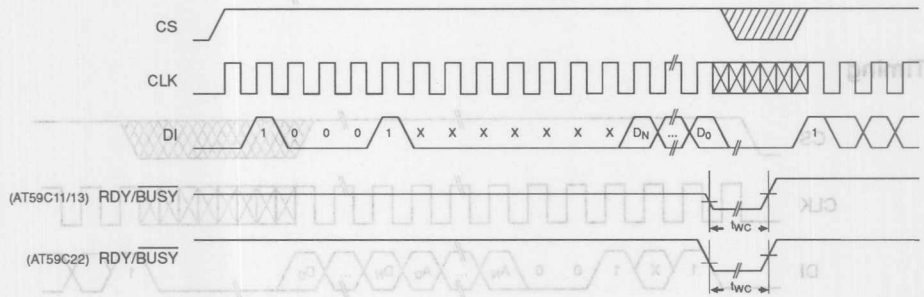


Timing Diagrams (Continued)

ERAL Timing



WRAL Timing



Ordering Information

t_{WC} (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	1000	30.0	1000	AT59C11-10PC AT59C11W-10SC	8P3 8S2	Commercial (0°C to 70°C)
10	400	10.0	1000	AT59C11-10PC-2.7 AT59C11W-10SC-2.7	8P3 8S2	Commercial (0°C to 70°C)
10	300	7.0	500	AT59C11-10PC-2.5 AT59C11W-10SC-2.5	8P3 8S2	Commercial (0°C to 70°C)
10	40	0.1	250	AT59C11-10PC-1.8 AT59C11W-10SC-1.8	8P3 8S2	Commercial (0°C to 70°C)
10	1000	30.0	1000	AT59C11-10PI AT59C11W-10SI	8P3 8S2	Industrial (-40°C to 85°C)
10	400	10.0	1000	AT59C11-10PI-2.7 AT59C11W-10SI-2.7	8P3 8S2	Industrial (-40°C to 85°C)
10	300	7.0	500	AT59C11-10PI-2.5 AT59C11W-10SI-2.5	8P3 8S2	Industrial (-40°C to 85°C)
10	40	0.1	250	AT59C11-10PI-1.8 AT59C11W-10SI-1.8	8P3 8S2	Industrial (-40°C to 85°C)

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S2	8 Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
Options	
Blank	Standard Device (4.5 V to 5.5 V)
-2.7	Low Voltage (2.7 V to 5.5 V)
-2.5	Low Voltage (2.5 V to 5.5 V)
-1.8	Low Voltage (1.8 V to 5.5 V)

Ordering Information

t_{WC} (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	1000	30.0	1000	AT59C22-10PC AT59C22W-10SC	8P3 8S2	Commercial (0°C to 70°C)
10	400	10.0	1000	AT59C22-10PC-2.7 AT59C22W-10SC-2.7	8P3 8S2	Commercial (0°C to 70°C)
10	300	7.0	500	AT59C22-10PC-2.5 AT59C22W-10SC-2.5	8P3 8S2	Commercial (0°C to 70°C)
10	40	0.1	250	AT59C22-10PC-1.8 AT59C22W-10SC-1.8	8P3 8S2	Commercial (0°C to 70°C)
10	1000	30.0	1000	AT59C22-10PI AT59C22W-10SI	8P3 8S2	Industrial (-40°C to 85°C)
10	400	10.0	1000	AT59C22-10PI-2.7 AT59C22W-10SI-2.7	8P3 8S2	Industrial (-40°C to 85°C)
10	300	7.0	500	AT59C22-10PI-2.5 AT59C22W-10SI-2.5	8P3 8S2	Industrial (-40°C to 85°C)
10	40	0.1	250	AT59C22-10PI-1.8 AT59C22W-10SI-1.8	8P3 8S2	Industrial (-40°C to 85°C)

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8 Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
Options	
Blank	Standard Device (4.5 V to 5.5 V)
-2.7	Low Voltage (2.7 V to 5.5 V)
-2.5	Low Voltage (2.5 V to 5.5 V)
-1.8	Low Voltage (1.8 V to 5.5 V)

Ordering Information

t_{WC} (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	1000	30.0	1000	AT59C13-10PC AT59C13W-10SC	8P3 8S2	Commercial (0°C to 70°C)
10	400	10.0	1000	AT59C13-10PC-2.7 AT59C13W-10SC-2.7	8P3 8S2	Commercial (0°C to 70°C)
10	300	7.0	500	AT59C13-10PC-2.5 AT59C13W-10SC-2.5	8P3 8S2	Commercial (0°C to 70°C)
10	40	0.1	250	AT59C13-10PC-1.8 AT59C13W-10SC-1.8	8P3 8S2	Commercial (0°C to 70°C)
10	1000	30.0	1000	AT59C13-10PI AT59C13W-10SI	8P3 8S2	Industrial (-40°C to 85°C)
10	400	10.0	1000	AT59C13-10PI-2.7 AT59C13W-10SI-2.7	8P3 8S2	Industrial (-40°C to 85°C)
10	300	7.0	500	AT59C13-10PI-2.5 AT59C13W-10SI-2.5	8P3 8S2	Industrial (-40°C to 85°C)
10	40	0.1	250	AT59C13-10PI-1.8 AT59C13W-10SI-1.8	8P3 8S2	Industrial (-40°C to 85°C)

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8 Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
Options	
Blank	Standard Device (4.5 V to 5.5 V)
-2.7	Low Voltage (2.7 V to 5.5 V)
-2.5	Low Voltage (2.5 V to 5.5 V)
-1.8	Low Voltage (1.8 V to 5.5 V)

Operation Range	Package	Ordering Code	fMAX (kHz)	Isb (max) (µA)	Icc (max) (mA)	Vcc
Commercial (0°C to 70°C)	8P3 8S2	AT89C13-10PC AT89C13-10SC	1000	30.0	1000	10
Commercial (0°C to 70°C)	8P3 8S2	AT89C13-10PC-2.7 AT89C13-10SC-2.7	1000	10.0	400	10
Commercial (0°C to 70°C)	8P3 8S2	AT89C13-10PC-2.5 AT89C13-10SC-2.5	500	7.0	300	10
Commercial (0°C to 70°C)	8P3 8S2	AT89C13-10PC-1.8 AT89C13-10SC-1.8	250	0.1	40	10
Industrial (-40°C to 85°C)	8P3 8S2	AT89C13-10PI AT89C13-10SI	1000	30.0	1000	10
Industrial (-40°C to 85°C)	8P3 8S2	AT89C13-10PI-2.7 AT89C13-10SI-2.7	1000	10.0	400	10
Industrial (-40°C to 85°C)	8P3 8S2	AT89C13-10PI-2.5 AT89C13-10SI-2.5	500	7.0	300	10
Industrial (-40°C to 85°C)	8P3 8S2	AT89C13-10PI-1.8 AT89C13-10SI-1.8	250	0.1	40	10

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8 Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
Options	
Blank	Standard Device (4.5 V to 5.5 V)
-2.7	Low Voltage (2.7 V to 5.5 V)
-2.5	Low Voltage (2.5 V to 5.5 V)
-1.8	Low Voltage (1.8 V to 5.5 V)

4K (512 x 8) CMOS E²PROM

- **Fast Read Access Time - 150 ns**
- **Fast Byte Write - 200 µs or 1 ms**
- **Self-Timed Byte Write Cycle**
  - **Internal Address and Data Latches**
  - **Internal Control Timer**
  - **Automatic Clear Before Write**
- **Direct Microprocessor Control**
  - **DATA POLLING**
- **Low Power**
  - **30 mA Active Current**
  - **100 µa CMOS Standby Current**
- **High Reliability**
  - **Endurance: 10^4 or 10^5 cycles**
  - **Data Retention: 10 years**
- **5 V ± 10% Supply**
- **CMOS & TTL Compatible Inputs and Outputs**
- **JEDEC Approved Byte Wide Pinout**
- **Full Military, Commercial, and Industrial Temperature Ranges**

Description

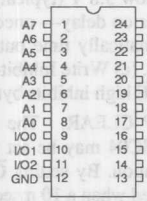
The AT28C04 is a low-power, high-performance Electrically Erasable and Programmable Read Only Memory with easy to use features. The AT28C04 is a 4K memory organized as 512 words x 8 bits. The device is manufactured with Atmel's reliable nonvolatile CMOS technology.

The AT28C04 is accessed like a static RAM for the read or write cycles without the need of external components. During a byte write, the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. The end of a write cycle can be determined by $\overline{DATA}$ polling of I/O_7. Once the end of a write cycle has been detected, a new access for a read or a write can begin.

The CMOS technology offers fast access times of 150 ns at low power dissipation. When the chip is deselected the standby current is less than 100 µA. Atmel's 28C04 has additional features to ensure high quality and manufacturability, including internal error correction for extended endurance and for improved data retention characteristics.

Pin Configurations

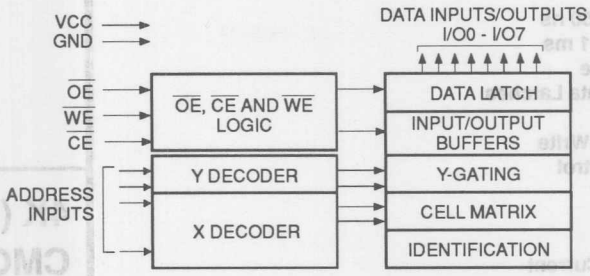
Pin Name	Function
A0 - A8	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect





Note: PLCC package pins 1 and 17 are DON'T CONNECT.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6 V to +6.25 V
All Output Voltages with Respect to Ground	-0.6 V to V_{CC} +0.6 V
Voltage on $\overline{OE}$ with Respect to Ground	-0.6 V to +13.5 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: The AT28C04 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers increased flexibility in preventing bus contention.

BYTE WRITE: Writing data into the AT28C04 is similar to writing into a Static RAM. A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{OE}$ high and $\overline{CE}$ or $\overline{WE}$ low (respectively) initiates a byte write. The address location is latched on the last falling edge of $\overline{WE}$ (or $\overline{CE}$); the new data is latched on the first rising edge. Internally, the device performs a self-clear before write. Once a byte write has been started, it will automatically time itself to completion.

FAST BYTE WRITE: The AT28C04F offers a byte write time of 200 µs maximum. This feature allows the entire device to be rewritten in 0.1 seconds.

$\overline{DATA}$ POLLING: The AT28C04 provides $\overline{DATA}$ POLLING to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the complement of that data for I/O_7 (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

WRITE PROTECTION: Inadvertent writes to the device are protected against in the following ways. (a) Vcc sense— if Vcc is below 3.8 V (typical) the write function is inhibited. (b) Vcc power on delay— once Vcc has reached 3.8 V the device will automatically time out 5 ms (typical) before allowing a byte write. (c) Write Inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits byte write cycles.

CHIP CLEAR: The contents of the entire memory of the AT28C04 may be set to the high state by the CHIP CLEAR operation. By setting $\overline{CE}$ low and $\overline{OE}$ to 12 volts, the chip is cleared when a 10 msec low pulse is applied to $\overline{WE}$.

D.C. and A.C. Operating Range

		AT28C04-15	AT28C04-20	AT28C04-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 10%	5 V ± 10%	5 V±10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write(2)	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X(1)	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H (3)	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.
3. $V_H = 12.0\ V \pm 0.5\ V$.

D.C. Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	$V_{IN} = 0\ V$ to $V_{CC} + 1\ V$			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$=0V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE} = V_{CC}$-0.3 V to $V_{CC} + 1.0\ V$			100	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0 V to $V_{CC} + 1.0\ V$	Com.		2	mA
			Ind., Mil.		3	mA
I_{CC}	V_{CC} Active Current A.C.	f = 5 MHz; I_{OUT} = 0 mA $\overline{CE} = V_{IL}$	Com.		30	mA
			Ind., Mil.		45	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1\ mA$			.4	V
V_{OH}	Output High Voltage	$I_{OH} = -400\ µA$		2.4		V

Pin Capacitance (f = 1 MHz, T = 25°C) (1)

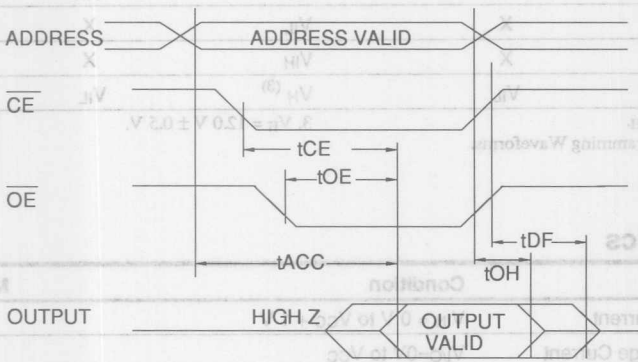
	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	$V_{IN} = 0\ V$
C_{OUT}	8	12	pF	$V_{OUT} = 0\ V$

Note: 1. This parameter is characterized and is not 100% tested.

A.C. Read Characteristics

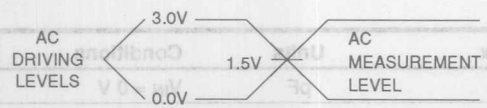
		AT28C04-15		AT28C04-20		AT28C04-25		
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Units
t_{ACC}	Address to Output Delay		150		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		150		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	10	70	10	80	10	100	ns
t_{DF} (3,4)	$\overline{CE}$ or $\overline{OE}$ High to Output Float	0	50	0	55	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

A.C. Read Waveforms



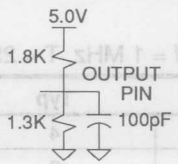
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 20 ns

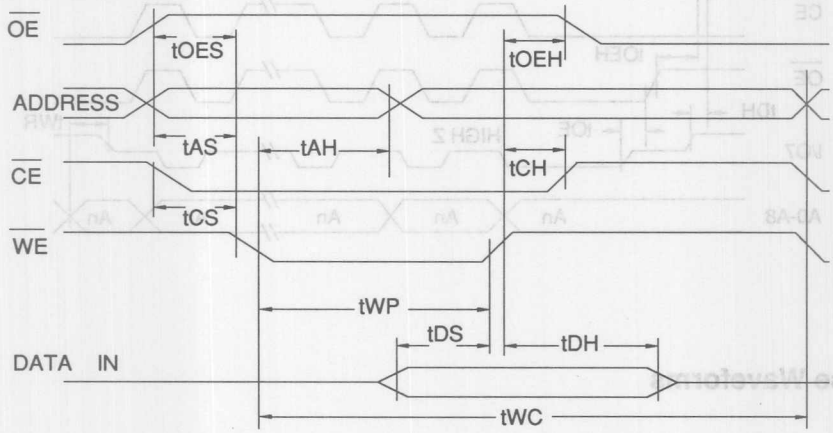
Output Test Load



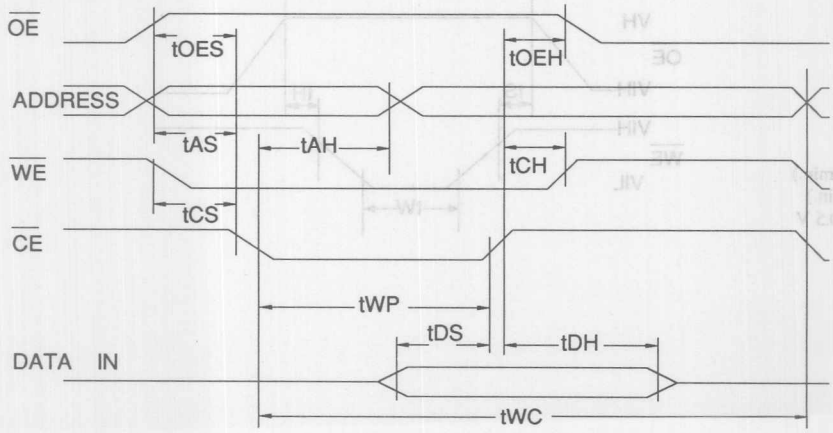
A.C. Write Characteristics

Symbol	Parameter		Min	Typ	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time		10			ns
t_{AH}	Address Hold Time		50			ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)		100		1000	ns
t_{DS}	Data Set-up Time		50			ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time		10			ns
t_{WC}	Write Cycle Time	AT28C04		0.5	1.0	ms
		AT28C04E/F		100	200	µs

A.C. Write Waveforms- $\overline{WE}$ Controlled



A.C. Write Waveforms- $\overline{CE}$ Controlled

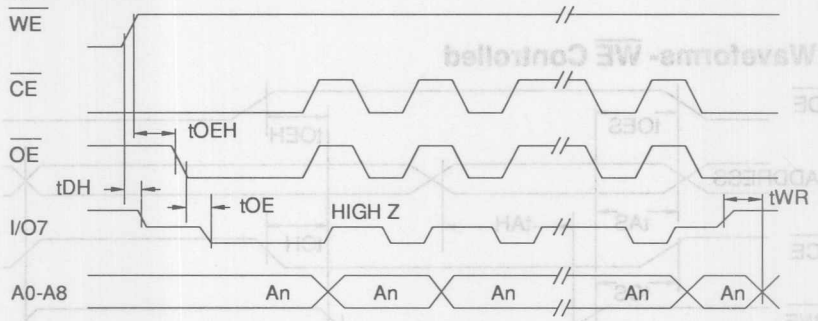


$\overline{\text{Data}}$ Polling Characteristics[1]

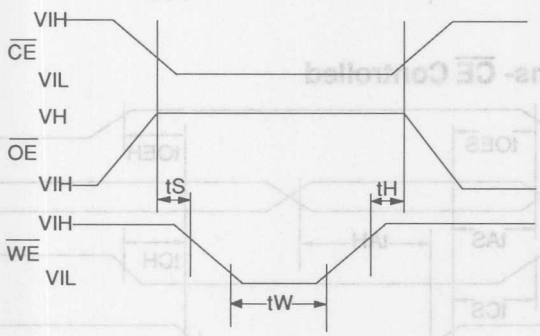
Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{\text{OE}}$ Hold Time	10			ns
t_{OE}	$\overline{\text{OE}}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{Data}}$ Polling Waveforms

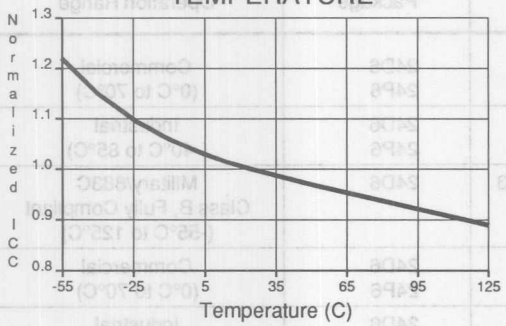


Chip Erase Waveforms

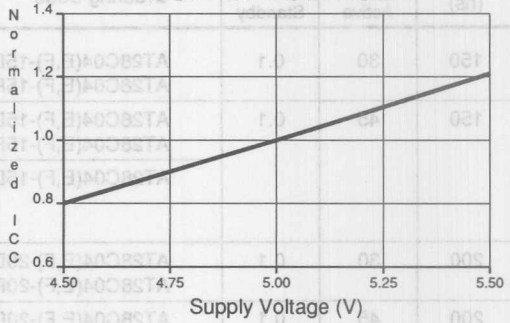


$t_S = t_H = 1$ µsec (min.)
$t_W = 10$ msec (min.)
$V_H = 12.0\ V \pm 0.5\ V$

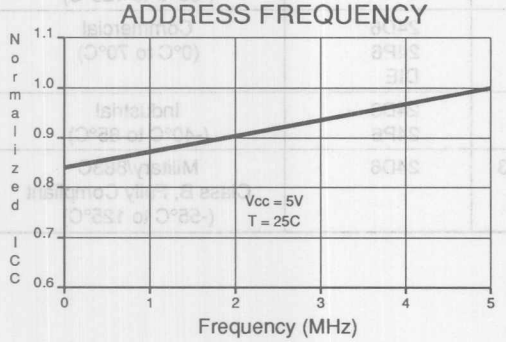
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



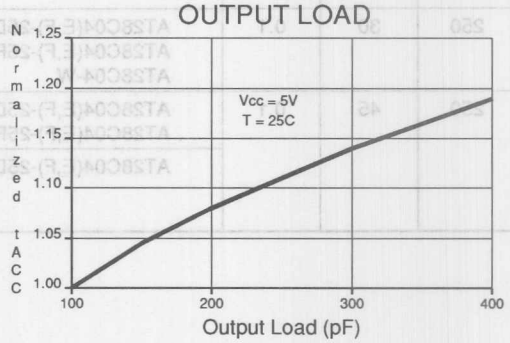
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



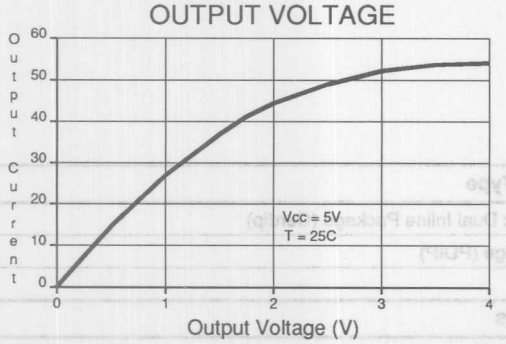
NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



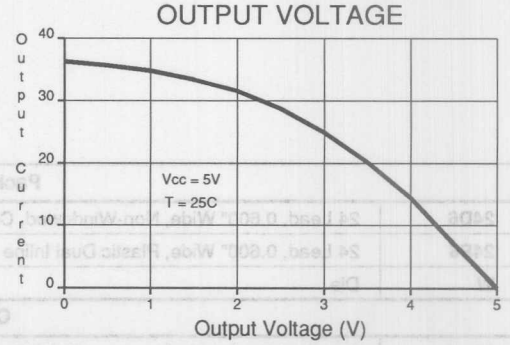
NORMALIZED ACCESS TIME vs. OUTPUT LOAD



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	30	0.1	AT28C04(E,F)-15DC AT28C04(E,F)-15PC	24D6 24P6	Commercial (0°C to 70°C)
150	45	0.1	AT28C04(E,F)-15DI AT28C04(E,F)-15PI	24D6 24P6	Industrial (-40°C to 85°C)
			AT28C04(E,F)-15DM/883	24D6	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	30	0.1	AT28C04(E,F)-20DC AT28C04(E,F)-20PC	24D6 24P6	Commercial (0°C to 70°C)
200	45	0.1	AT28C04(E,F)-20DI AT28C04(E,F)-20PI	24D6 24P6	Industrial (-40°C to 85°C)
			AT28C04(E,F)-20DM/883	24D6	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	30	0.1	AT28C04(E,F)-25DC AT28C04(E,F)-25PC AT28C04-W	24D6 24P6 DIE	Commercial (0°C to 70°C)
250	45	0.1	AT28C04(E,F)-25DI AT28C04(E,F)-25PI	24D6 24P6	Industrial (-40°C to 85°C)
			AT28C04(E,F)-25DM/883	24D6	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
24D6	24 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
24P6	24 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 1 ms
E	High Endurance Option: Endurance = 100K Write Cycles; Write Time = 200 µs
F	Fast Write Option: Write Time = 200 µs

16K (2K x 8) CMOS E^2PROM

Features

- Fast Read Access Time - 150 ns
- Fast Byte Write - 200 µs or 1 ms
- Self-Timed Byte Write Cycle
  - Internal Address and Data Latches
  - Internal Control Timer
  - Automatic Clear Before Write
- Direct Microprocessor Control
  - DATA POLLING
- Low Power
  - 30 mA Active Current
  - 100 µA CMOS Standby Current
- High Reliability
  - Endurance: 10^4 or 10^5 cycles
  - Data Retention: 10 years
- 5 V ± 10% Supply
- CMOS & TTL Compatible Inputs and Outputs
- JEDEC Approved Byte Wide Pinout
- Full Military, Commercial, and Industrial Temperature Ranges

Description

The AT28C16 is a low-power, high-performance Electrically Erasable and Programmable Read Only Memory with easy to use features. The AT28C16 is a 16K memory organized as 2,048 words x 8 bits. The device is manufactured with Atmel's reliable non-volatile CMOS technology.

The AT28C16 is accessed like a static RAM for the read or write cycles without the need of external components. During a byte write, the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. The end of a write cycle can be determined by $\overline{DATA}$ polling of I/O_7. Once the end of a write cycle has been detected, a new access for a read or a write can begin.

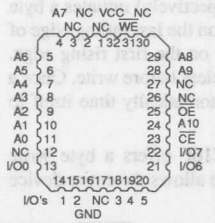
The CMOS technology offers fast access times of 150 ns at low power dissipation. When the chip is deselected the standby current is less than 100 µA.

Atmel's 28C16 has additional features to ensure high quality and manufacturability. The device utilizes error correction internally for extended endurance and for improved data retention characteristics. An extra 32 bytes of E^2PROM are available for device identification or tracking.

Pin Configurations

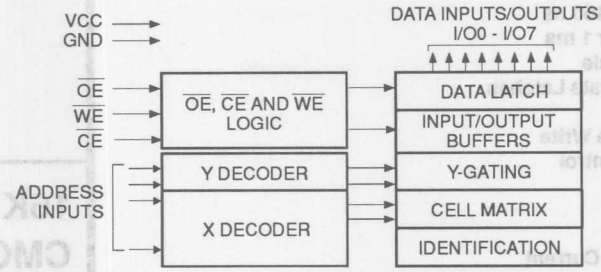
Pin Name	Function
A0 - A10	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect





Note: PLCC package pins 1 and 17 are DON'T CONNECT.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6 V to +6.25 V
All Output Voltages with Respect to Ground	-0.6 V to V_{CC} +0.6 V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6 V to +13.5 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: The AT28C16 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers increased flexibility in preventing bus contention.

BYTE WRITE: Writing data into the AT28C16 is similar to writing into a Static RAM. A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{OE}$ high and $\overline{CE}$ or $\overline{WE}$ low (respectively) initiates a byte write. The address location is latched on the last falling edge of $\overline{WE}$ (or $\overline{CE}$); the new data is latched on the first rising edge. Internally, the device performs a self-clear before write. Once a byte write has been started, it will automatically time itself to completion.

FAST BYTE WRITE: The AT28C16F offers a byte write time of 200 µs maximum. This feature allows the entire device to be rewritten in 0.4 seconds.

$\overline{DATA}$ POLLING: The AT28C16 provides $\overline{DATA}$ POLLING to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the complement of that data for I/O_7 (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

WRITE PROTECTION: Inadvertent writes to the device are protected against in the following ways. (a) Vcc sense— if Vcc is below 3.8 V (typical) the write function is inhibited. (b) Vcc power on delay— once Vcc has reached 3.8 V the device will automatically time out 5 ms (typical) before allowing a byte write. (c) Write Inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits byte write cycles.

CHIP CLEAR: The contents of the entire memory of the AT28C16 may be set to the high state by the CHIP CLEAR operation. By setting $\overline{CE}$ low and $\overline{OE}$ to 12 volts, the chip is cleared when a 10 msec low pulse is applied to $\overline{WE}$.

DEVICE IDENTIFICATION: An extra 32 bytes of E^2PROM memory are available to the user for device identification. By raising A9 to 12 ± 0.5 V and using address locations 7E0H to 7FFH the additional bytes may be written to or read from in the same manner as the regular memory array.

D.C. and A.C. Operating Range

		AT28C16-15	AT28C16-20	AT28C16-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 10%	5 V ± 10%	5 V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H [3]	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.
3. V_H = 12.0 V ± 0.5 V.

D.C. Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC} + 1 V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$=0V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC}-0.3 V to V_{CC} + 1.0 V			100	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0 V to V_{CC} + 1.0 V	Com.		2	mA
			Ind., Mil.		3	mA
I_{CC}	V_{CC} Active Current A.C.	f = 5 MHz; I_{OUT} = 0 mA $\overline{CE}$ = V_{IL}	Com.		30	mA
			Ind., Mil.		45	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA		2.4		V

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

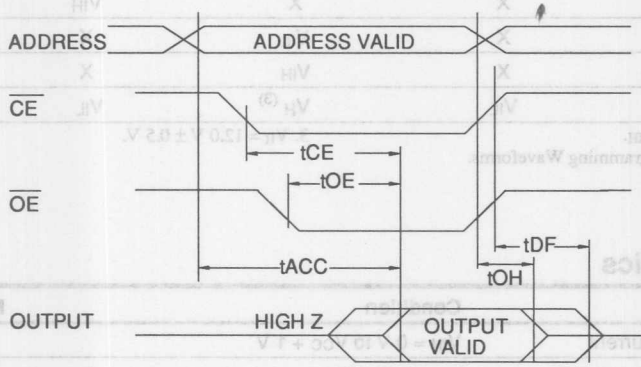
	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Note: 1. This parameter is characterized and is not 100% tested.

A.C. Read Characteristics

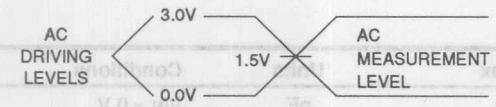
Symbol	Parameter	AT28C16-15		AT28C16-20		AT28C16-25		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		150		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		150		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	10	70	10	80	10	100	ns
t_{DF} (3,4)	$\overline{CE}$ or $\overline{OE}$ High to Output Float	0	50	0	55	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

A.C. Read Waveforms



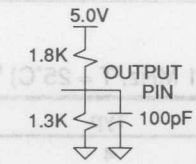
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 20 ns

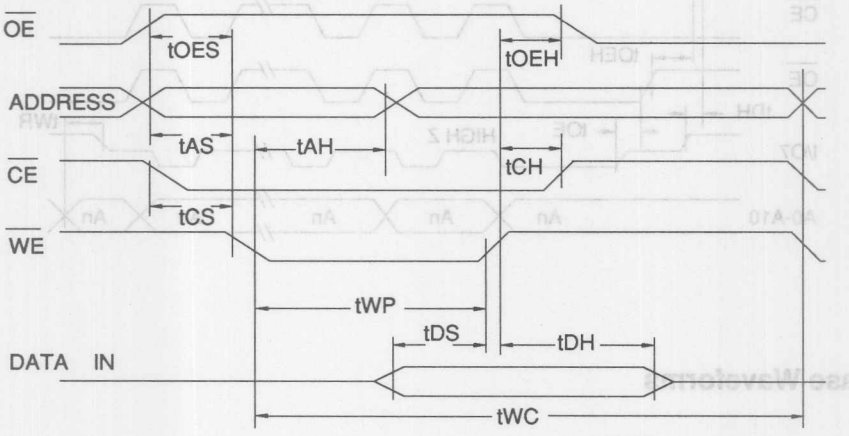
Output Test Load



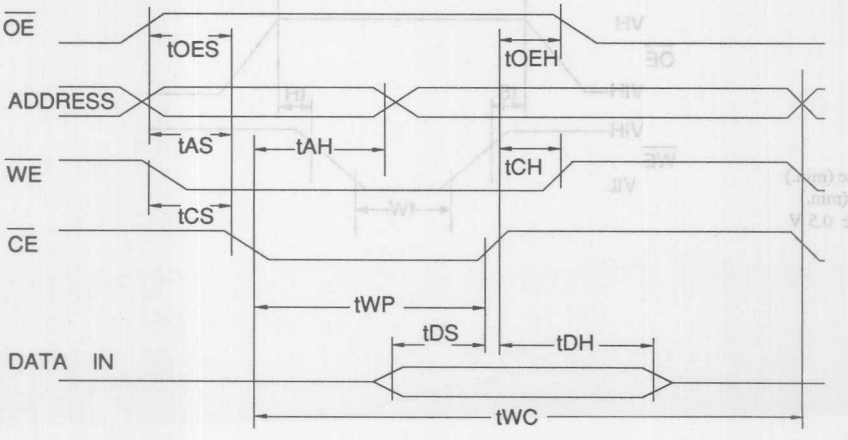
A.C. Write Characteristics

Symbol	Parameter		Min	Typ	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time		10			ns
t_{AH}	Address Hold Time		50			ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)		100		1000	ns
t_{DS}	Data Set-up Time		50			ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time		10			ns
t_{WC}	Write Cycle Time	AT28C16		0.5	1.0	ms
		AT28C16E/F		100	200	µs

A.C. Write Waveforms- $\overline{WE}$ Controlled



A.C. Write Waveforms- $\overline{CE}$ Controlled

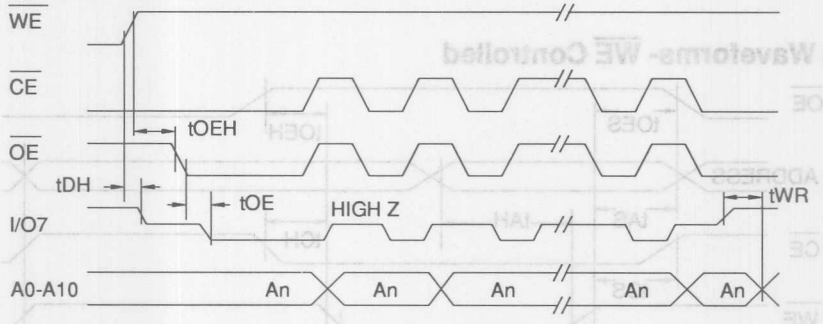


$\overline{\text{Data}}$ Polling Characteristics[1]

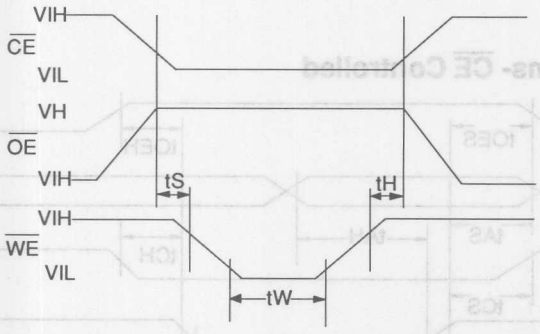
Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{Data}}$ Polling Waveforms

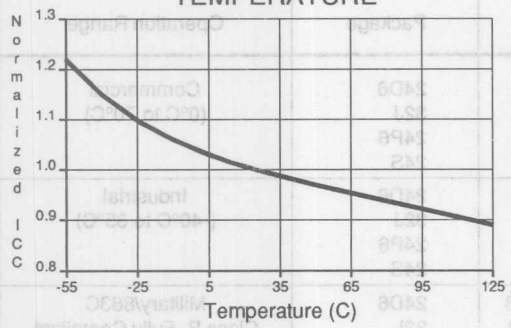


Chip Erase Waveforms

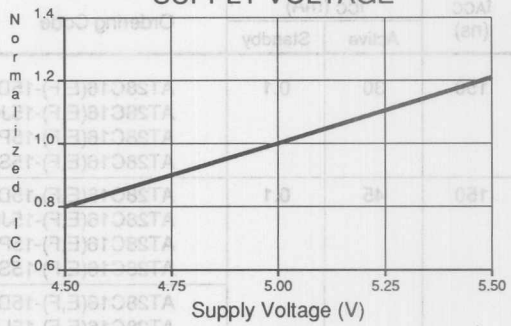


$t_S = t_H = 1\ \mu sec$ (min.)
$t_W = 10$ msec (min.)
$V_H = 12.0\ V \pm 0.5\ V$

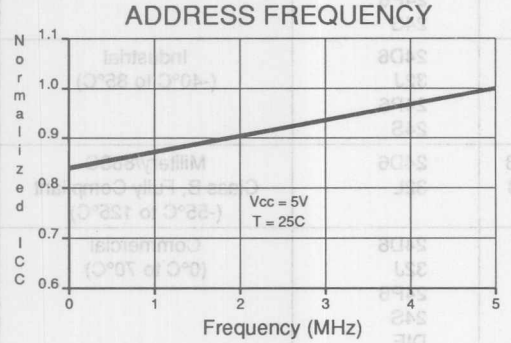
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



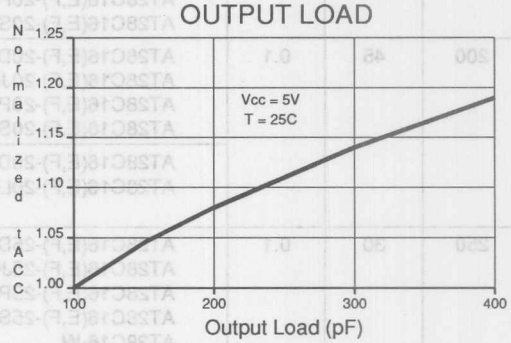
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



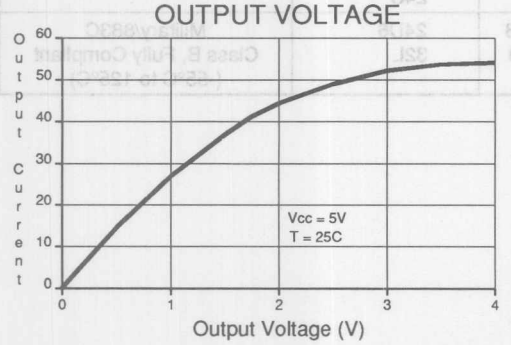
NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



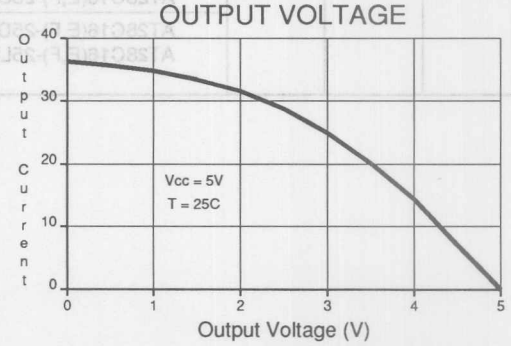
NORMALIZED ACCESS TIME vs. OUTPUT LOAD



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	30	0.1	AT28C16(E,F)-15DC AT28C16(E,F)-15JC AT28C16(E,F)-15PC AT28C16(E,F)-15SC	24D6 32J 24P6 24S	Commercial (0°C to 70°C)
150	45	0.1	AT28C16(E,F)-15DI AT28C16(E,F)-15JI AT28C16(E,F)-15PI AT28C16(E,F)-15SI	24D6 32J 24P6 24S	Industrial (-40°C to 85°C)
			AT28C16(E,F)-15DM/883 AT28C16(E,F)-15LM/883	24D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	30	0.1	AT28C16(E,F)-20DC AT28C16(E,F)-20JC AT28C16(E,F)-20PC AT28C16(E,F)-20SC	24D6 32J 24P6 24S	Commercial (0°C to 70°C)
200	45	0.1	AT28C16(E,F)-20DI AT28C16(E,F)-20JI AT28C16(E,F)-20PI AT28C16(E,F)-20SI	24D6 32J 24P6 24S	Industrial (-40°C to 85°C)
			AT28C16(E,F)-20DM/883 AT28C16(E,F)-20LM/883	24D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	30	0.1	AT28C16(E,F)-25DC AT28C16(E,F)-25JC AT28C16(E,F)-25PC AT28C16(E,F)-25SC AT28C16-W	24D6 32J 24P6 24S DIE	Commercial (0°C to 70°C)
250	45	0.1	AT28C16(E,F)-25DI AT28C16(E,F)-25JI AT28C16(E,F)-25PI AT28C16(E,F)-25SI	24D6 32J 24P6 24S	Industrial (-40°C to 85°C)
			AT28C16(E,F)-25DM/883 AT28C16(E,F)-25LM/883	24D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

Package Type	
24D6	24 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
24P6	24 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
24S	24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 1 ms
E	High Endurance Option: Endurance = 100K Write Cycles; Write Time = 200 µs
F	Fast Write Option: Write Time = 200 µs

Package Type	
J	24 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
L	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
N	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
P	24 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
S	24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 1 ms
E	High Endurance Option: Endurance = 100K Write Cycles; Write Time = 200 µs
F	Fast Write Option: Write Time = 200 µs

2

16K (2K x 8) CMOS E^2PROM

Features

- Fast Read Access Time - 150 ns
- Fast Byte Write - 200 µs or 1 ms
- Self-Timed Byte Write Cycle
  - Internal Address and Data Latches
  - Internal Control Timer
  - Automatic Clear Before Write
- Direct Microprocessor Control
  - DATA POLLING
  - READY/BUSY Open Drain Output
- Low Power
  - 30 mA Active Current
  - 100 µa CMOS Standby Current
- High Reliability
  - Endurance: 10^4 or 10^5 cycles
  - Data Retention: 10 years
- 5 V ± 10% Supply
- CMOS & TTL Compatible Inputs and Outputs
- JEDEC Approved Byte Wide Pinout
- Full Military, Commercial, and Industrial Temperature Ranges

Description

The AT28C17 is a low-power, high-performance Electrically Erasable and Programmable Read Only Memory with easy to use features. The AT28C17 is a 16K memory organized as 2,048 words x 8 bits. The device is manufactured with Atmel's reliable nonvolatile CMOS technology.

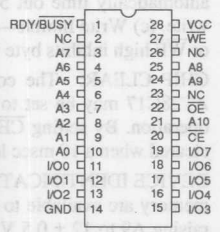
The AT28C17 is accessed like a static RAM for the read or write cycles without the need of external components. During a byte write, the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. The device includes two methods for detecting the end of a write cycle, level detection of RDY/$\overline{BUSY}$ and $\overline{DATA}$ polling of I/O_7. Once the end of a write cycle has been detected, a new access for a read or a write can begin.

The CMOS technology offers fast access times of 150 ns at low power dissipation. When the chip is deselected the standby current is less than 100 µA.

Atmel's 28C17 has additional features to ensure high quality and manufacturability. The device utilizes error correction internally for extended endurance and for improved data retention characteristics. An extra 32 bytes of E^2PROM are available for device identification or tracking.

Pin Configurations

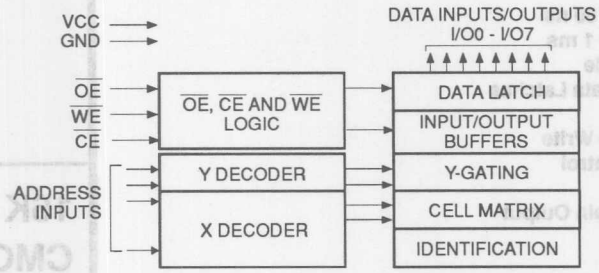
Pin Name	Function
A0 - A10	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
RDY/$\overline{BUSY}$	Ready/$\overline{Busy}$ Output
NC	No Connect





Note: PLCC package pins 1 and 17 are DON'T CONNECT.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6 V to +6.25 V
All Output Voltages with Respect to Ground	-0.6 V to V_{CC} +0.6 V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6 V to +13.5 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: The AT28C17 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers increased flexibility in preventing bus contention.

BYTE WRITE: Writing data into the AT28C17 is similar to writing into a Static RAM. A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{OE}$ high and $\overline{CE}$ or $\overline{WE}$ low (respectively) initiates a byte write. The address location is latched on the last falling edge of $\overline{WE}$ (or $\overline{CE}$); the new data is latched on the first rising edge. Internally, the device performs a self-clear before write. Once a byte write has been started, it will automatically time itself to completion.

FAST BYTE WRITE: The AT28C17F offers a byte write time of 200 µs maximum. This feature allows the entire device to be rewritten in 0.4 seconds.

READY/$\overline{BUSY}$: Pin 1 is an open drain READY/$\overline{BUSY}$ output that can be used to detect the end of a write cycle. RDY/$\overline{BUSY}$ is actively pulled low during the write cycle and is released at the completion of the write. The open drain connection allows for OR-tying of several devices to the same RDY/$\overline{BUSY}$ line.

$\overline{DATA}$ POLLING: The AT28C17 provides $\overline{DATA}$ POLLING to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the complement of that data for I/O_7 (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

WRITE PROTECTION: Inadvertent writes to the device are protected against in the following ways. (a) Vcc sense— if Vcc is below 3.8 V (typical) the write function is inhibited. (b) Vcc power on delay— once Vcc has reached 3.8 V the device will automatically time out 5 ms (typical) before allowing a byte write. (c) Write Inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits byte write cycles.

CHIP CLEAR: The contents of the entire memory of the AT28C17 may be set to the high state by the CHIP CLEAR operation. By setting $\overline{CE}$ low and $\overline{OE}$ to 12 volts, the chip is cleared when a 10 msec low pulse is applied to $\overline{WE}$.

DEVICE IDENTIFICATION: An extra 32 bytes of E^2PROM memory are available to the user for device identification. By raising A9 to 12 ± 0.5 V and using address locations 7E0H to 7FFH the additional bytes may be written to or read from in the same manner as the regular memory array.

D.C. and A.C. Operating Range

		AT28C17-15	AT28C17-20	AT28C17-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 10%	5 V ± 10%	5V±10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H [3]	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.
3. $V_H = 12.0\ V \pm 0.5\ V$.

D.C. Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	$V_{IN} = 0\ V$ to $V_{CC} + 1\ V$			10	µA
I_{LO}	Output Leakage Current	$V_{I/O} = 0\ V$ to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE} = V_{CC}$-0.3 V to $V_{CC} + 1.0\ V$			100	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE} = 2.0\ V$ to $V_{CC} + 1.0\ V$	Com.		2	mA
			Ind., Mil.		3	mA
I_{CC}	V_{CC} Active Current A.C.	f = 5 MHz; $I_{OUT} = 0$ mA $\overline{CE} = V_{IL}$	Com.		30	mA
			Ind., Mil.		45	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA = 4.0 for RDY/$\overline{BUSY}$			.4	V
V_{OH}	Output High Voltage	$I_{OH} = -400\ \mu A$		2.4		V

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

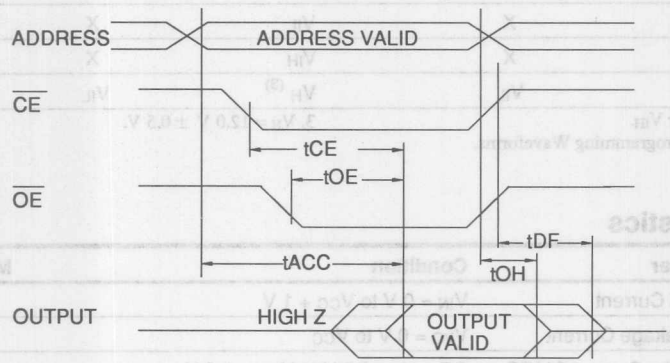
	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	$V_{IN} = 0\ V$
C_{OUT}	8	12	pF	$V_{OUT} = 0\ V$

Note: 1. This parameter is characterized and is not 100% tested.

A.C. Read Characteristics

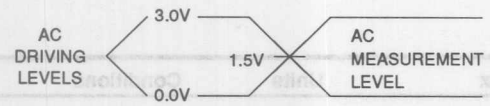
Symbol	Parameter	AT28C17-15 Min	AT28C17-15 Max	AT28C17-20 Min	AT28C17-20 Max	AT28C17-25 Min	AT28C17-25 Max	Units
t_{ACC}	Address to Output Delay		150		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		150		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	10	70	10	80	10	100	ns
t_{DF} (3,4)	$\overline{CE}$ or $\overline{OE}$ High to Output Float	0	50	0	55	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

A.C. Read Waveforms



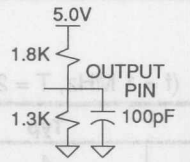
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 20 ns

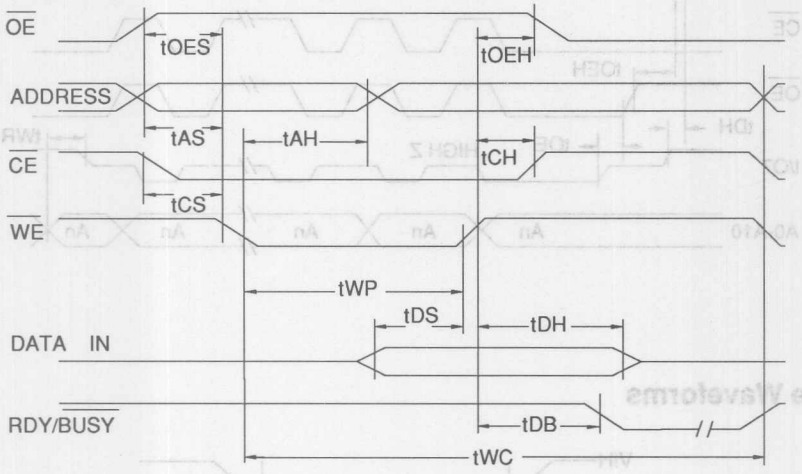
Output Test Load



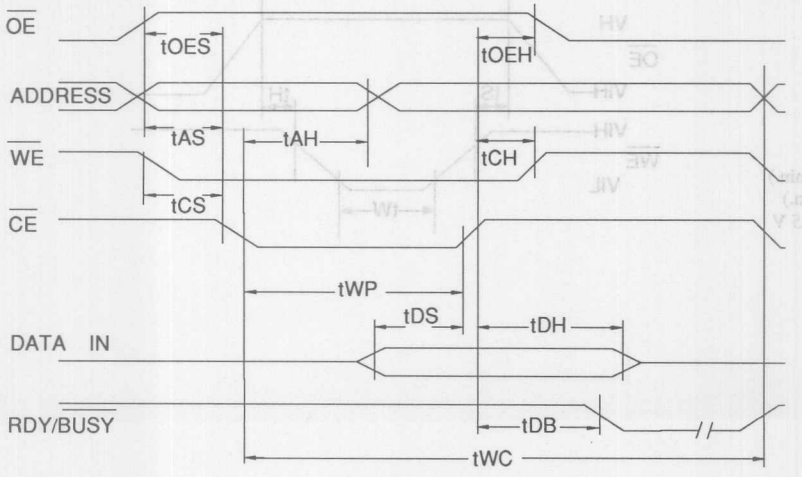
A.C. Write Characteristics

Symbol	Parameter		Min	Typ	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time		10			ns
t_{AH}	Address Hold Time		50			ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)		100		1000	ns
t_{DS}	Data Set-up Time		50			ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time		10			ns
t_{DB}	Time to Device Busy				50	ns
t_{WC}	Write Cycle Time	AT28C17		0.5	1.0	ms
		AT28C17E/F		100	200	µs

A.C. Write Waveforms- $\overline{WE}$ Controlled



A.C. Write Waveforms- $\overline{CE}$ Controlled

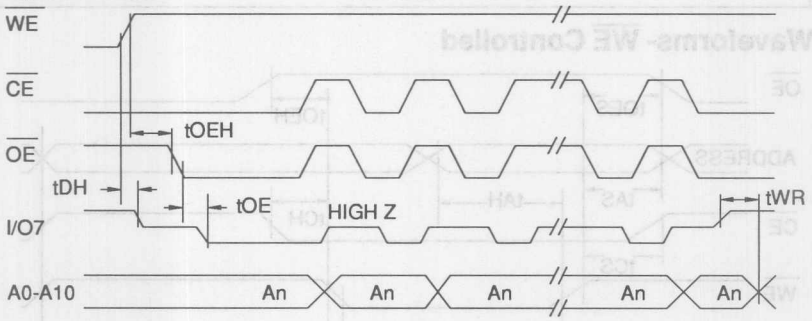


$\overline{\text{Data}}$ Polling Characteristics[1]

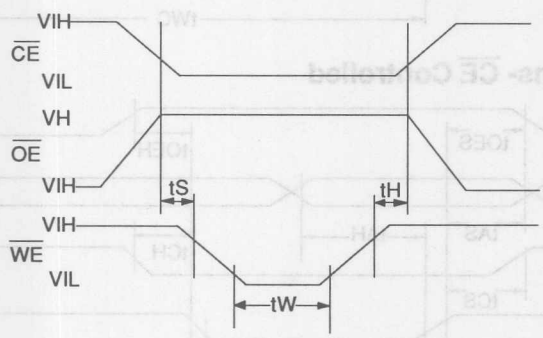
Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{Data}}$ Polling Waveforms

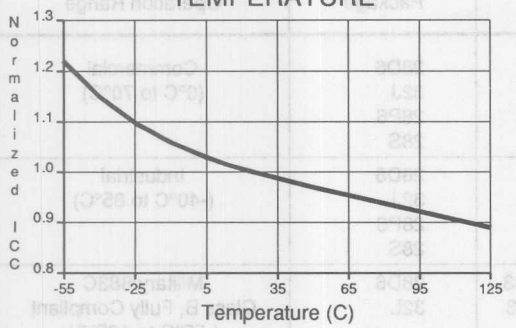


Chip Erase Waveforms

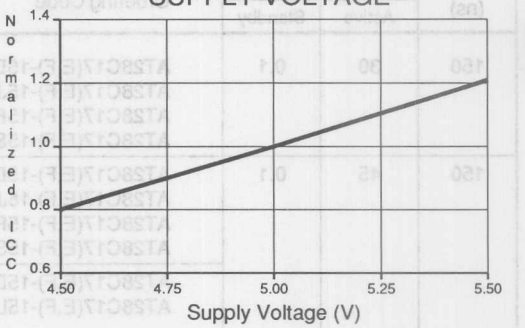


$t_S = t_H = 1$ µsec (min.)
$t_W = 10$ msec (min.)
$V_H = 12.0\ V \pm 0.5\ V$

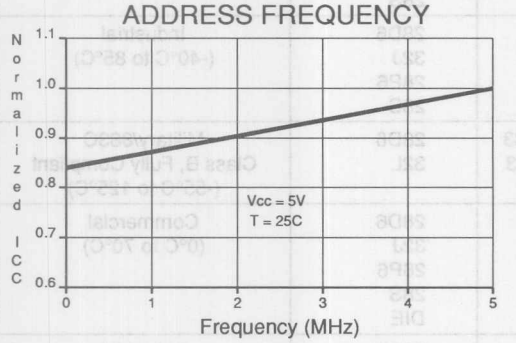
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



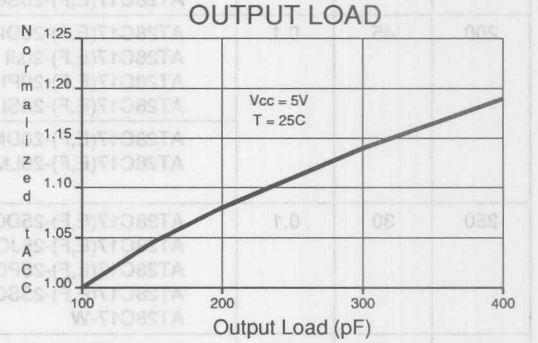
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



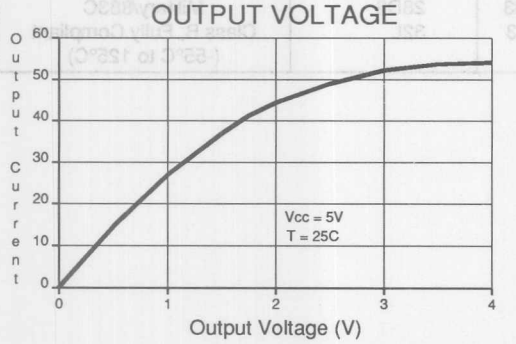
NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



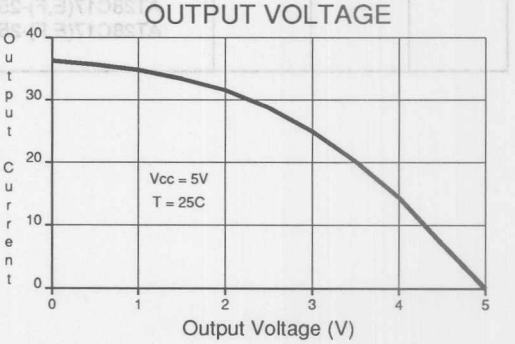
NORMALIZED ACCESS TIME vs. OUTPUT LOAD



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	30	0.1	AT28C17(E,F)-15DC AT28C17(E,F)-15JC AT28C17(E,F)-15PC AT28C17(E,F)-15SC	28D6 32J 28P6 28S	Commercial (0°C to 70°C)
150	45	0.1	AT28C17(E,F)-15DI AT28C17(E,F)-15JI AT28C17(E,F)-15PI AT28C17(E,F)-15SI	28D6 32J 28P6 28S	Industrial (-40°C to 85°C)
			AT28C17(E,F)-15DM/883 AT28C17(E,F)-15LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	30	0.1	AT28C17(E,F)-20DC AT28C17(E,F)-20JC AT28C17(E,F)-20PC AT28C17(E,F)-20SC	28D6 32J 28P6 28S	Commercial (0°C to 70°C)
200	45	0.1	AT28C17(E,F)-20DI AT28C17(E,F)-20JI AT28C17(E,F)-20PI AT28C17(E,F)-20SI	28D6 32J 28P6 28S	Industrial (-40°C to 85°C)
			AT28C17(E,F)-20DM/883 AT28C17(E,F)-20LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	30	0.1	AT28C17(E,F)-25DC AT28C17(E,F)-25JC AT28C17(E,F)-25PC AT28C17(E,F)-25SC AT28C17-W	28D6 32J 28P6 28S DIE	Commercial (0°C to 70°C)
250	45	0.1	AT28C17(E,F)-25DI AT28C17(E,F)-25JI AT28C17(E,F)-25PI AT28C17(E,F)-25SI	28D6 32J 28P6 28S	Industrial (-40°C to 85°C)
			AT28C17(E,F)-25DM/883 AT28C17(E,F)-25LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28S	28 Lead, 0.300" Wide, Plastic Gull Wing, Small Outline (SOIC)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 1 ms
E	High Endurance Option: Endurance = 100K Write Cycles; Write Time = 200 µs
F	Fast Write Option: Write Time = 200 µs

Ordering Information

Package Type	
28DG	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28S	28 Lead, 0.300" Wide, Plastic Gull Wing, Small Outline (SOIC)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 1 ms
E	High Endurance Option: Endurance = 100K Write Cycles; Write Time = 200 µs
F	Fast Write Option: Write Time = 200 µs

64K (8K x 8) CMOS E²PROM

Features

- Fast Read Access Time - 120 ns
- Fast Byte Write - 200 µs or 1 ms
- Self-Timed Byte Write Cycle
  - Internal Address and Data Latches
  - Internal Control Timer
  - Automatic Clear Before Write
- Direct Microprocessor Control
  - READY/BUSY Open Drain Output
  - DATA Polling
- Low Power
  - 30 mA Active Current
  - 100 µA CMOS Standby Current
- High Reliability
  - Endurance: 10^4 or 10^5 Cycles
  - Data Retention: 10 years
- 5 V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-Wide Pinout
- Full Military, Commercial, and Industrial Temperature Ranges

Description

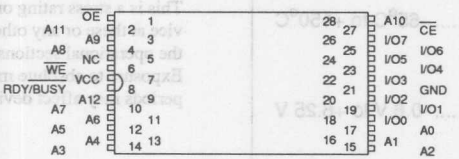
The AT28C64 is a low-power, high-performance 8,192 words x 8 bit nonvolatile Electrically Erasable and Programmable Read Only Memory with popular, easy to use features. The device is manufactured with Atmel's reliable nonvolatile technology.

The AT28C64 is accessed like a Static RAM for the read or write cycles without the need for external components. During a byte write, the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a

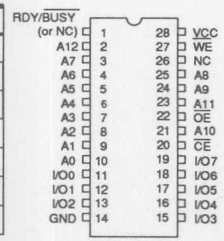
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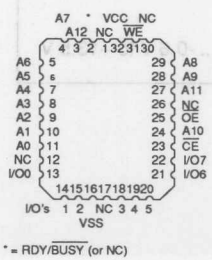
Pin Configurations

TSOP Top View



Pin Name	Function
A0 - A12	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
RDY/$\overline{BUSY}$	Ready/$\overline{Busy}$ Output
NC	No Connect





* = RDY/$\overline{BUSY}$ (or NC)

Note: PLCC package pins 1 and 17 are DON'T CONNECT.

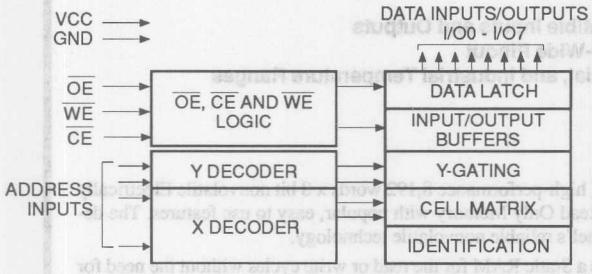
Description (Continued)

write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. The device includes two methods for detecting the end of a write cycle, level detection of RDY/$\overline{BUSY}$ (unless pin 1 is N.C.) and $\overline{DATA}$ polling of I/O_7. Once the end of a write cycle has been detected, a new access for a read or write can begin.

The CMOS technology offers fast access times of 150 ns at low power dissipation. When the chip is deselected the standby current is less than 100 µA.

Atmel's 28C64 has additional features to ensure high quality and manufacturability. The device utilizes error correction internally for extended endurance and for improved data retention characteristics. An extra 32 bytes of E^2PROM are available for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6 V to +6.25 V
All Output Voltages with Respect to Ground	-0.6 V to V_{CC} +0.6 V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6 V to +13.5 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: The AT28C64 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers increased flexibility in preventing bus contention.

BYTE WRITE: Writing data into the AT28C64 is similar to writing into a Static RAM. A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{OE}$ high and $\overline{CE}$ or $\overline{WE}$ low (respectively) initiates a byte write. The address location is latched on the falling edge of $\overline{WE}$ (or $\overline{CE}$); the new data is latched on the rising edge. Internally, the device performs a self-clear before write. Once a byte write has been started, it will automatically time itself to completion.

FAST BYTE WRITE: The AT28C64F offers a byte write time of 200 µs maximum. This feature allows the entire device to be rewritten in 1.6 seconds.

READY/$\overline{BUSY}$: Pin 1 is an open drain READY/$\overline{BUSY}$ output that can be used to detect the end of a write cycle. RDY/$\overline{BUSY}$ is actively pulled low during the write cycle and is released at the completion of the write. The open drain connection allows for OR-tying of several devices to the same RDY/$\overline{BUSY}$ line. Pin 1 is not connected for the AT28C64X.

$\overline{DATA}$ POLLING: The AT28C64 provides $\overline{DATA}$ POLLING to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the complement of that data for I/O_7 (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

WRITE PROTECTION: Inadvertent writes to the device are protected against in the following ways. (a) Vcc sense— if Vcc is below 3.8 V (typical) the write function is inhibited. (b) Vcc power on delay— once Vcc has reached 3.8 V the device will automatically time out 5 ms (typical) before allowing a byte write. (c) Write Inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits byte write cycles.

CHIP CLEAR: The contents of the entire memory of the AT28C64 may be set to the high state by the CHIP CLEAR operation. By setting $\overline{CE}$ low and $\overline{OE}$ to 12 volts, the chip is cleared when a 10 msec low pulse is applied to $\overline{WE}$.

DEVICE IDENTIFICATION: An extra 32 bytes of E^2PROM memory are available to the user for device identification. By raising A9 to 12 ± 0.5 V and using address locations 1FE0H to 1FFFH the additional bytes may be written to or read from in the same manner as the regular memory array.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Note: 1. This parameter is characterized and is not 100% tested.

D.C. and A.C. Operating Range

		AT28C64-12	AT28C64-15	AT28C64-20	AT28C64-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 10%	5 V ± 10%	5 V ± 10%	5 V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H [3]	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.
3. $V_H = 12.0\ V \pm 0.5\ V$.

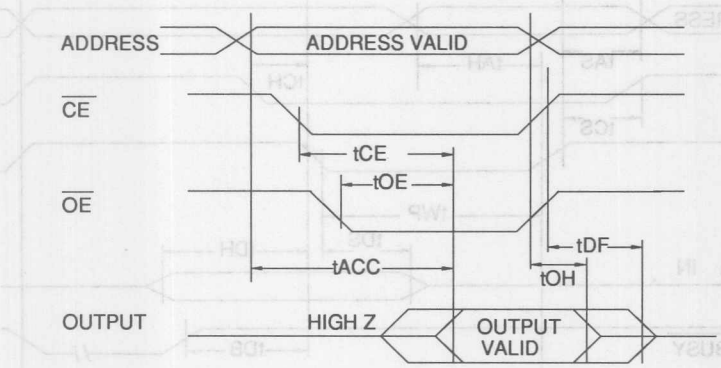
D.C. Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	$V_{IN} = 0\ V$ to $V_{CC} + 1\ V$			10	µA
I_{LO}	Output Leakage Current	$V_{I/O} = 0\ V$ to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE} = V_{CC}-0.3\ V$ to $V_{CC} + 1.0\ V$			100	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE} = 2.0\ V$ to $V_{CC} + 1.0\ V$	Com.		2	mA
			Ind., Mil.		3	mA
I_{CC}	V_{CC} Active Current A.C.	f = 5 MHz; $I_{OUT} = 0$ mA $\overline{CE} = V_{IL}$	Com.		30	mA
			Ind., Mil.		45	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA = 4.0 mA for RDY/$\overline{BUSY}$			.45	V
V_{OH}	Output High Voltage	$I_{OH} = -400\ \mu A$		2.4		V

A.C. Read Characteristics

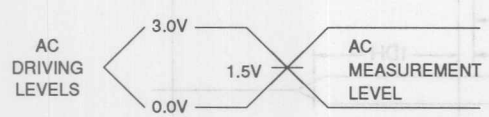
Symbol	Parameter	AT28C64-12		AT28C64-15		AT28C64-20		AT28C64-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		120		150		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		120		150		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	10	60	10	70	10	80	10	100	ns
t_{DF} (3,4)	$\overline{CE}$ or $\overline{OE}$ High to Output Float	0	45	0	50	0	55	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		ns

A.C. Read Waveforms



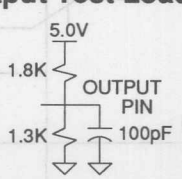
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



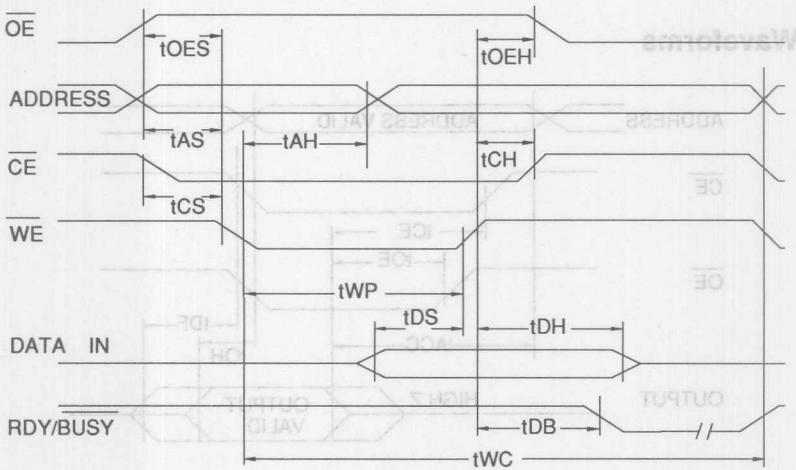
t_R, t_F < 20 ns

Output Test Load

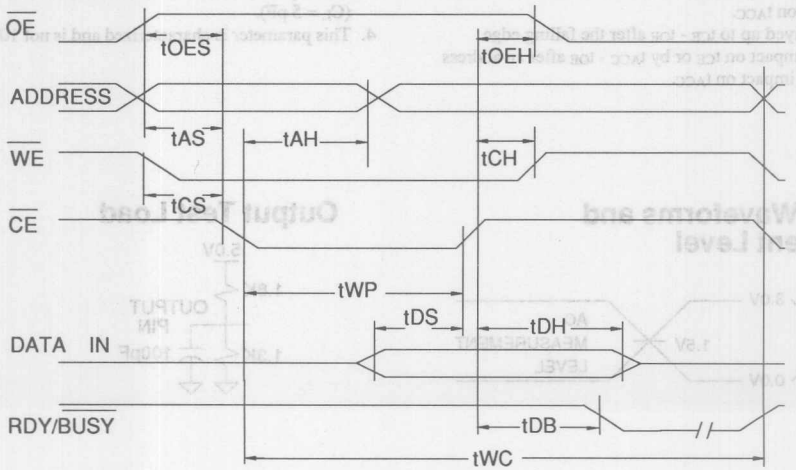


Symbol	Parameter		Min	Typ	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time		10			ns
t_{AH}	Address Hold Time		50			ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)		100		1000	ns
t_{DS}	Data Set-up Time		50			ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time		10			ns
t_{DB}	Time to Device Busy				50	ns
t_{WC}	Write Cycle Time	AT28C64		0.5	1.0	ms
		AT28C64E/F		100	200	µs

A.C. Write Waveforms- $\overline{WE}$ Controlled



A.C. Write Waveforms- $\overline{CE}$ Controlled

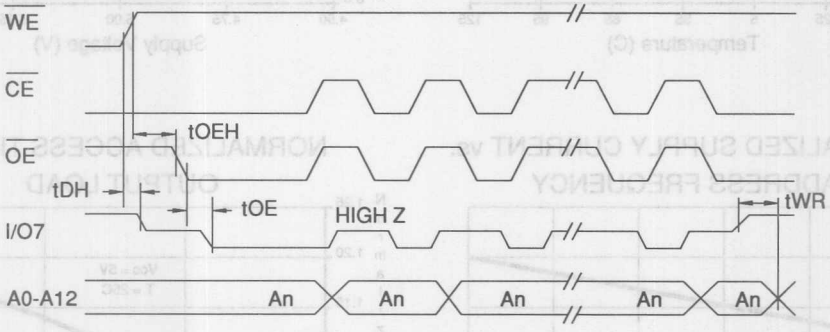


$\overline{\text{Data}}$ Polling Characteristics[1]

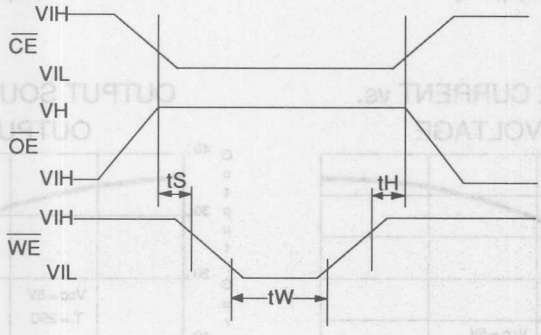
Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{Data}}$ Polling Waveforms

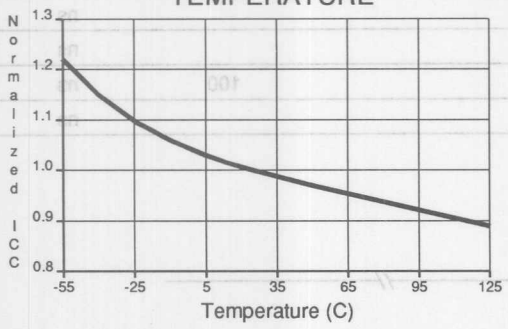


Chip Erase Waveforms

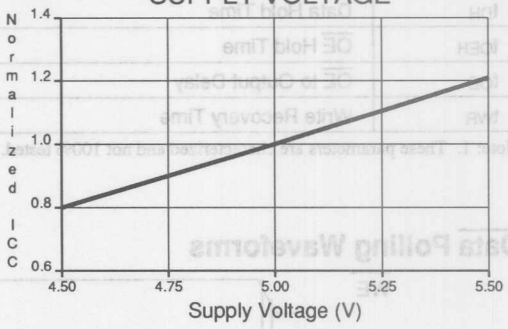


$t_S = t_H = 1$ µsec (min.)
$t_W = 10$ msec (min.)
$V_H = 12.0\ V \pm 0.5\ V$

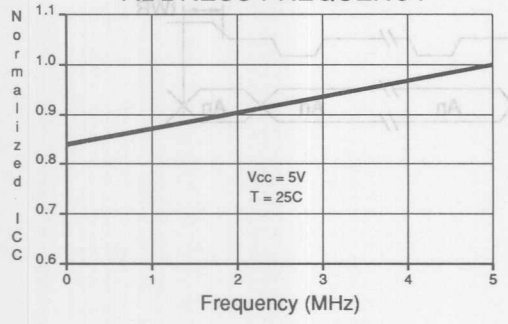
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



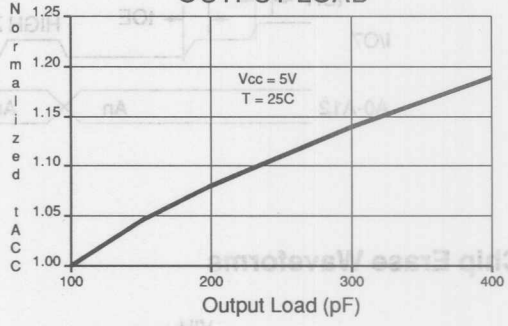
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



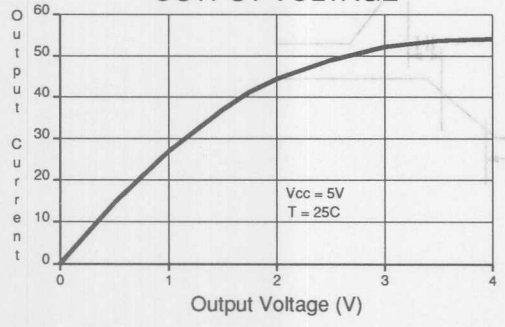
NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



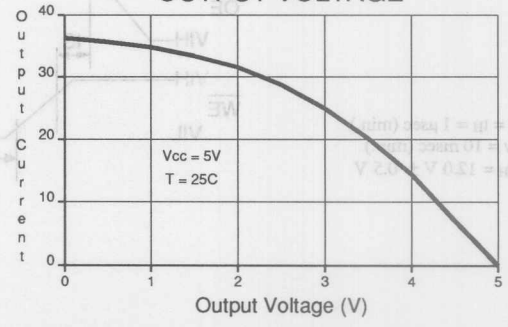
NORMALIZED ACCESS TIME vs. OUTPUT LOAD



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	30	0.1	AT28C64(E,F)-12DC AT28C64(E,F)-12JC AT28C64(E,F)-12PC AT28C64(E,F)-12SC	28D6 32J 28P6 28S	Commercial (0°C to 70°C)
120	45	0.1	AT28C64(E,F)-12DI AT28C64(E,F)-12JI AT28C64(E,F)-12PI AT28C64(E,F)-12SI	28D6 32J 28P6 28S	Industrial (-40°C to 85°C)
			AT28C64(E,F)-12DM/883 AT28C64(E,F)-12FM/883 AT28C64(E,F)-12LM/883	28D6 28F 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	30	0.1	AT28C64(E,F)-15DC AT28C64(E,F)-15JC AT28C64(E,F)-15PC AT28C64(E,F)-15SC AT28C64(E,F)-15TC	28D6 32J 28P6 28S 28T	Commercial (0°C to 70°C)
150	45	0.1	AT28C64(E,F)-15DI AT28C64(E,F)-15JI AT28C64(E,F)-15PI AT28C64(E,F)-15SI AT28C64(E,F)-15TI	28D6 32J 28P6 28S 28T	Industrial (-40°C to 85°C)
			AT28C64(E,F)-15DM/883 AT28C64(E,F)-15FM/883 AT28C64(E,F)-15LM/883	28D6 28F 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	30	0.1	AT28C64(E,F)-20DC AT28C64(E,F)-20JC AT28C64(E,F)-20PC AT28C64(E,F)-20SC	28D6 32J 28P6 28S	Commercial (0°C to 70°C)
200	45	0.1	AT28C64(E,F)-20DI AT28C64(E,F)-20JI AT28C64(E,F)-20PI AT28C64(E,F)-20SI	28D6 32J 28P6 28S	Industrial (-40°C to 85°C)
			AT28C64(E,F)-20DM/883 AT28C64(E,F)-20FM/883 AT28C64(E,F)-20LM/883	28D6 28F 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	30	0.1	AT28C64(E,F)-25DC AT28C64(E,F)-25JC AT28C64(E,F)-25PC AT28C64(E,F)-25SC AT28C64-W	28D6 32J 28P6 28S DIE	Commercial (0°C to 70°C)
250	45	0.1	AT28C64(E,F)-25DI AT28C64(E,F)-25JI AT28C64(E,F)-25PI AT28C64(E,F)-25SI	28D6 32J 28P6 28S	Industrial (-40°C to 85°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
250	45	0.1	AT28C64(E,F)-25DM/883 AT28C64(E,F)-25FM/883 AT28C64(E,F)-25LM/883	28D6 28F 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
300[1]	45	0.1	AT28C64(E,F)-30DM/883 AT28C64(E,F)-30FM/883 AT28C64(E,F)-30LM/883	28D6 28F 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
350[1]	45	0.1	AT28C64(E,F)-35DM/883 AT28C64(E,F)-35FM/883 AT28C64(E,F)-35LM/883	28D6 28F 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	45	0.1	5962-87514 17 XX 5962-87514 17 YX	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	45	0.1	5962-87514 16 XX 5962-87514 16 YX	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	45	0.1	5962-87514 15 XX 5962-87514 15 YX 5962-87514 15 ZX	28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
300[1]	45	0.1	5962-87514 14 XX 5962-87514 14 YX	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
350[1]	45	0.1	5962-87514 13 XX 5962-87514 13 YX 5962-87514 13 ZX	28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Notes: 1. Electrical specifications for these speeds are defined in Standardized Military Drawing 5962-87514.

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
28F	28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28S	28 Lead, 0.300" Wide, Plastic Gull Wing, Small Outline (SOIC)
28T	28 Lead, Plastic Thin Small Outline Package (TSOP)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 1 ms
E	High Endurance Option: Endurance = 100K Write Cycles; Write Time = 200 µs
F	Fast Write Option: Write Time = 200 µs

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	30	0.1	AT28C64X-15DC AT28C64X-15FC AT28C64X-15JC AT28C64X-15PC AT28C64X-15SC	28D6 28F 32J 28P6 28S	Commercial (0°C to 70°C)
150	45	0.1	AT28C64X-15DI AT28C64X-15FI AT28C64X-15JI AT28C64X-15PI AT28C64X-15SI	28D6 28F 32J 28P6 28S	Industrial (-40°C to 85°C)
			AT28C64X-15DM/883 AT28C64X-15FM/883 AT28C64X-15LM/883	28D6 28F 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	30	0.1	AT28C64X-20DC AT28C64X-20FC AT28C64X-20JC AT28C64X-20PC AT28C64X-20SC	28D6 28F 32J 28P6 28S	Commercial (0°C to 70°C)
200	45	0.1	AT28C64X-20DI AT28C64X-20FI AT28C64X-20JI AT28C64X-20PI AT28C64X-20SI	28D6 28F 32J 28P6 28S	Industrial (-40°C to 85°C)
			AT28C64X-20DM/883 AT28C64X-20FM/883 AT28C64X-20LM/883	28D6 28F 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	30	0.1	AT28C64X-25DC AT28C64X-25FC AT28C64X-25JC AT28C64X-25PC AT28C64X-25SC	28D6 28F 32J 28P6 28S	Commercial (0°C to 70°C)
250	45	0.1	AT28C64X-25DI AT28C64X-25FI AT28C64X-25JI AT28C64X-25PI AT28C64X-25SI	28D6 28F 32J 28P6 28S	Industrial (-40°C to 85°C)
			AT28C64X-25DM/883 AT28C64X-25FM/883 AT28C64X-25LM/883	28D6 28F 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
300	45	0.1	AT28C64X-30DM/883 AT28C64X-30FM/883 AT28C64X-30LM/883	28D6 28F 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
350	45	0.1	AT28C64X-35DM/883 AT28C64X-35FM/883 AT28C64X-35LM/883	28D6 28F 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	45	0.1	5962-87514 22 XX 5962-87514 22 YX	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	45	0.1	5962-87514 21 XX 5962-87514 21 YX	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	45	0.1	5962-87514 20 XX 5962-87514 20 YX 5962-87514 20 ZX	28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
300	45	0.1	5962-87514 19 XX 5962-87514 19 YX	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
350	45	0.1	5962-87514 18 XX 5962-87514 18 YX	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
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32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide Plastic Dual Inline Package (PDIP)
28S	28 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)

64K (8K x 8) High Speed CMOS E^2PROM

Features

- Fast Read Access Time - 55 ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 32 Bytes
  - Internal Control Timer
- Fast Write Cycle Times
  - Maximum Page Write Cycle Time: 2 ms
  - 1 to 32 Byte Page Write Operation
- Low Power Dissipation
  - 80 mA Active Current
  - 100 µA CMOS Standby Current (28HC64L)
- Direct Microprocessor Control
  - $\overline{\text{DATA}}$ Polling
- High Reliability CMOS Technology
  - Endurance: 10^4 or 10^5 Cycles
  - Data Retention: 10 years
- Single 5 V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-Wide Pinout
- Full Military, Commercial, and Industrial Temperature Ranges

Description

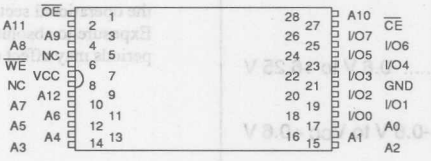
The AT28HC64/L is a high-speed, low-power Electrically Erasable and Programmable Read Only Memory. Its 64K of memory is organized as 8,192 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 55 ns with power dissipation of just 440mW. When the device is deselected the standby current is less than 100 µA.

The AT28HC64/L is accessed like a Static RAM for the read or write cycles without the need for external components. The device contains a 32-byte page register to allow writing of up to 32 bytes simultaneously. During a write cycle, the addresses and 1 to 32 bytes of data are

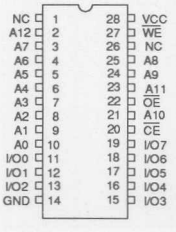
(continued on next page)

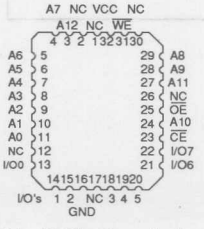
Pin Configurations

TSOP Top View



Pin Name	Function
A0 - A12	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect





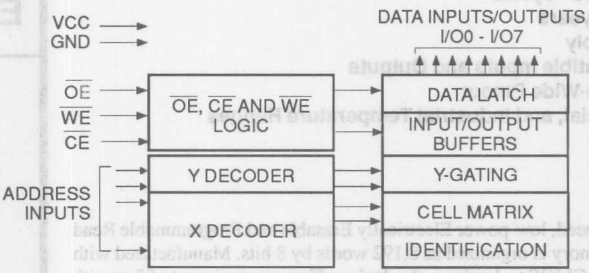
Note: PLCC package pins 1 and 17 are DON'T CONNECT.

Description (Continued)

internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{\text{DATA}}$ polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's 28HC64/L has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. The AT28HC64/L also includes an extra 32 bytes of E^2PROM for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6 V to +6.25 V
All Output Voltages with Respect to Ground	-0.6 V to V_{CC} +0.6 V
Voltage on $\overline{\text{OE}}$ and A9 with Respect to Ground	-0.6 V to +13.5 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: The AT28HC64 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

BYTE WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started it will automatically time itself to completion.

PAGE WRITE: The page write operation of the AT28HC64 allows one to thirty-two bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; the first byte written can then be followed by one to thirty-one additional bytes. Each successive byte must be written within 150 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded the AT28HC64 will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A5-A12 inputs. For each $\overline{WE}$ high to low transition during the page write operation, A5 - A12 must be the same.

The A0 to A4 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The AT28HC64 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{DATA}$ Polling may begin at anytime during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling the AT28HC64 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes to the AT28HC64 may occur during transitions of the host system power supply. Atmel has incorporated the following features that will protect the memory against inadvertent writes.

HARDWARE PROTECTION: Hardware features protect against inadvertent writes to the AT28HC64 in the following ways: (a) V_{CC} sense - if V_{CC} is below 3.8 V (typical) the write function is inhibited; (b) V_{CC} power-on delay - once V_{CC} has reached 3.8 V the device will automatically time out 5 ms (typical) before allowing a write: (c) write inhibit - holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles; (d) noise filter - pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

CHIP CLEAR: The contents of the entire memory of the AT28HC64 may be set to the high state (erased) by the use of the CHIP CLEAR operation. By setting $\overline{CE}$ low and $\overline{OE}$ to 12 volts, the chip is cleared when a 10ms low pulse is applied to the $\overline{WE}$ pin.

DEVICE IDENTIFICATION: An extra 32 bytes of E^2PROM memory are available to the user for device identification. By raising A9 to 12 V ± 0.5 V and using address locations 1FE0H to 1FFFH the additional bytes may be written to or read from in the same manner as the regular memory array.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Note: 1. This parameter is characterized and is not 100% tested.

D.C. and A.C. Operating Range

		AT28HC64-55	AT28HC64L-70	AT28HC64-70	AT28HC64/L-90	AT28HC64/L-12
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.			-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 10%	5 V ± 10%	5 V ± 10%	5 V ± 10%	5 V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H [3]	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.
3. $V_H = 12.0\ V \pm 0.5\ V$.

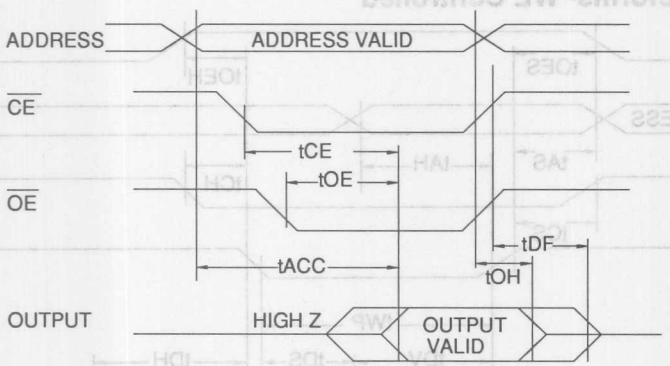
D.C. Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0 V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS AT28HC64L	$\overline{CE}$ = V_{CC}-0.3 V to V_{CC} + 1 V	Com., Ind.		100	µA
			Mil.		200	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0 V to V_{CC} + 1 V	AT28HC64L		3	mA
			AT28HC64		60	mA
I_{CC}	V_{CC} Active Current	f = 10 MHz; I_{OUT} = 0 mA			80	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 4 mA			.4	V
V_{OH}	Output High Voltage	I_{OH} = -4.0 mA		2.4		V

A.C. Read Characteristics [1]

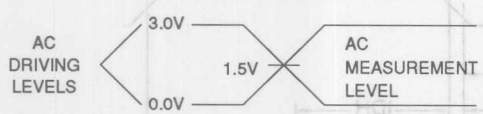
Symbol	Parameter	AT28HC64 -55 Min	AT28HC64 -55 Max	AT28HC64/L -70 Min	AT28HC64/L -70 Max	AT28HC64/L -90 Min	AT28HC64/L -90 Max	AT28HC64L -12 Min	AT28HC64L -12 Max	Units
t_{ACC}	Address to Output Delay		55		70		90		120	ns
t_{CE} [2]	$\overline{CE}$ to Output Delay		55		70		90		120	ns
t_{OE} [3]	$\overline{OE}$ to Output Delay	0	30	0	35	0	40	0	50	ns
t_{DF} [4,5]	$\overline{OE}$ to Output Float	0	30	0	35	0	40	0	50	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		ns

A.C. Read Waveforms



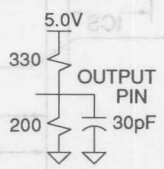
Notes:
1. C_L = 30 pF.
2. $\overline{CE}$ may be delayed up to t_{ACC} - t_{CE} after the address transition without impact on t_{ACC}.
3. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
5. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



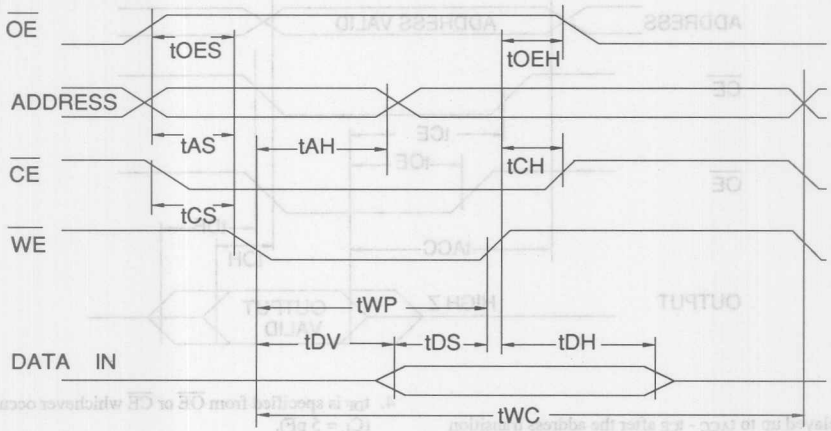
t_R, t_F < 5 ns

Output Test Load

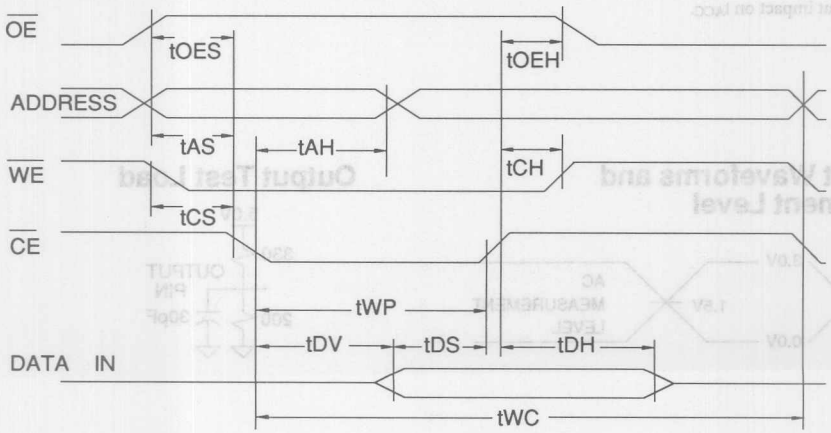


Symbol	Parameter	Min	Typ	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{CS}	Chip Select Set-up Time	0			ns
t_{CH}	Chip Select Hold Time	0			ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		1000	ns
t_{DS}	Data Set-up Time	50			ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time	0			ns
t_{DV}	Time to Data Valid			1	µs
t_{WC}	Write Cycle Time		1.0	2.0	ms

A.C. Write Waveforms- $\overline{WE}$ Controlled



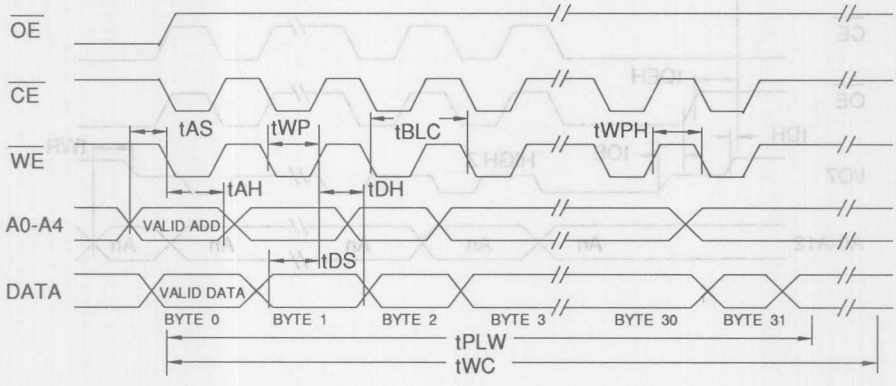
A.C. Write Waveforms- $\overline{CE}$ Controlled



Page Mode Write Characteristics

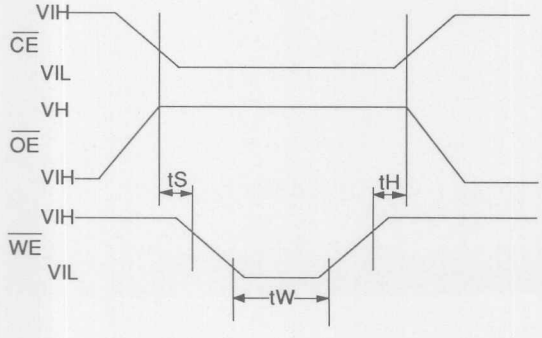
Symbol	Parameter	Min	Typ	Max	Units
t_{WC}	Write Cycle Time		1	2.0	ms
t_{AS}	Address Set-up Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{DS}	Data Set-up Time	50			ns
t_{DH}	Data Hold Time	0			ns
t_{WP}	Write Pulse Width	100		1000	ns
t_{BLC}	Byte Load Cycle Time	150			ns
t_{PLW}	Page Load Width			150	µs
t_{WPH}	Write Pulse Width High	50			ns

Page Mode Write Waveforms



Notes: A5 through A12 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Chip Erase Waveforms



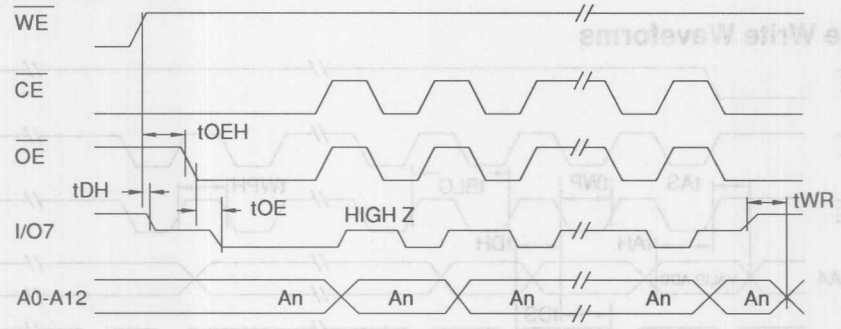
$t_S = t_H = 1$ µsec (min.)
$t_W = 10$ msec (min.)
$V_H = 12.0\ V \pm 0.5\ V$

Data Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	0			ns
t_{OE}	$\overline{OE}$ to Output Delay			50	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

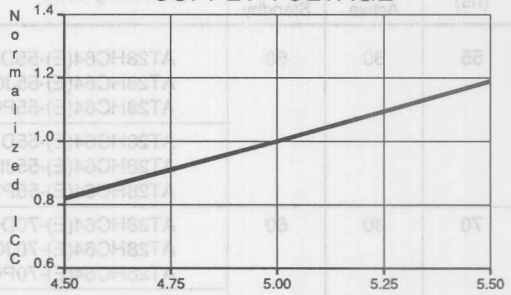
Data Polling Waveforms



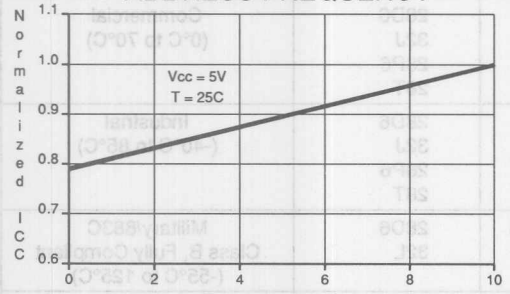
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
55	80	60	AT28HC64(E)-55DC AT28HC64(E)-55JC AT28HC64(E)-55PC	28D6 32J 28P6	Commercial (0°C to 70°C)
			AT28HC64(E)-55DI AT28HC64(E)-55JI AT28HC64(E)-55PI	28D6 32J 28P6	Industrial (-40°C to 85°C)
70	80	60	AT28HC64(E)-70DC AT28HC64(E)-70JC AT28HC64(E)-70PC	28D6 32J 28P6	Commercial (0°C to 70°C)
			AT28HC64(E)-70DI AT28HC64(E)-70JI AT28HC64(E)-70PI	28D6 32J 28P6	Industrial (-40°C to 85°C)
			AT28HC64(E)-70DM/883 AT28HC64(E)-70LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	80	60	AT28HC64(E)-90DC AT28HC64(E)-90JC AT28HC64(E)-90PC AT28HC64(E)-90TC	28D6 32J 28P6 28T	Commercial (0°C to 70°C)
			AT28HC64(E)-90DI AT28HC64(E)-90JI AT28HC64(E)-90PI AT28HC64(E)-90TI	28D6 32J 28P6 28T	Industrial (-40°C to 85°C)
			AT28HC64(E)-90DM/883 AT28HC64(E)-90LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	80	60	AT28HC64(E)-12DC AT28HC64(E)-12JC AT28HC64(E)-12PC	28D6 32J 28P6	Commercial (0°C to 70°C)
			AT28HC64(E)-12DI AT28HC64(E)-12JI AT28HC64(E)-12PI	28D6 32J 28P6	Industrial (-40°C to 85°C)
			AT28HC64(E)-12DM/883 AT28HC64(E)-12LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28T	28 Lead, Plastic Thin Small Outline Package (TSOP)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 2 ms
E	High Endurance Option: Endurance = 100K Write Cycles

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	80	0.1	AT28HC64L(E)-70DC AT28HC64L(E)-70JC AT28HC64L(E)-70PC	28D6 32J 28P6	Commercial (0°C to 70°C)
			AT28HC64L(E)-70DI AT28HC64L(E)-70JI AT28HC64L(E)-70PI	28D6 32J 28P6	Industrial (-40°C to 85°C)
90	80	0.1	AT28HC64L(E)-90DC AT28HC64L(E)-90JC AT28HC64L(E)-90PC	28D6 32J 28P6	Commercial (0°C to 70°C)
			AT28HC64L(E)-90DI AT28HC64L(E)-90JI AT28HC64L(E)-90PI	28D6 32J 28P6	Industrial (-40°C to 85°C)
90	80	0.2	AT28HC64L(E)-90DM/883 AT28HC64L(E)-90LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	80	0.1	AT28HC64L(E)-12DC AT28HC64L(E)-12JC AT28HC64L(E)-12PC AT28HC64L-W	28D6 32J 28P6 DIE	Commercial (0°C to 70°C)
			AT28HC64L(E)-12DI AT28HC64L(E)-12JI AT28HC64L(E)-12PI	28D6 32J 28P6	Industrial (-40°C to 85°C)
120	80	0.2	AT28HC64L(E)-12DM/883 AT28HC64L(E)-12LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
70	80	0.2	5962-87514 12 XX 5962-87514 12 YX	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	80	0.2	5962-87514 11 XX 5962-87514 11 YX	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	80	0.2	5962-87514 10 XX 5962-87514 10 YX	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 2 ms
E	High Endurance Option: Endurance = 100K Write Cycles

Ordering Information

t_{ACC} (ns)	I_{CC} (mA) Active	I_{CC} (mA) Standby	Ordering Code	Package	Operation Range
70	80	0.1	AT28HC64L(E)-70DC AT28HC64L(E)-70JC AT28HC64L(E)-70PC	28DB 32J 28P6	Commercial (0°C to 70°C)
			AT28HC64L(E)-70DI AT28HC64L(E)-70JI AT28HC64L(E)-70PI	28DB 32J 28P6	Industrial (-40°C to 85°C)
90	80	0.1	AT28HC64L(E)-90DC AT28HC64L(E)-90JC AT28HC64L(E)-90PC	28DB 32J 28P6	Commercial (0°C to 70°C)
			AT28HC64L(E)-90DI AT28HC64L(E)-90JI AT28HC64L(E)-90PI	28DB 32J 28P6	Industrial (-40°C to 85°C)
90	80	0.2	AT28HC64L(E)-90DM/883 AT28HC64L(E)-90LM/883	28DB 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	80	0.1	AT28HC64L(E)-12DC AT28HC64L(E)-12JC AT28HC64L(E)-12PC AT28HC64L-W	28DB 32J 28P6 DIE	Commercial (0°C to 70°C)
			AT28HC64L(E)-12DI AT28HC64L(E)-12JI AT28HC64L(E)-12PI	28DB 32J 28P6	Industrial (-40°C to 85°C)
120	80	0.2	AT28HC64L(E)-12DM/883 AT28HC64L(E)-12LM/883	28DB 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
70	80	0.2	5962-87514 12 XX 5962-87514 12 YX	28DB 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	80	0.2	5962-87514 11 XX 5962-87514 11 YX	28DB 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	80	0.2	5962-87514 10 XX 5962-87514 10 YX	28DB 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
28DB	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 2 ms
E	High Endurance Option: Endurance = 100K Write Cycles

2

64K (8K x 8) Low Voltage CMOS E^2PROM

Preliminary

Features

- 2.7 V to 3.6 V Supply
  - Full Read and Write Operation
- Low Power Dissipation
  - 8 mA Active Current
  - 50 µA CMOS Standby Current
- Read Access Time - 200 ns
- Byte Write - 3 ms
- Direct Microprocessor Control
  - DATA Polling
  - READY/BUSY Open Drain Output
- High Reliability CMOS Technology
  - Endurance: 100,000 Cycles
  - Data Retention: 10 years
- Low Voltage CMOS Compatible Inputs and Outputs
- JEDEC Approved Byte-Wide Pinout
- Commercial and Industrial Temperature Ranges

Description

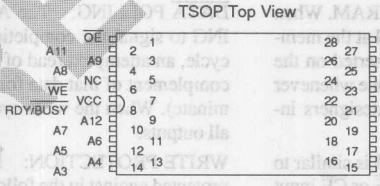
The AT28LV64 is a low-voltage, low-power Electrically Erasable and Programmable Read Only Memory. Its 64K of memory is organized 8,192 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 200 ns with power dissipation less than 30 mW. When the device is deselected the standby current is less than 50 µA.

The AT28LV64 is accessed like a Static RAM for the read or write cycles without the need for external components. During a byte write, the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. The device includes two methods for detecting the end of a write cycle, level detection of RDY/$\overline{BUSY}$ and $\overline{DATA}$ polling of I/O_7. Once the end of a write cycle has been detected, a new access for a read or write can begin.

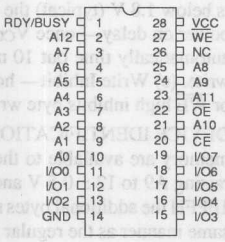
Atmel's 28LV64 has additional features to ensure high quality and manufacturability. The device utilizes error correction internally for extended endurance and for improved data retention characteristics. An extra 32 bytes of E^2PROM are available for device identification or tracking.

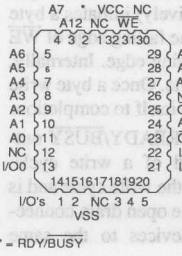
Pin Configurations

TSOP Top View



Pin Name	Function
A0 - A12	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/ Outputs
RDY/$\overline{BUSY}$	Ready/$\overline{Busy}$ Output
NC	No Connect

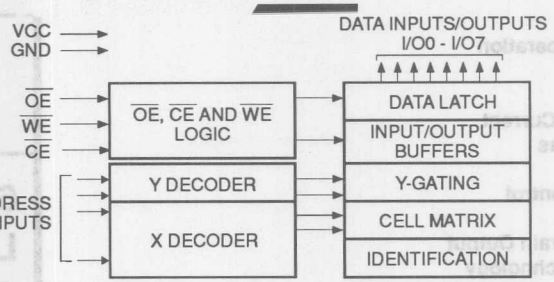




* = RDY/$\overline{BUSY}$

Note: PLCC package pins 1 and 17 are DON'T CONNECT.

PRELIMINARY



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6 V to +6.25 V
All Output Voltages with Respect to Ground	-0.6 V to V_{CC} +0.6 V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6 V to +13.5 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: The AT28LV64 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers increased flexibility in preventing bus contention.

BYTE WRITE: Writing data into the AT28LV64 is similar to writing into a Static RAM. A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{OE}$ high and $\overline{CE}$ or $\overline{WE}$ low (respectively) initiates a byte write. The address location is latched on the falling edge of $\overline{WE}$ (or $\overline{CE}$); the new data is latched on the rising edge. Internally, the device performs a self-clear before write. Once a byte write has been started, it will automatically time itself to completion.

READY/$\overline{BUSY}$: Pin 1 is an open drain READY/$\overline{BUSY}$ output that can be used to detect the end of a write cycle. RDY/$\overline{BUSY}$ is actively pulled low during the write cycle and is released at the completion of the write. The open drain connection allows for OR-tying of several devices to the same RDY/$\overline{BUSY}$ line.

$\overline{DATA}$ POLLING: The AT28LV64 provides $\overline{DATA}$ POLLING to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the complement of that data for I/O_7 (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

WRITE PROTECTION: Inadvertent writes to the device are protected against in the following ways. (a) V_{CC} sense— if V_{CC} is below 1.8 V (typical) the write function is inhibited. (b) V_{CC} power on delay— once V_{CC} has reached 2.0 V the device will automatically time out 10 ms (typical) before allowing a byte write. (c) Write Inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits byte write cycles.

DEVICE IDENTIFICATION: An extra 32 bytes of E^2PROM memory are available to the user for device identification. By raising A9 to 12 ± 0.5 V and using address locations 1FE0H to 1FFFH the additional bytes may be written to or read from in the same manner as the regular memory array.

D.C. and A.C. Operating Range

		AT28LV64-20	AT28LV64-30
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		3.0 V to 3.6 V	2.7 V to 3.6 V

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z

Notes: 1. X can be V_{IL} or V_{IH}. 2. Refer to A.C. Programming Waveforms.

D.C. Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC} + 1.0 V		5	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0 V to V_{CC}		5	µA
I_{SB}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3 V to V_{CC} + 1.0 V		50	µA
I_{CC}	V_{CC} Active Current A.C.	f = 5 MHz; I_{OUT} = 0 mA $\overline{CE}$ = V_{IL}		8	mA
V_{IL}	Input Low Voltage			0.6	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 1 mA		0.3	V
		I_{OL} = 2 mA for RDY/$\overline{BUSY}$		0.3	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA	2.0		V

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

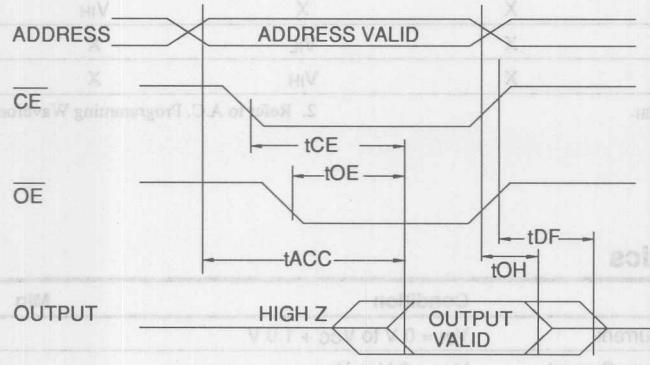
	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Note: 1. This parameter is characterized and is not 100% tested.

A.C. Read Characteristics

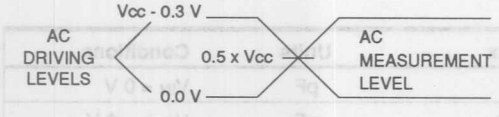
Symbol	Parameter	AT28LV64-20 Min	AT28LV64-20 Max	AT28LV64-30 Min	AT28LV64-30 Max	Units
t_{ACC}	Address to Output Delay		200		300	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		200		300	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	80	0	150	ns
t_{DF} (3,4)	$\overline{CE}$ or $\overline{OE}$ High to Output Float	0	55	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		ns

A.C. Read Waveforms



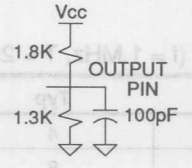
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 20 ns

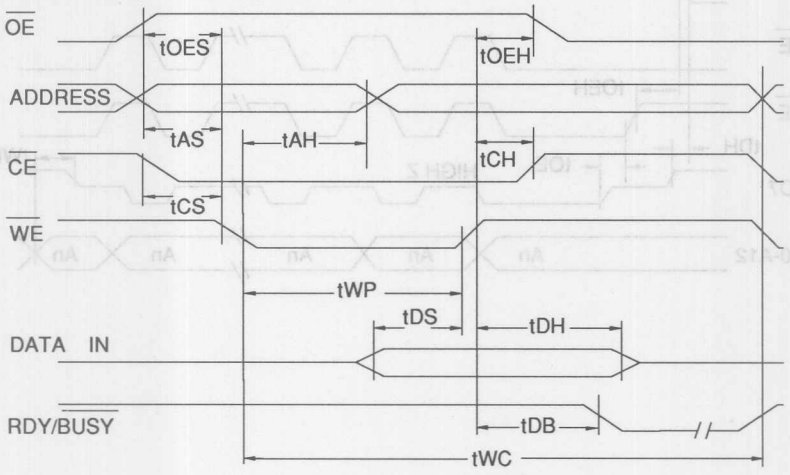
Output Test Load



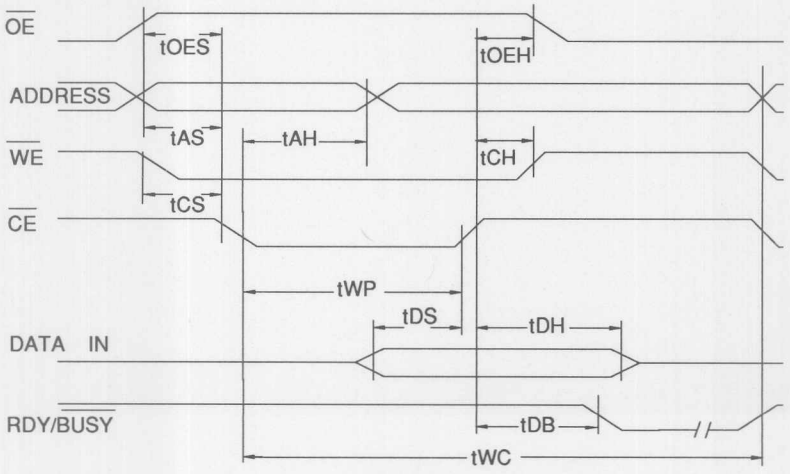
A.C. Write Characteristics

Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	10		ns
t_{AH}	Address Hold Time	100		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	150	1000	ns
t_{DS}	Data Set-up Time	100		ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time	10		ns
t_{DB}	Time to Device Busy		50	ns
t_{WC}	Write Cycle Time		3	ms

A.C. Write Waveforms- $\overline{WE}$ Controlled



A.C. Write Waveforms- $\overline{CE}$ Controlled

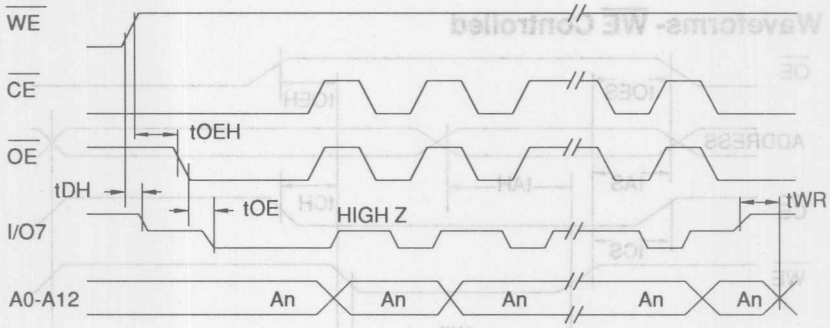


$\overline{\text{Data}}$ Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{Data}}$ Polling Waveforms



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Operating Voltage	Ordering Code	Package	Operation Range
	Active	Standby				
200	8	0.05	3.0 V to 3.6 V	AT28LV64-20JC AT28LV64-20PC AT28LV64-20SC AT28LV64-20TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
200	8	0.05	3.0 V to 3.6 V	AT28LV64-20JI AT28LV64-20PI AT28LV64-20SI AT28LV64-20TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)
300	8	0.05	2.7 V to 3.6 V	AT28LV64-30JC AT28LV64-30PC AT28LV64-30SC AT28LV64-30TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
300	8	0.05	2.7 V to 3.6 V	AT28LV64-30JI AT28LV64-30PI AT28LV64-30SI AT28LV64-30TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28S	28 Lead, 0.300" Wide, Plastic Gull Wing, Small Outline (SOIC)
28T	28 Lead, Plastic Thin Small Outline Package (TSOP)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Operating Voltage	Ordering Code	Package	Operation Range
	Active	Standby				
200	8	0.05	3.0 V to 3.6 V	AT28LV64-20JC AT28LV64-20PC AT28LV64-20SC AT28LV64-20TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
200	8	0.05	3.0 V to 3.6 V	AT28LV64-20JI AT28LV64-20PI AT28LV64-20SI AT28LV64-20TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)
200	8	0.05	2.7 V to 3.6 V	AT28LV64-30JC AT28LV64-30PC AT28LV64-30SC AT28LV64-30TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
200	8	0.05	2.7 V to 3.6 V	AT28LV64-30JI AT28LV64-30PI AT28LV64-30SI AT28LV64-30TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28S	28 Lead, 0.300" Wide, Plastic Gull Wing, Small Outline (SOIC)
28T	28 Lead, Plastic Thin Small Outline Package (TSOP)

64K (8K x 8) CMOS E²PROM with Software Data Protection

Features

- Fast Read Access Time - 150 ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 64 Bytes
- Fast Write Cycle Times
  - Page Write Cycle Time: 2 ms maximum
  - 1 to 64 Byte Page Write Operation
- Low Power Dissipation
  - 60 mA Active Current
  - 100 µA CMOS Standby Current
- Hardware and Software Data Protection
- $\overline{\text{DATA}}$ Polling and Toggle Bit for End of Write Detection
- High Reliability CMOS Technology
  - Endurance: 100,000 Cycles
  - Data Retention: 10 years
- Single 5 V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-Wide Pinout
- Full Military, Commercial, and Industrial Temperature Ranges

Description

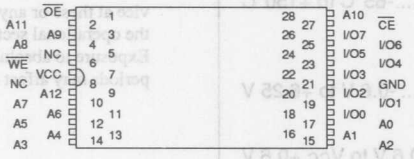
The AT28C64B is a high-performance Electrically Erasable and Programmable Read Only Memory. Its 64K of memory is organized as 8,192 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 150 ns with power dissipation of just 440 mW. When the device is deselected, the CMOS standby current is less than 100 µA.

The AT28C64B is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow writing of up to 64 bytes simultaneously. During a write cycle, the addresses and 1 to 64 bytes of data are inter-

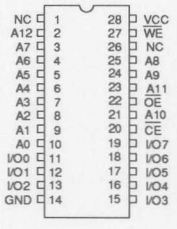
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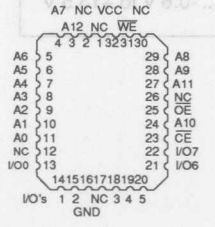
Pin Configurations

TSOP Top View



Pin Name	Function
A0 - A12	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect





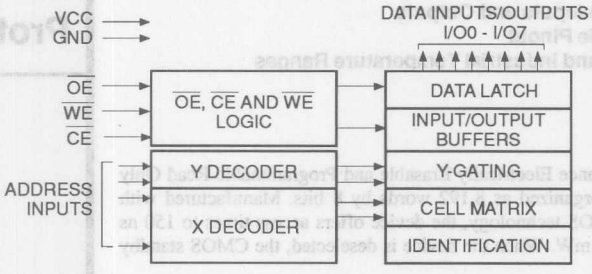
Note: PLCC package pins 1 and 17 are DON'T CONNECT.

Description (Continued)

nally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{DATA}$ polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's 28C64B has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64 bytes of E^2PROM for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6 V to +6.25 V
All Output Voltages with Respect to Ground	-0.6 V to V_{CC} +0.6 V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6 V to +13.5 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: The AT28C64B is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high-impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers flexibility in preventing bus contention in their system.

BYTE WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started it will automatically time itself to completion.

PAGE WRITE: The page write operation of the AT28C64B allows one to 64 bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; after the first byte is written, it can then be followed by one to 63 additional bytes. Each successive byte must be loaded within 150 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded the AT28C64B will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A6-A12 inputs. For each $\overline{WE}$ high to low transition during the page write operation, A6 - A12 must be the same.

The A0 to A5 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The AT28C64B features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{DATA}$ Polling may begin at anytime during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling the AT28C64B provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Atmel has incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE PROTECTION: Hardware features protect against inadvertent writes to the AT28C64B in the following ways: (a) V_{CC} sense - if V_{CC} is below 3.8 V (typical) the write function is inhibited; (b) V_{CC} power-on delay - once V_{CC} has reached 3.8 V the device will automatically time out 5 ms (typical) before allowing a write; (c) write inhibit - holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles; (d) noise filter - pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature has been implemented on the AT28C64B. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the AT28C64B is shipped from Atmel with SDP disabled.

SDP is enabled by the user issuing a series of three write commands; three specific bytes of data are written to three specific addresses (refer to Software Data Protection Algorithm). After writing the three-byte command sequence and t_{WC} the entire AT28C64B will be protected against inadvertent writes. It should be noted that once protected the user may still perform a byte or page write to the AT28C64B. This is done by preceding the data to be written by the same three-byte command sequence used to enable SDP.

Once set, SDP will remain active unless the disable command sequence is issued. Power transitions do not disable SDP and SDP will protect the AT28C64B during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not actually written into the device; their addresses may still be written with user data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the three-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, read operations will effectively be polling operations.

DEVICE IDENTIFICATION: An extra 64 bytes of E^2PROM memory are available to the user for device identification. By raising A9 to 12 V ±0.5 V and using address locations 1FC0H to 1FFFH the additional bytes may be written to or read from in the same manner as the regular memory array.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Note: 1. This parameter is characterized and is not 100% tested.

D.C. and A.C. Operating Range

		AT28C64B-15	AT28C64B-20	AT28C64B-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 10%	5 V ± 10%	5 V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write(2)	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X(1)	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H (3)	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.
3. $V_H = 12.0\ V \pm 0.5\ V$.

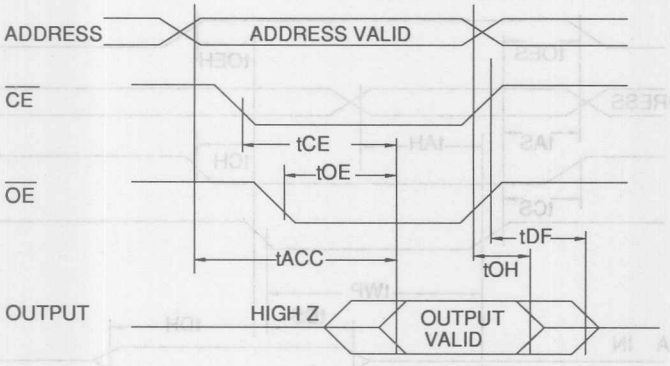
D.C. Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC} + 1 V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0 V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$= V_{CC}-0.3 V to V_{CC} + 1 V	Com., Ind.		100	µA
			Mil.		200	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0 V to V_{CC} + 1 V			2	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA			60	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			.40	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA		2.4		V

A.C. Read Characteristics

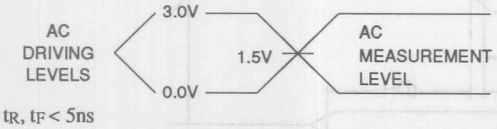
Symbol	Parameter	AT28C64B-15 Min	AT28C64B-15 Max	AT28C64B-20 Min	AT28C64B-20 Max	AT28C64B-25 Min	AT28C64B-25 Max	Units
t_{ACC}	Address to Output Delay		150		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		150		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	70	0	80	0	100	ns
t_{DF} (3,4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	50	0	55	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

A.C. Read Waveforms



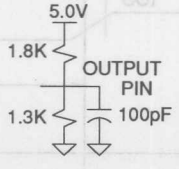
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5ns

Output Test Load

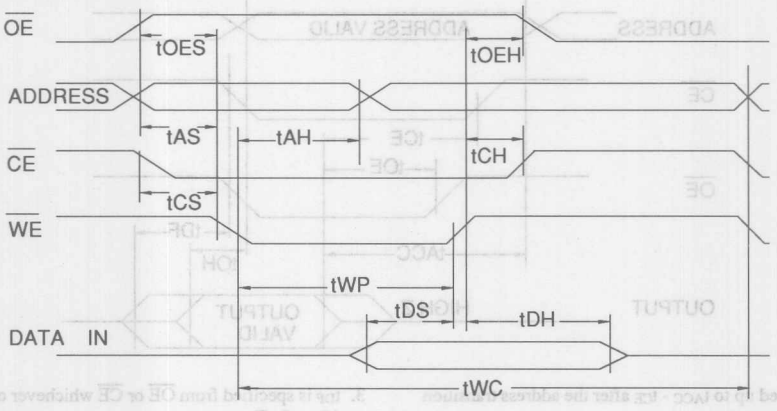


A.C. Write Characteristics

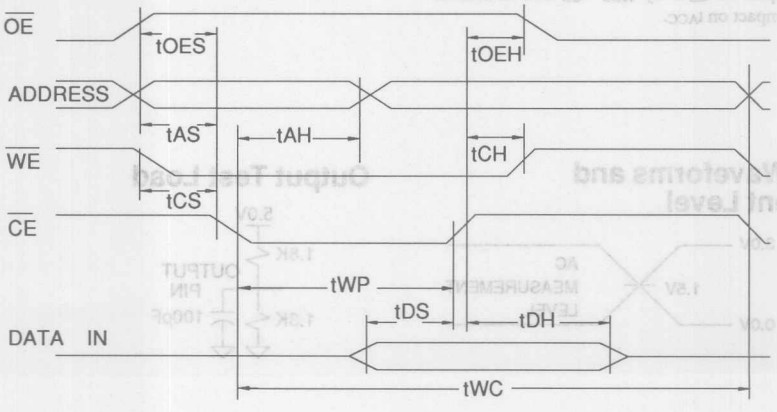
Symbol	Parameter		Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time		0		ns
t_{AH}	Address Hold Time		50		ns
t_{CS}	Chip Select Set-up Time		0		ns
t_{CH}	Chip Select Hold Time		0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)		100		ns
t_{DS}	Data Set-up Time		50		ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time		0		ns
t_{WC}	Write Cycle Time	AT28C256		2	ms

Note: 1. NR = No Restiction

A.C. Write Waveforms- $\overline{WE}$ Controlled



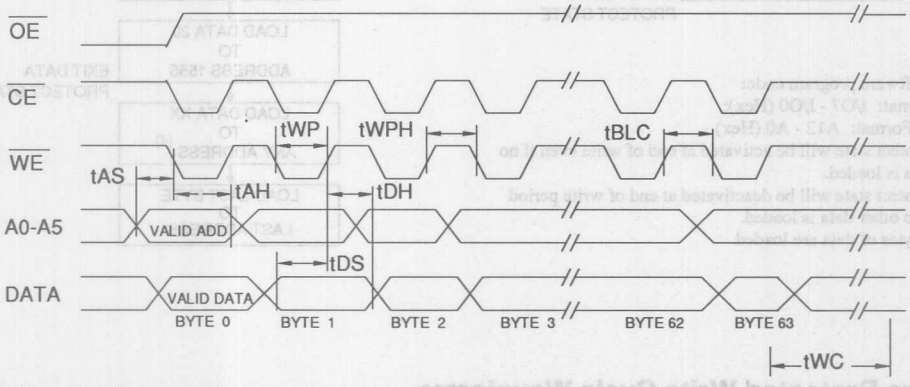
A.C. Write Waveforms- $\overline{CE}$ Controlled



Page Mode Characteristics

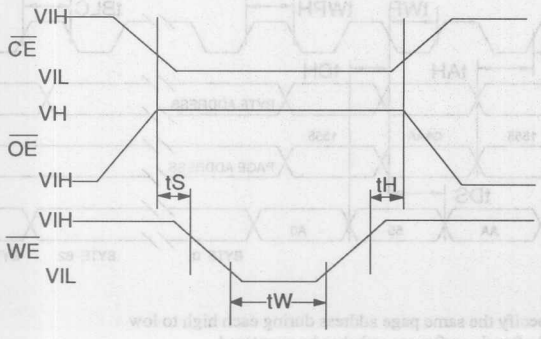
Symbol	Parameter		Min	Max	Units
t_{WC}	Write Cycle Time	AT28C256		2	ms
t_{AS}	Address Set-up Time		0		ns
t_{AH}	Address Hold Time		50		ns
t_{DS}	Data Set-up Time		50		ns
t_{DH}	Data Hold Time		0		ns
t_{WP}	Write Pulse Width		100		ns
t_{BLC}	Byte Load Cycle Time			150	µs
t_{WPH}	Write Pulse Width High		50		ns

Page Mode Write Waveforms



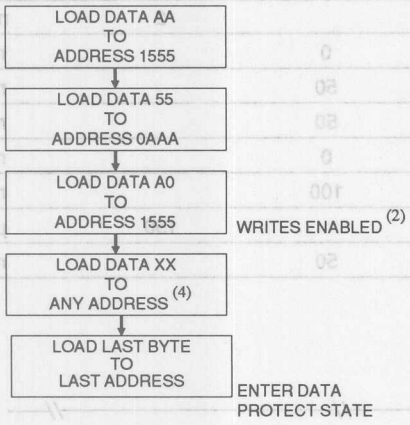
Notes: A6 through A12 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Chip Erase Waveforms

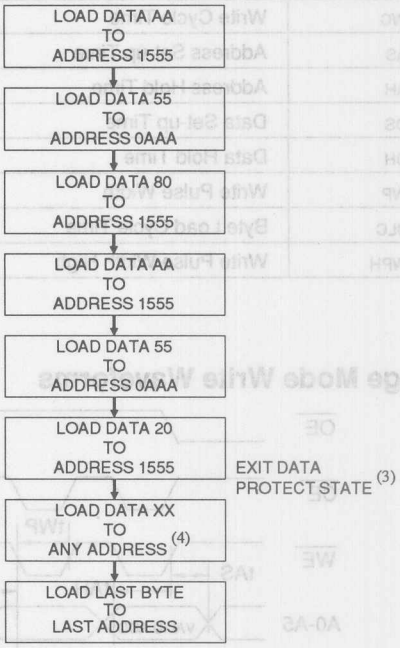


$t_S = t_H = 5$ µsec (min.)
$t_W = 10$ msec (min.)
$V_H = 12.0\ V \pm 0.5\ V$

Software Data Protection Enable Algorithm [1]

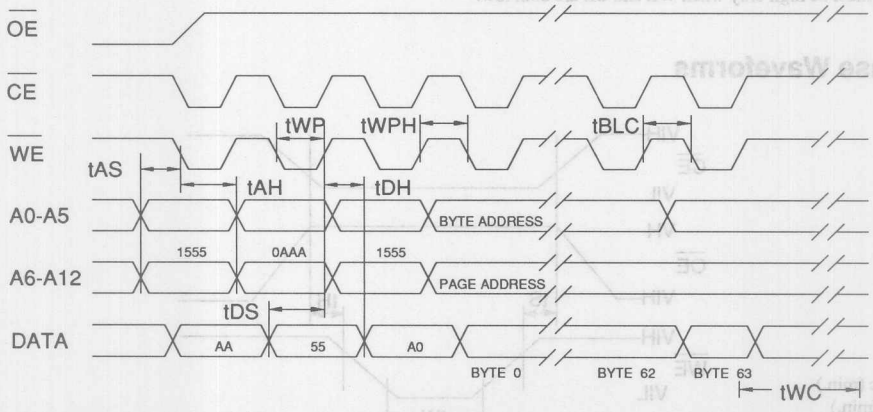


Software Data Protection Disable Algorithm [1]



Notes for software program code:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A12 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 64 bytes of data are loaded.

Software Protected Write Cycle Waveforms



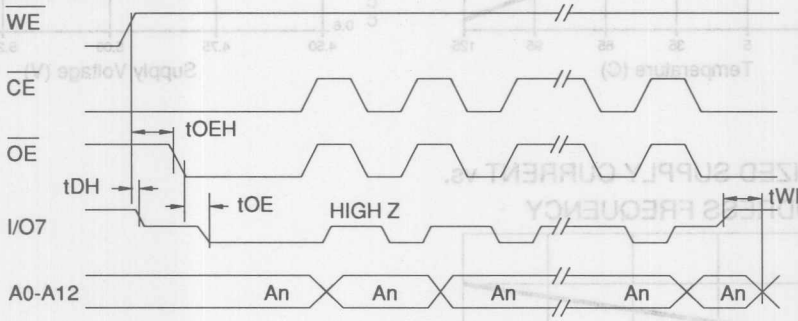
Notes: A6 through A12 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

$\overline{\text{Data}}$ Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	0			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{Data}}$ Polling Waveforms

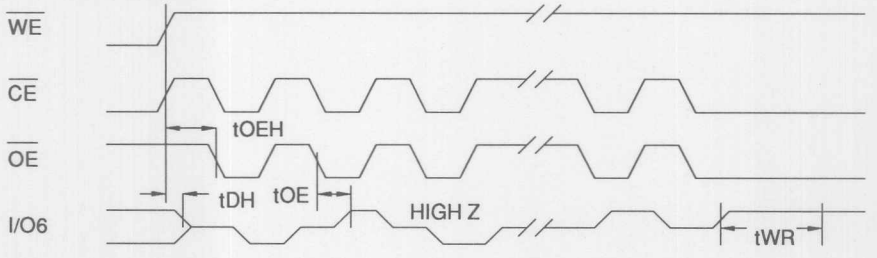


Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

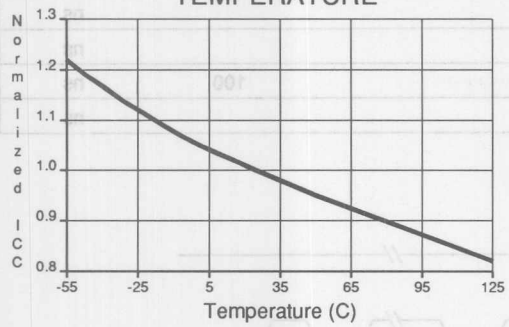
Note: 1. These parameters are characterized and not 100% tested.

Toggle Bit Waveforms

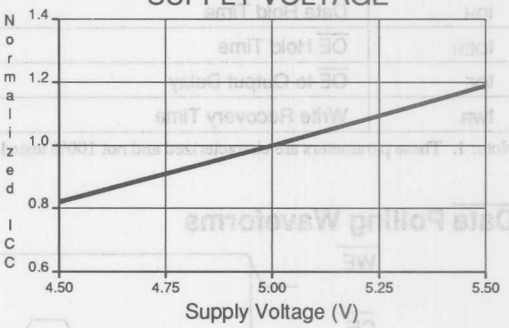


Notes:
1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

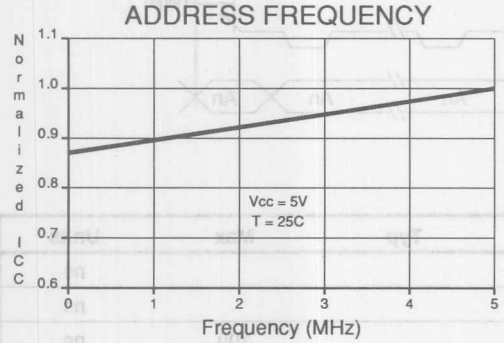
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	60	0.1	AT28C64B-15DC AT28C64B-15JC AT28C64B-15PC AT28C64B-15SC AT28C64B-15TC	28D6 32J 28P6 28S 28T	Commercial (0°C to 70°C)
			AT28C64B-15DI AT28C64B-15JI AT28C64B-15PI AT28C64B-15SI AT28C64B-15TI	28D6 32J 28P6 28S 28T	Industrial (-40°C to 85°C)
150	80	0.2	AT28C64B-15DM/883 AT28C64B-15UM/883	28D6 28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	60	0.1	AT28C64B-20DC AT28C64B-20JC AT28C64B-20PC AT28C64B-20SC AT28C64B-20TC	28D6 32J 28P6 28S 28T	Commercial (0°C to 70°C)
			AT28C64B-20DI AT28C64B-20JI AT28C64B-20PI AT28C64B-20SI AT28C64B-20TI	28D6 32J 28P6 28S 28T	Industrial (-40°C to 85°C)
200	80	0.2	AT28C64B-20DM/883 AT28C64B-20UM/883	28D6 28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	60	0.1	AT28C64B-25DC AT28C64B-25JC AT28C64B-25PC AT28C64B-25SC AT28C64B-25TC	28D6 32J 28P6 28S 28T	Commercial (0°C to 70°C)
			AT28C64B-25DI AT28C64B-25JI AT28C64B-25PI AT28C64B-25SI AT28C64B-25TI	28D6 32J 28P6 28S 28T	Industrial (-40°C to 85°C)
250	80	0.2	AT28C64B-25DM/883 AT28C64B-25UM/883	28D6 28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28S	28 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
28T	28 Lead, Plastic Thin Small Outline Package (TSOP)
28U	28 Pin, Ceramic Pin Grid Array (PGA)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA) Active	I_{CC} (mA) Standby	Ordering Code	Package	Operation Range
150	60	0.1	AT28C64B-15DC AT28C64B-15JC AT28C64B-15PC AT28C64B-15SC AT28C64B-15TC	28DB 32J 28P6 28S 28T	Commercial (0°C to 70°C)
			AT28C64B-15DI AT28C64B-15JI AT28C64B-15PI AT28C64B-15SI AT28C64B-15TI	28DB 32J 28P6 28S 28T	Industrial (-40°C to 85°C)
150	80	0.2	AT28C64B-15DM/883 AT28C64B-15UM/883	28DB 28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	60	0.1	AT28C64B-20DC AT28C64B-20JC AT28C64B-20PC AT28C64B-20SC AT28C64B-20TC	28DB 32J 28P6 28S 28T	Commercial (0°C to 70°C)
			AT28C64B-20DI AT28C64B-20JI AT28C64B-20PI AT28C64B-20SI AT28C64B-20TI	28DB 32J 28P6 28S 28T	Industrial (-40°C to 85°C)
200	80	0.2	AT28C64B-20DM/883 AT28C64B-20UM/883	28DB 28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	60	0.1	AT28C64B-25DC AT28C64B-25JC AT28C64B-25PC AT28C64B-25SC AT28C64B-25TC	28DB 32J 28P6 28S 28T	Commercial (0°C to 70°C)
			AT28C64B-25DI AT28C64B-25JI AT28C64B-25PI AT28C64B-25SI AT28C64B-25TI	28DB 32J 28P6 28S 28T	Industrial (-40°C to 85°C)
250	80	0.2	AT28C64B-25DM/883 AT28C64B-25UM/883	28DB 28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
28DB	28 Lead, 0.600" Wide, Non-Windowed Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28S	28 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
28T	28 Lead, Plastic Thin Small Outline Package (TSOP)
28U	28 Pin, Ceramic Pin Grid Array (PGA)

64K (8K x 8) Paged CMOS E^2PROM

Features

- **Fast Read Access Time - 150 ns**
- **Automatic Page Write Operation**
  - **Internal Address and Data Latches for 32 Bytes**
  - **Internal Control Timer**
- **Fast Write Cycle Times**
  - **Maximum Page Write Cycle Time: 2 ms**
  - **1 to 32 Byte Page Write Operation**
- **Low Power Dissipation**
  - **80 mA Active Current**
  - **100 µA CMOS Standby Current**
- **Direct Microprocessor Control**
  - **DATA Polling**
- **High Reliability CMOS Technology**
  - **Endurance: 10^4 or 10^5 Cycles**
  - **Data Retention: 10 years**
- **Single 5 V ± 10% Supply**
- **CMOS and TTL Compatible Inputs and Outputs**
- **JEDEC Approved Byte-Wide Pinout**
- **Full Military, Commercial, and Industrial Temperature Ranges**

Description

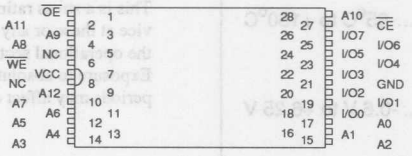
The AT28PC64 is a high-speed, low-power Electrically Erasable and Programmable Read Only Memory. Its 64K of memory is organized as 8,192 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 150 ns with power dissipation of just 440 mW. When the device is deselected the standby current is less than 100 µA.

The AT28PC64 is accessed like a Static RAM for the read or write cycles without the need for external components. The device contains a 32-byte page register to allow writing of up to 32 bytes simultaneously. During a write cycle, the addresses and 1 to 32 bytes of data are

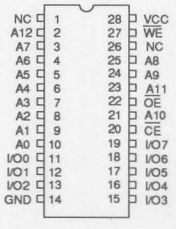
(continued on next page)

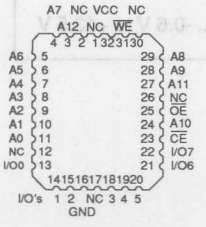
Pin Configurations

TSOP Top View



Pin Name	Function
A0 - A12	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect





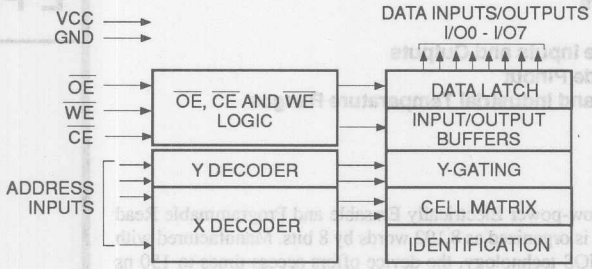
Note: PLCC package pins 1 and 17 are DON'T CONNECT.

Description (Continued)

internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{\text{DATA}}$ polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's 28PC64 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. The AT28PC64 also includes an extra 32 bytes of E^2PROM for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6 V to +6.25 V
All Output Voltages with Respect to Ground	-0.6 V to V_{CC} +0.6 V
Voltage on $\overline{\text{OE}}$ and A9 with Respect to Ground	-0.6 V to +13.5 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: The AT28PC64 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

BYTE WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started it will automatically time itself to completion.

PAGE WRITE: The page write operation of the AT28PC64 allows one to thirty-two bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; the first byte written can then be followed by one to thirty-one additional bytes. Each successive byte must be written within 150 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded the AT28PC64 will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A5-A12 inputs. For each $\overline{WE}$ high to low transition during the page write operation, A5 - A12 must be the same.

The A0 to A4 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The AT28PC64 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{DATA}$ Polling may begin at anytime during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling the AT28PC64 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes to the AT28PC64 may occur during transitions of the host system power supply. Atmel has incorporated the following features that will protect the memory against inadvertent writes.

HARDWARE PROTECTION: Hardware features protect against inadvertent writes to the AT28PC64 in the following ways: (a) V_{CC} sense - if V_{CC} is below 3.8 V (typical) the write function is inhibited; (b) V_{CC} power-on delay - once V_{CC} has reached 3.8 V the device will automatically time out 5 ms typical) before allowing a write: (c) write inhibit - holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles; (d) noise filter - pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

CHIP CLEAR: The contents of the entire memory of the AT28PC64 may be set to the high state (erased) by the use of the CHIP CLEAR operation. By setting $\overline{CE}$ low and $\overline{OE}$ to 12 volts, the chip is cleared when a 10 ms low pulse is applied to the $\overline{WE}$ pin.

DEVICE IDENTIFICATION: An extra 32 bytes of E^2PROM memory are available to the user for device identification. By raising A9 to 12 V ± 0.5 V and using address locations 1FE0H to 1FFFH the additional bytes may be written to or read from in the same manner as the regular memory array.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Note: 1. This parameter is characterized and is not 100% tested.

D.C. and A.C. Operating Range

		AT28PC64-15	AT28PC64-20	AT28PC64-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 10%	5 V ± 10%	5 V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H [3]	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.
3. $V_H = 12.0\ V \pm 0.5\ V$.

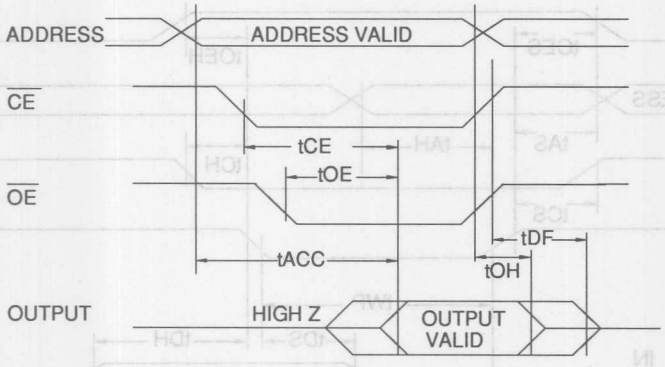
D.C. Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	$V_{IN} = 0\ V$ to $V_{CC} + 1V$			10	µA
I_{LO}	Output Leakage Current	$V_{I/O} = 0\ V$ to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE} = V_{CC}-0.3\ V$ to $V_{CC} + 1\ V$	Com., Ind.		100	µA
			Mil.		200	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE} = 2.0\ V$ to $V_{CC} + 1\ V$			3	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; $I_{OUT} = 0$ mA			80	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA			.4	V
V_{OH}	Output High Voltage	$I_{OH} = -400$ µA		2.4		V

A.C. Characteristics [1]

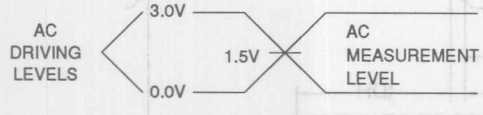
Symbol	Parameter	AT28PC64-15 Min	AT28PC64-15 Max	AT28PC64-20 Min	AT28PC64-20 Max	AT28PC64-25 Min	AT28PC64-25 Max	Units
t_{ACC}	Address to Output Delay		150		200		250	ns
t_{CE} [2]	$\overline{CE}$ to Output Delay		150		200		250	ns
t_{OE} [3]	$\overline{OE}$ to Output Delay	0	70	0	80	0	100	ns
t_{DF} [4,5]	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	50	0	55	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

A.C. Read Waveforms



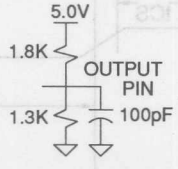
Notes:
1. C_L = 100 pF.
2. $\overline{CE}$ may be delayed up to t_{ACC} - t_{CE} after the address transition without impact on t_{ACC}.
3. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
5. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

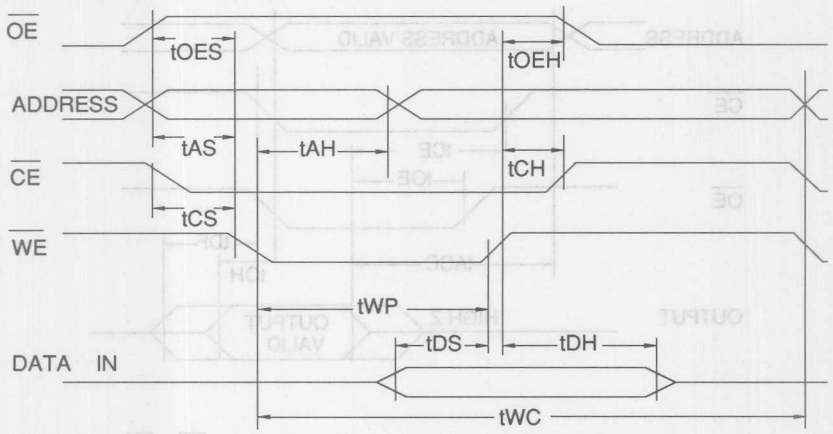
Output Test Load



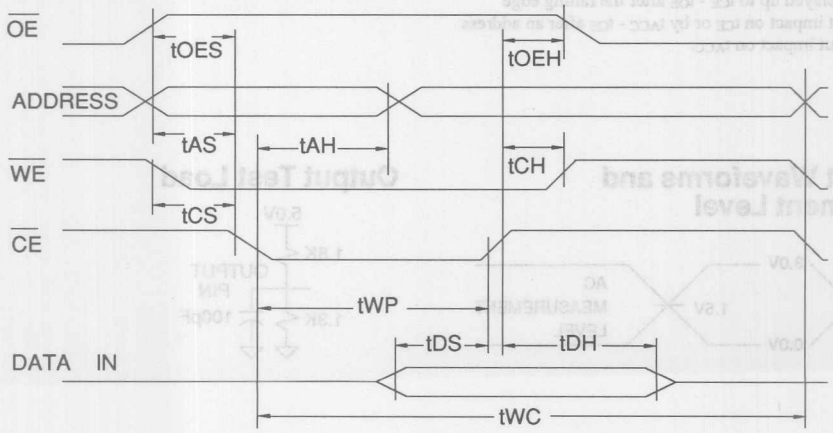
A.C. Write Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{CS}	Chip Select Set-up Time	0			ns
t_{CH}	Chip Select Hold Time	0			ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		1000	ns
t_{DS}	Data Set-up Time	50			ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time	0			ns
t_{WC}	Write Cycle Time		1.0	2.0	ms

A.C. Write Waveforms- $\overline{WE}$ Controlled



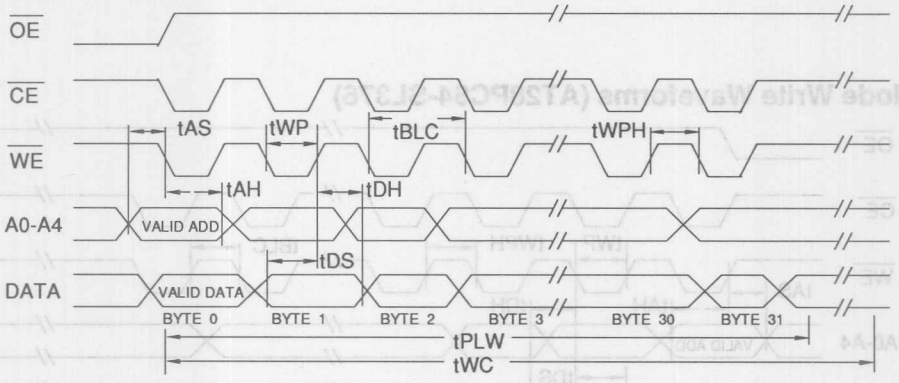
A.C. Write Waveforms- $\overline{CE}$ Controlled



Page Mode Write Characteristics

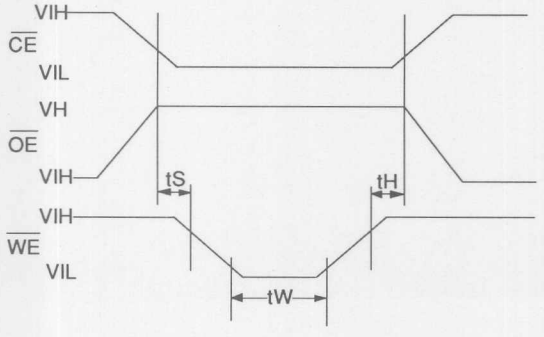
Symbol	Parameter	Min	Typ	Max	Units
t_{WC}	Write Cycle Time		1	2.0	ms
t_{AS}	Address Set-up Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{DS}	Data Set-up Time	50			ns
t_{DH}	Data Hold Time	0			ns
t_{WP}	Write Pulse Width	100		1000	ns
t_{BLC}	Byte Load Cycle Time	150			ns
t_{PLW}	Page Load Width			150	µs
t_{WPH}	Write Pulse Width High	50			ns

Page Mode Write Waveforms



Notes: A5 through A12 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Chip Erase Waveforms



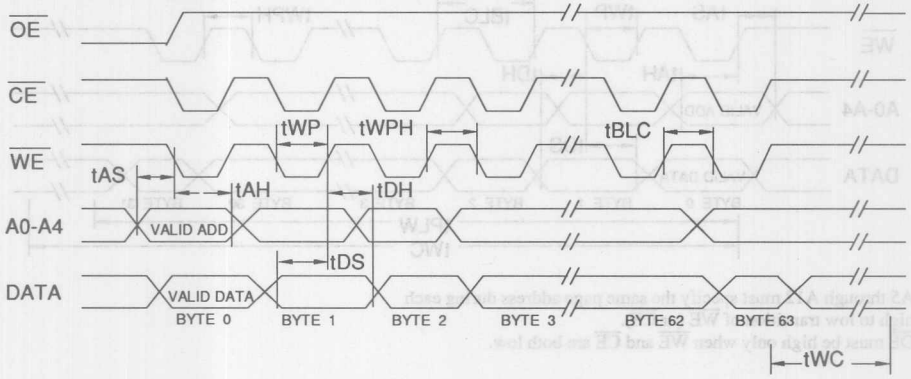
$t_S = t_H = 1$ µsec (min.)
$t_W = 10$ msec (min.)
$V_H = 12.0\ V \pm 0.5\ V$

Note: Some systems require increased load cycle time, beyond that permitted by the AT28PC64. The following Page Mode Write Characteristics and Waveforms address this situation. Please reference Atmel part number AT28PC64-SL376 to specify this device.

Page Mode Write Characteristics (AT28PC64-SL376)

Symbol	Parameter	Min	Typ	Max	Units
t_{WC}	Write Cycle Time		1	2.0	ms
t_{AS}	Address Set-up Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{DS}	Data Set-up Time	50			ns
t_{DH}	Data Hold Time	0			ns
t_{WP}	Write Pulse Width	100			ns
t_{BLC}	Byte Load Cycle Time			150	µs
t_{WPH}	Write Pulse Width High	50			ns

Page Mode Write Waveforms (AT28PC64-SL376)



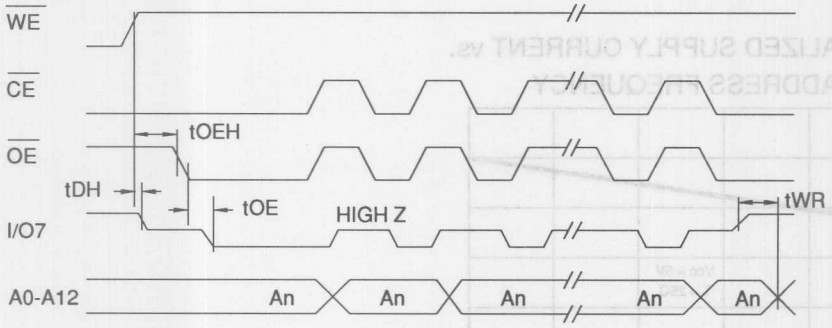
Notes: A5 through A12 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

$\overline{\text{Data}}$ Polling Characteristics[1]

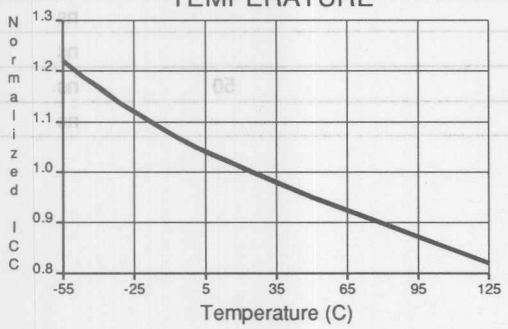
Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	0			ns
t_{OE}	$\overline{OE}$ to Output Delay			50	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

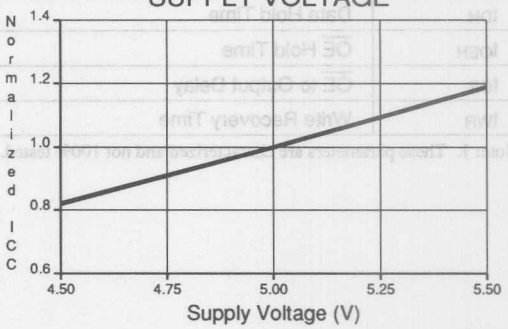
$\overline{\text{Data}}$ Polling Waveforms



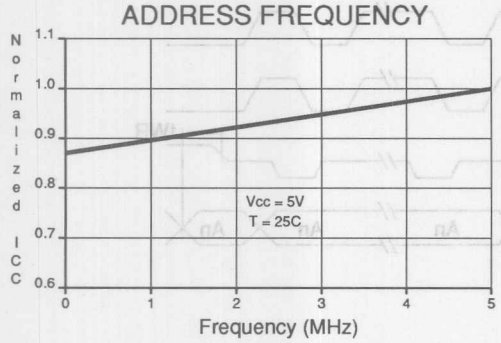
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	80	0.1	AT28PC64(E)-15DC AT28PC64(E)-15JC AT28PC64(E)-15PC AT28PC64(E)-15TC	28D6 32J 28P6 28T	Commercial (0°C to 70°C)
			AT28PC64(E)-15DI AT28PC64(E)-15JI AT28PC64(E)-15PI AT28PC64(E)-15TI	28D6 32J 28P6 28T	Industrial (-40°C to 85°C)
150	80	0.2	AT28PC64(E)-15DM/883 AT28PC64(E)-15LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	80	0.1	AT28PC64(E)-20DC AT28PC64(E)-20JC AT28PC64(E)-20PC	28D6 32J 28P6	Commercial (0°C to 70°C)
			AT28PC64(E)-20DI AT28PC64(E)-20JI AT28PC64(E)-20PI	28D6 32J 28P6	Industrial (-40°C to 85°C)
200	80	0.2	AT28PC64(E)-20DM/883 AT28PC64(E)-20LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	80	0.1	AT28PC64(E)-25DC AT28PC64(E)-25JC AT28PC64(E)-25PC AT28PC64-W	28D6 32J 28P6 DIE	Commercial (0°C to 70°C)
			AT28PC64(E)-25DI AT28PC64(E)-25JI AT28PC64(E)-25PI	28D6 32J 28P6	Industrial (-40°C to 85°C)
250	80	0.2	AT28PC64(E)-25DM/883 AT28PC64(E)-25LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
300[1]	80	0.2	AT28PC64(E)-30DM/883 AT28PC64(E)-30LM/883	28D6 32L	Military/883 Class B, Fully Compliant (-55°C to 125°C)
350[1]	80	0.2	AT28PC64(E)-35DM/883 AT28PC64(E)-35LM/883	28D6 32L	Military/883 Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

tACC (ns)	ICC (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
200	80	0.2	5962-87514 09 XX 5962-87514 09 YX	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	80	0.2	5962-87514 08 XX 5962-87514 08 YX	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
300[1]	80	0.2	5962-87514 07 XX 5962-87514 07 YX	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
350[1]	80	0.2	5962-87514 06 XX 5962-87514 06 YX	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Notes: 1. Electrical specifications for these speeds are defined in Standardized Military Drawing 5962-87514.

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier OTP (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
28T	28 Lead, Plastic Thin Small Outline Package (TSOP)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 2 ms
E	High Endurance Option: Endurance = 100K Write Cycles

256K (32K x 8) Paged CMOS E^2PROM

Features

- **Fast Read Access Time - 150 ns**
- **Automatic Page Write Operation**
  - **Internal Address and Data Latches for 64 Bytes**
  - **Internal Control Timer**
- **Fast Write Cycle Times**
  - **Page Write Cycle Time: 3.0 ms or 10 ms maximum**
  - **1 to 64 Byte Page Write Operation**
- **Low Power Dissipation**
  - **80 mA Active Current**
  - **200 µA CMOS Standby Current**
- **Hardware and Software Data Protection**
- **$\overline{\text{DATA}}$ Polling for End of Write Detection**
- **High Reliability CMOS Technology**
  - **Endurance: 10^4 or 10^5 Cycles**
  - **Data Retention: 10 years**
- **Single 5 V ± 10% Supply**
- **CMOS and TTL Compatible Inputs and Outputs**
- **JEDEC Approved Byte-Wide Pinout**
- **Full Military, Commercial, and Industrial Temperature Ranges**

Description

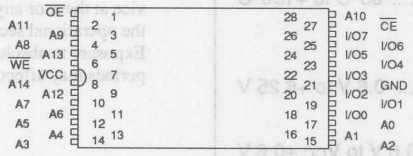
The AT28C256 is a high-performance Electrically Erasable and Programmable Read Only Memory. Its 256K of memory is organized as 32,768 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 150 ns with power dissipation of just 440 mW. When the device is deselected, the CMOS standby current is less than 200 µA.

The AT28C256 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow writing of up to 64

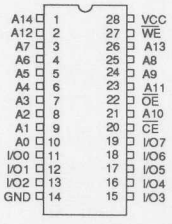
(continued on next page)

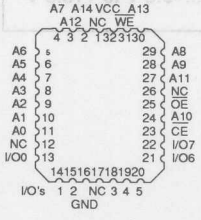
Pin Configurations

TSOP Top View



Pin Name	Function
A0 - A14	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect





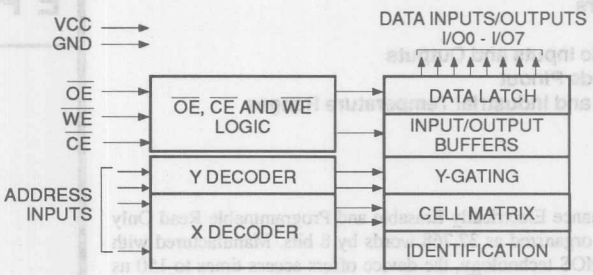
Note: PLCC package pins 1 and 17 are DON'T CONNECT.

Description (Continued)

bytes simultaneously. During a write cycle, the addresses and 1 to 64 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{DATA}$ polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's 28C256 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64 bytes of E^2PROM for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6 V to +6.25 V
All Output Voltages with Respect to Ground	-0.6 V to V_{CC} +0.6 V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6 V to +13.5 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: The AT28C256 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

BYTE WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started it will automatically time itself to completion.

PAGE WRITE: The page write operation of the AT28C256 allows one to sixty-four bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; the first byte written can then be followed by one to sixty-three additional bytes. Each successive byte must be written within 150 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded the AT28C256 will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A6-A14 inputs. For each $\overline{WE}$ high to low transition during the page write operation, A6 - A14 must be the same.

The A0 to A5 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The AT28C256 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{DATA}$ Polling may begin at anytime during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling the AT28C256 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Atmel has incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE PROTECTION: Hardware features protect against inadvertent writes to the AT28C256 in the following ways: (a) V_{CC} sense - if V_{CC} is below 3.8 V (typical) the write function is inhibited; (b) V_{CC} power-on delay - once V_{CC} has reached 3.8 V the device will automatically time out 5 ms (typical) before allowing a write: (c) write inhibit - holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles; (d) noise filter - pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature has been implemented on the AT28C256. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the AT28C256 is shipped from Atmel with SDP disabled.

SDP is enabled by the host system issuing a series of three write commands; three specific bytes of data are written to three specific addresses (refer to Software Data Protection Algorithm). After writing the three byte command sequence and after t_{WC} the entire AT28C256 will be protected against inadvertent write operations. It should be noted, that once protected the host may still perform a byte or page write to the AT28C256. This is done by preceding the data to be written by the same three byte command sequence used to enable SDP.

Once set, SDP will remain active unless the disable command sequence is issued. Power transitions do not disable SDP and SDP will protect the AT28C256 during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not written to the device and the memory addresses used in the sequence may be written with data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the three byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, read operations will effectively be polling operations.

DEVICE IDENTIFICATION: An extra 64 bytes of E^2PROM memory are available to the user for device identification. By raising A9 to 12 V ± 0.5 V and using address locations 7FC0H to 7FFFH the additional bytes may be written to or read from in the same manner as the regular memory array.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Note: 1. This parameter is characterized and is not 100% tested.

D.C. and A.C. Operating Range

		AT28C256-15	AT28C256-20	AT28C256-25	AT28C256-35
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 10%	5 V ± 10%	5 V ± 10%	5 V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H [3]	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.
3. $V_H = 12.0\ V \pm 0.5\ V$.

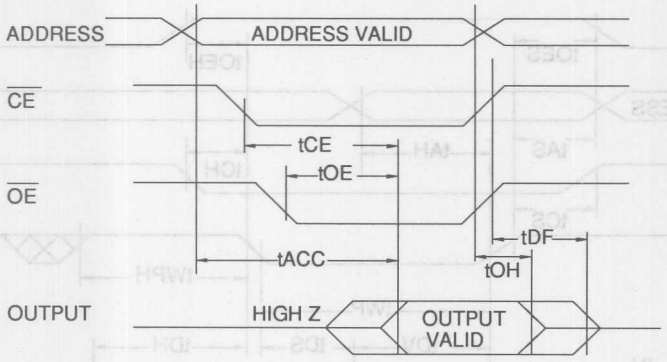
D.C. Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	$V_{IN} = 0\ V$ to $V_{CC} + 1\ V$			10	µA
I_{LO}	Output Leakage Current	$V_{I/O} = 0\ V$ to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE} = V_{CC}-0.3\ V$ to $V_{CC} + 1\ V$	Com., Ind.		200	µA
			Mil.		300	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE} = 2.0\ V$ to $V_{CC} + 1\ V$			3	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; $I_{OUT} = 0$ mA			80	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA			.45	V
V_{OH}	Output High Voltage	$I_{OH} = -400$ µA		2.4		V

A.C. Read Characteristics

Symbol	Parameter	AT28C256-15 Min	AT28C256-15 Max	AT28C256-20 Min	AT28C256-20 Max	AT28C256-25 Min	AT28C256-25 Max	AT28C256-35 Min	AT28C256-35 Max	Units
t_{ACC}	Address to Output Delay		150		200		250		350	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		150		200		250		350	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	70	0	80	0	100	0	100	ns
t_{DF} (3,4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	50	0	55	0	60	0	70	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		ns

A.C. Read Waveforms



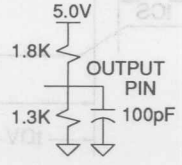
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5ns

Output Test Load

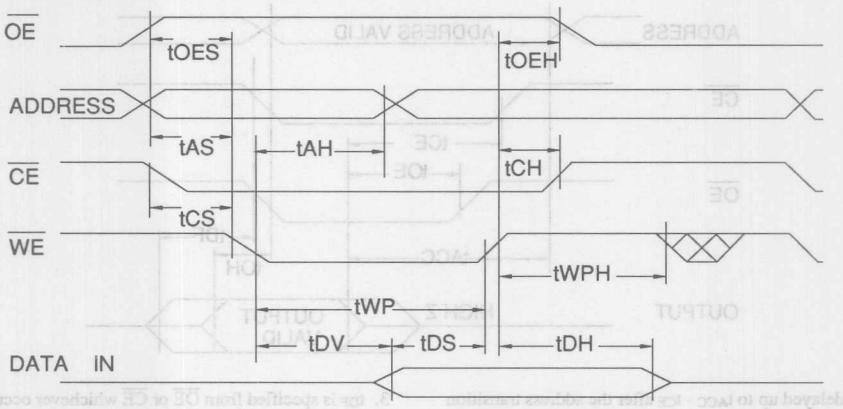


A.C. Write Characteristics

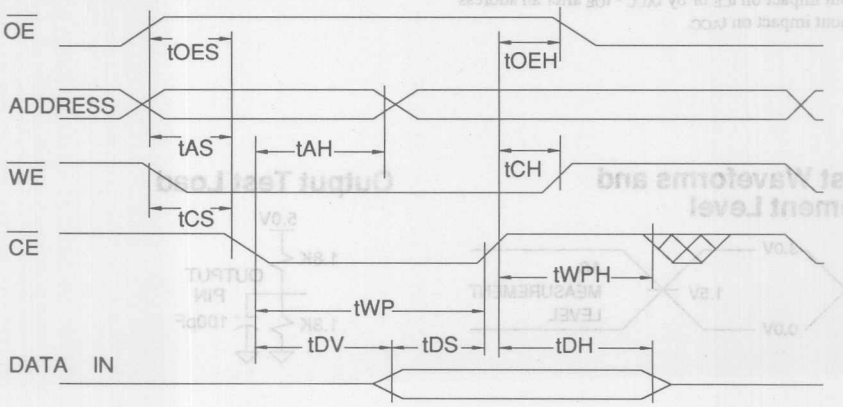
Symbol	Parameter		Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time		0		ns
t_{AH}	Address Hold Time		50		ns
t_{CS}	Chip Select Set-up Time		0		ns
t_{CH}	Chip Select Hold Time		0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)		100		ns
t_{DS}	Data Set-up Time		50		ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time		0		ns
t_{DV}	Time to Data Valid		NR(1)		
t_{WC}	Write Cycle Time	AT28C256		10	ms
		AT28C256F		3.0	ms

Note: 1. NR = No Restiction

A.C. Write Waveforms- $\overline{WE}$ Controlled



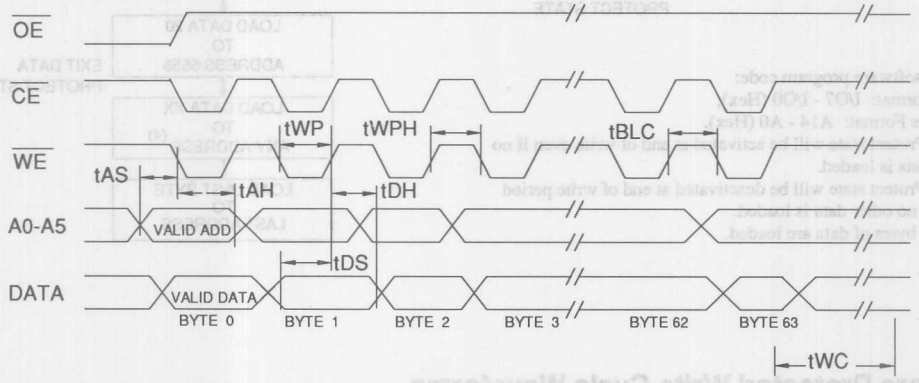
A.C. Write Waveforms- $\overline{CE}$ Controlled



Page Mode Characteristics

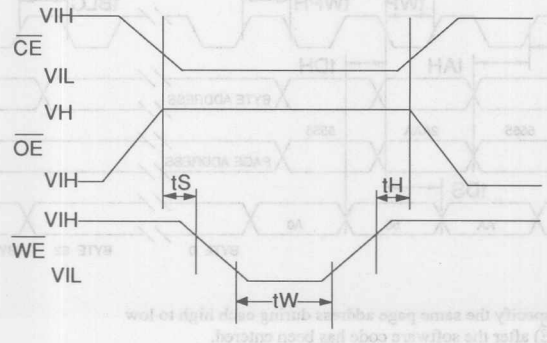
Symbol	Parameter		Min	Max	Units
t_{WC}	Write Cycle Time	AT28C256		10	ms
		AT28C256F		3.0	ms
t_{AS}	Address Set-up Time		0		ns
t_{AH}	Address Hold Time		50		ns
t_{DS}	Data Set-up Time		50		ns
t_{DH}	Data Hold Time		0		ns
t_{WP}	Write Pulse Width		100		ns
t_{BLC}	Byte Load Cycle Time			150	µs
t_{WPH}	Write Pulse Width High		50		ns

Page Mode Write Waveforms



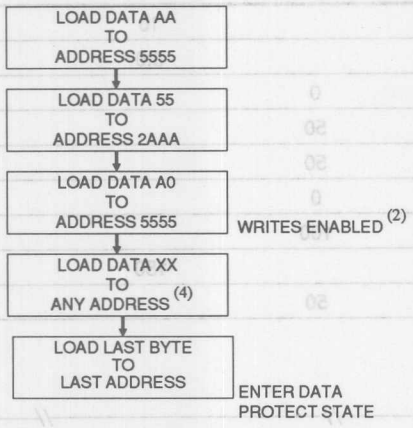
Notes: A6 through A14 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Chip Erase Waveforms

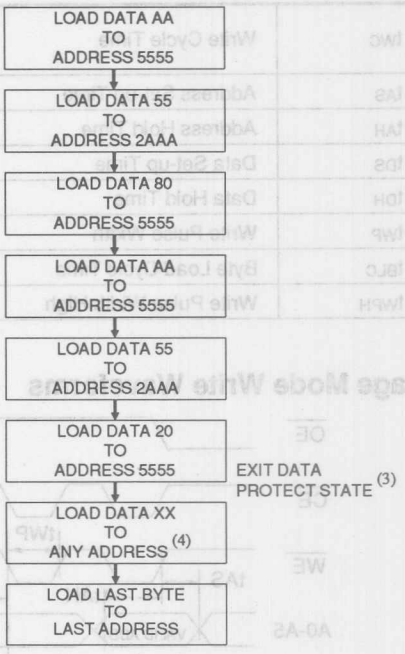


$t_S = t_H = 5$ µsec (min.)
$t_W = 10$ msec (min.)
$V_H = 12.0\ V \pm 0.5\ V$

Software Data Protection Enable Algorithm [1]

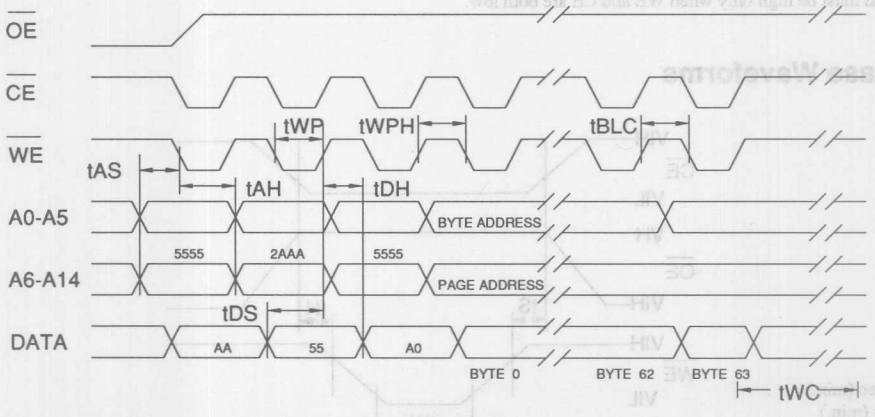


Software Data Protection Disable Algorithm [1]



Notes for software program code:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 64 bytes of data are loaded.

Software Protected Write Cycle Waveforms



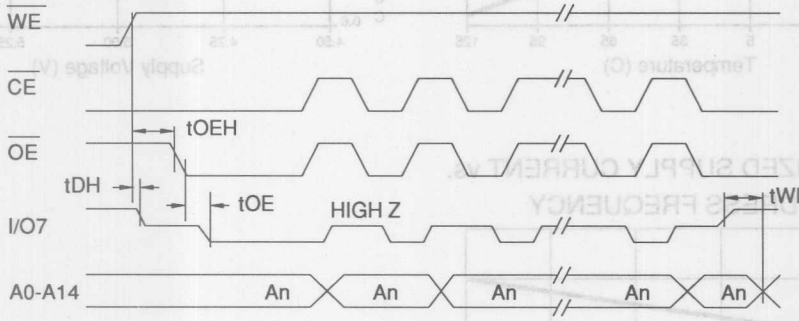
Notes: A6 through A14 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

$\overline{\text{Data}}$ Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	0			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{Data}}$ Polling Waveforms

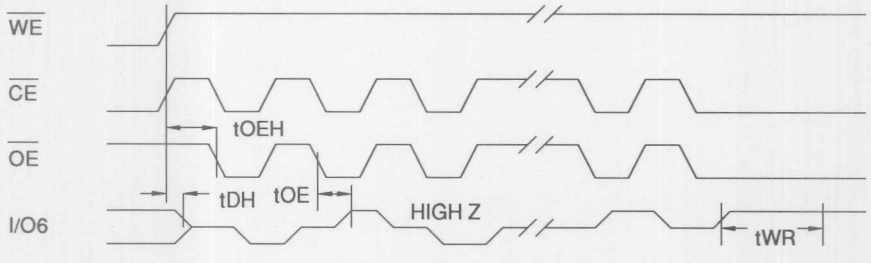


Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

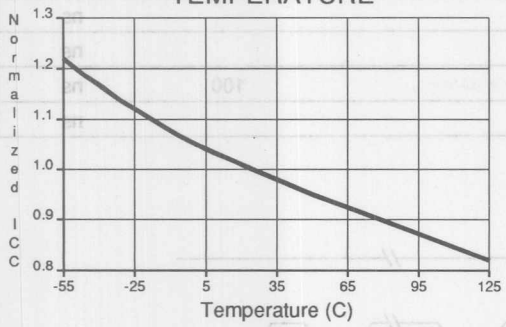
Note: 1. These parameters are characterized and not 100% tested.

Toggle Bit Waveforms

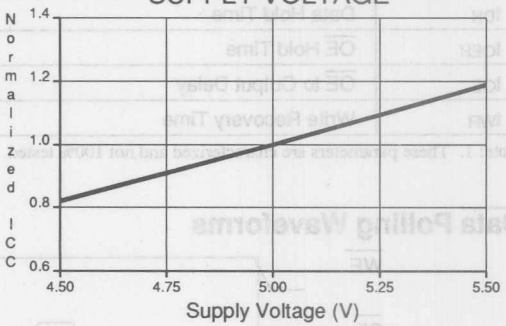


Notes:
1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

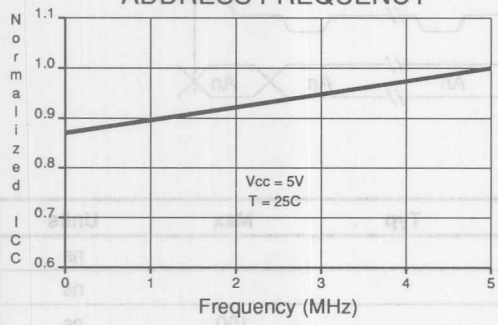
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	80	0.2	AT28C256(E,F)-15DC	28D6	Commercial (0°C to 70°C)
			AT28C256(E,F)-15JC	32J	
			AT28C256(E,F)-15PC	28P6	
			AT28C256(E,F)-15TC	28T	
			AT28C256(E,F)-15UC	28U	
			AT28C256(E,F)-15DI	28D6	Industrial (-40°C to 85°C)
			AT28C256(E,F)-15JI	32J	
			AT28C256(E,F)-15PI	28P6	
			AT28C256(E,F)-15TI	28T	
			AT28C256(E,F)-15UI	28U	
150	80	0.3	AT28C256(E,F)-15DM/883	28D6	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			AT28C256(E,F)-15FM/883	28F	
			AT28C256(E,F)-15LM/883	32L	
			AT28C256(E,F)-15UM/883	28U	
200	80	0.2	AT28C256(E,F)-20DC	28D6	Commercial (0°C to 70°C)
			AT28C256(E,F)-20JC	32J	
			AT28C256(E,F)-20PC	28P6	
			AT28C256(E,F)-20UC	28U	
			AT28C256(E,F)-20DI	28D6	Industrial (-40°C to 85°C)
			AT28C256(E,F)-20JI	32J	
			AT28C256(E,F)-20PI	28P6	
			AT28C256(E,F)-20UI	28U	
200	80	0.3	AT28C256(E,F)-20DM/883	28D6	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			AT28C256(E,F)-20FM/883	28F	
			AT28C256(E,F)-20LM/883	32L	
			AT28C256(E,F)-20UM/883	28U	
250	80	0.2	AT28C256(E,F)-25DC	28D6	Commercial (0°C to 70°C)
			AT28C256(E,F)-25JC	32J	
			AT28C256(E,F)-25PC	28P6	
			AT28C256(E,F)-25UC	28U	
			AT28C256-W	DIE	
			AT28C256(E,F)-25DI	28D6	Industrial (-40°C to 85°C)
			AT28C256(E,F)-25JI	32J	
			AT28C256(E,F)-25PI	28P6	
			AT28C256(E,F)-25UI	28U	
250	80	0.3	AT28C256(E,F)-25DM/883	28D6	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			AT28C256(E,F)-25FM/883	28F	
			AT28C256(E,F)-25LM/883	32L	
			AT28C256(E,F)-25UM/883	28U	
300[1]	80	0.3	AT28C256(E,F)-30DM/883	28D6	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			AT28C256(E,F)-30FM/883	28F	
			AT28C256(E,F)-30LM/883	32L	
			AT28C256(E,F)-30UM/883	28U	
350	80	0.3	AT28C256(E,F)-35DM/883	28D6	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			AT28C256(E,F)-35FM/883	28F	
			AT28C256(E,F)-35LM/883	32L	
			AT28C256(E,F)-35UM/883	28U	

Ordering Information

tACC (ns)	ICC (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	80	0.35	5962-88525 07 UX 5962-88525 07 XX 5962-88525 07 YX 5962-88525 07 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			5962-88525 06 UX 5962-88525 06 XX 5962-88525 06 YX 5962-88525 06 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	80	0.35	5962-88525 04 UX 5962-88525 04 XX 5962-88525 04 YX 5962-88525 04 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	80	0.35	5962-88525 03 UX 5962-88525 03 XX 5962-88525 03 YX 5962-88525 03 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			5962-88525 05 UX 5962-88525 05 XX 5962-88525 05 YX 5962-88525 05 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
300[1]	80	0.35	5962-88525 02 UX 5962-88525 02 XX 5962-88525 02 YX 5962-88525 02 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
350	80	0.35	5962-88525 01 UX 5962-88525 01 XX 5962-88525 01 YX 5962-88525 01 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Notes: 1. Electrical specifications for these speeds are defined by Standardized Military Drawing 5962-88525.

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
28F	28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28T	28 Lead, Plastic Thin Small Outline Package (TSOP)
28U	28 Pin, Ceramic Pin Grid Array (PGA)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms
E	High Endurance Option: Endurance = 100K Write Cycles
F	Fast Write Option: Write Time = 3 ms

256 (32K x 8) High Speed CMOS E^2PROM

Features

- Fast Read Access Time - 70 ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 64 Bytes
  - Internal Control Timer
- Fast Write Cycle Times
  - Page Write Cycle Time: 10 ms or 3 ms maximum
  - 1 to 64 Byte Page Write Operation
- Low Power Dissipation
  - 80 mA Active Current
  - 3 mA Standby Current (AT28HC256L)
- Hardware and Software Data Protection
- $\overline{\text{DATA}}$ Polling for End of Write Detection
- High Reliability CMOS Technology
  - Endurance: 10^4 or 10^5 Cycles
  - Data Retention: 10 years
- Single 5 V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-Wide Pinout
- Full Military, Commercial, and Industrial Temperature Ranges

Description

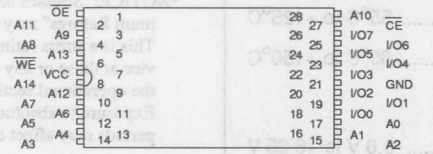
The AT28HC256/L is a high-performance Electrically Erasable and Programmable Read Only Memory. Its 256K of memory is organized as 32,768 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the AT28HC256 offers access times to 70 ns with power dissipation of just 440 mW. When the AT28HC256L is deselected, the standby current is less than 5 mA.

The AT28HC256/L is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow writing of up to

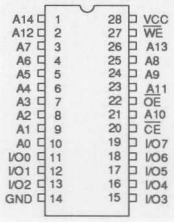
(continued on next page)

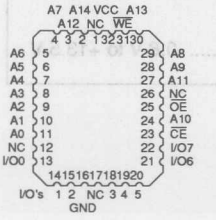
Pin Configurations

TSOP Top View



Pin Name	Function
A0 - A14	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect





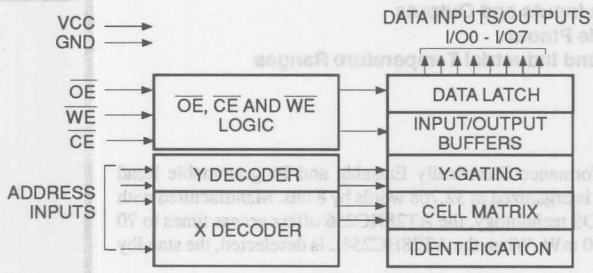
Note: PLCC package pins 1 and 17 are DON'T CONNECT.

Description (Continued)

64 bytes simultaneously. During a write cycle, the address and 1 to 64 bytes of data are internally latched, freeing the addresses and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{\text{DATA}}$ polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's 28HC256/L has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64 bytes of E^2PROM for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6 V to +6.25 V
All Output Voltages with Respect to Ground	-0.6 V to V_{CC} +0.6 V
Voltage on $\overline{\text{OE}}$ and A9 with Respect to Ground	-0.6 V to +13.5 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ: The AT28C256 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

BYTE WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started it will automatically time itself to completion.

PAGE WRITE: The page write operation of the AT28C256 allows one to sixty-four bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; the first byte written can then be followed by one to sixty-three additional bytes. Each successive byte must be written within 150 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded the AT28C256 will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A6-A14 inputs. That is, for each $\overline{WE}$ high to low transition during the page write operation, A6 - A14 must be the same.

The A0 to A5 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The AT28C256 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{DATA}$ Polling may begin at anytime during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling the AT28C256 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Testing the toggle bit may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes to any five-volt-only nonvolatile memory may occur during transition of the host system power supply. Atmel has incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE PROTECTION: Hardware features protect against inadvertent writes to the AT28C256 in the following ways: (a) V_{CC} sense - if V_{CC} is below 3.8 V (typical) the write function is inhibited; (b) V_{CC} power-on delay - once V_{CC} has reached 3.8 V the device will automatically time out 5 ms typical) before allowing a write: (c) write inhibit - holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles; (d) noise filter - pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature has been implemented on the AT28C256. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the AT28C256 is shipped from Atmel with SDP disabled.

SDP is enabled by the host system issuing a series of three write commands; three specific bytes of data are written to three specific addresses (refer to Software Data Protection Algorithm). After writing the three byte command sequence and after t_{WC} the entire AT28C256 will be protected against inadvertent write operations. It should be noted, that once protected the host may still perform a byte or page write to the AT28C64B. This is done by preceding the data to be written by the same three byte command sequence.

Once set, SDP will remain active unless the disable command sequence is issued. Power transitions do not disable SDP and SDP will protect the AT28C256 during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. It should also be noted that the data in the enable and disable command sequences is not written to the device and the memory addresses used in the sequence may be written with data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the three byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, read operations will effectively be polling operations.

DEVICE IDENTIFICATION: An extra 64 bytes of E^2PROM memory are available to the user for device identification. By raising A9 to 12 V ± 0.5 V and using address locations 7FC0H to 7FFFH the additional bytes may be written to or read from in the same manner as the regular memory array.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Note: 1. This parameter is characterized and is not 100% tested.

D.C. and A.C. Operating Range

		AT28HC256-70	AT28HC256L-90	AT28HC256-90	AT28HC256/L-12
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.			-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 10%	5 V ± 10%	5 V ± 10%	5 V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write(2)	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X(1)	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H (3)	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.
3. $V_H = 12.0\ V \pm 0.5\ V$.

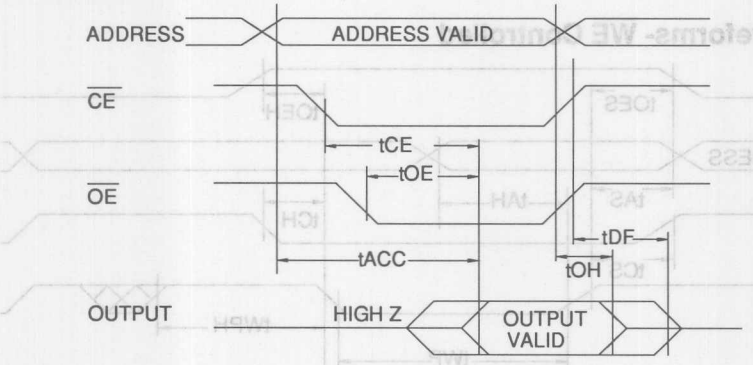
D.C. Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	$V_{IN} = 0\ V$ to $V_{CC} + 1\ V$			10	µA
I_{LO}	Output Leakage Current	$V_{I/O} = 0V$ to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current TTL	$\overline{CE} = 2.0\ V$ to $V_{CC} + 1\ V$	AT28HC256L		3	mA
			AT28HC256		60	mA
I_{SB2}	V_{CC} Standby Current CMOS	$\overline{CE} = -3.0\ V$ to $V_{CC} + 1\ V$	AT28HC256L		300	µA
I_{CC}	V_{CC} Active Current	f = 5 MHz; $I_{OUT} = 0$ mA			80	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	$I_{OL} = 6.0$ mA			.45	V
V_{OH}	Output High Voltage	$I_{OH} = -4$ mA		2.4		V

A.C. Read Characteristics

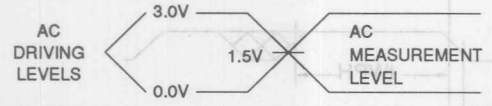
Symbol	Parameter	AT28HC256-70 Min	AT28HC256-70 Max	AT28C256/L-90 Min	AT28C256/L-90 Max	AT28HC256/L-12 Min	AT28HC256/L-12 Max	Units
t_{ACC}	Address to Output Delay		70		90		120	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		70		90		120	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	35	0	40	0	50	ns
t_{DF} (3,4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	35	0	40	0	50	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

A.C. Read Waveforms



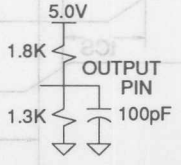
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

Output Test Load

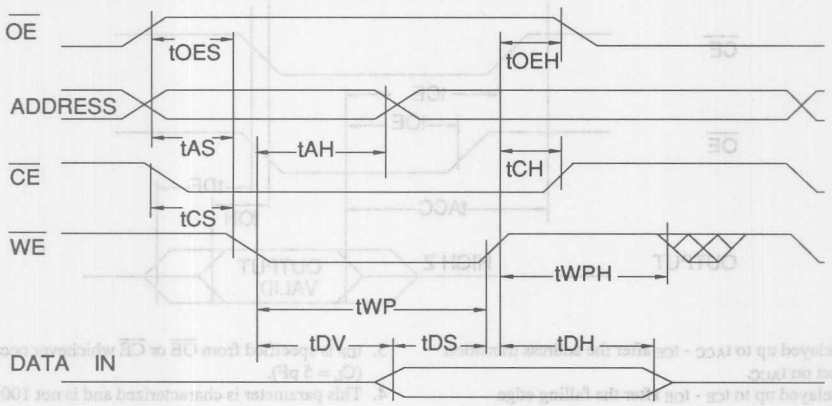


A.C. Write Characteristics

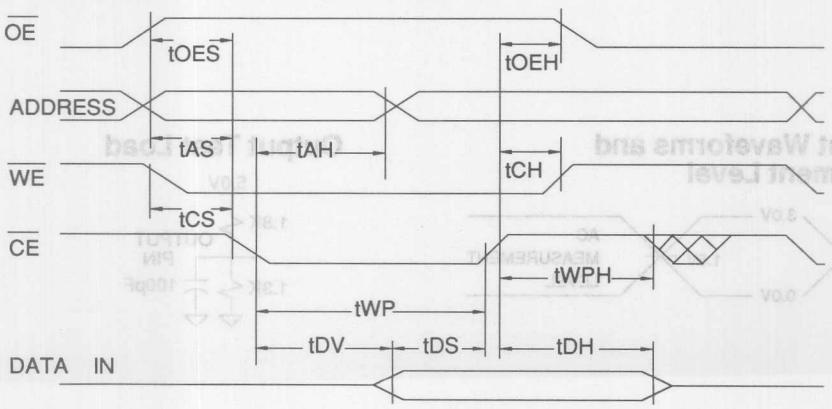
Symbol	Parameter		Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time		0		ns
t_{AH}	Address Hold Time		50		ns
t_{CS}	Chip Select Set-up Time		0		ns
t_{CH}	Chip Select Hold Time		0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)		100		ns
t_{DS}	Data Set-up Time		50		ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time		0		ns
t_{DV}	Time to Data Valid		NR(1)		
t_{WC}	Write Cycle Time	AT28HC256		10	ms
		AT28HC256F		3.0	ms

Note: 1. NR = No Restiction

A.C. Write Waveforms- $\overline{WE}$ Controlled



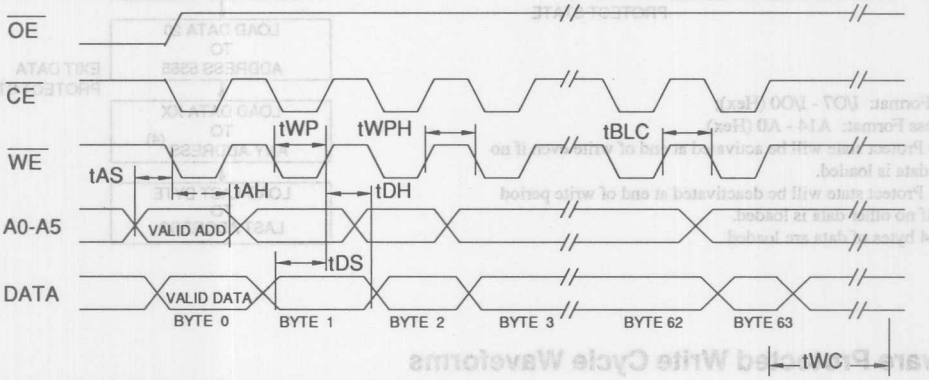
A.C. Write Load Waveforms- $\overline{CE}$ Controlled



Page Mode Write Characteristics

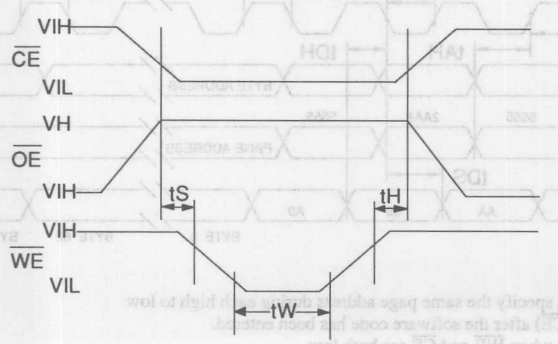
Symbol	Parameter		Min	Typ	Max	Units
t_{WC}	Write Cycle Time	AT28HC256		5	10	ms
		AT28HC256F		2	3.0	ms
t_{AS}	Address Set-up Time		0			ns
t_{AH}	Address Hold Time		50			ns
t_{DS}	Data Set-up Time		50			ns
t_{DH}	Data Hold Time		0			ns
t_{WP}	Write Pulse Width		100			ns
t_{BLC}	Byte Load Cycle Time				150	µs
t_{WPH}	Write Pulse Width High		50			ns

Page Mode Write Waveforms



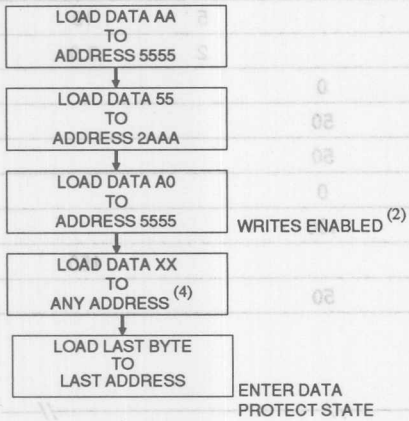
Notes: A6 through A14 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Chip Erase Waveforms

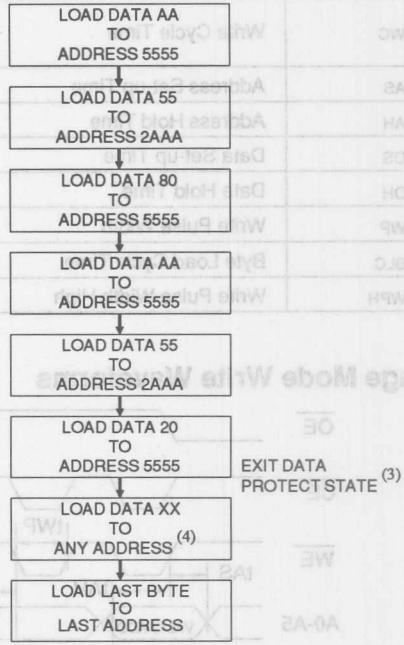


$t_S = t_H = 5$ µsec (min.)
$t_W = 10$ msec (min.)
$V_H = 12.0\ V \pm 0.5\ V$

Software Data Protection Enable Algorithm [1]

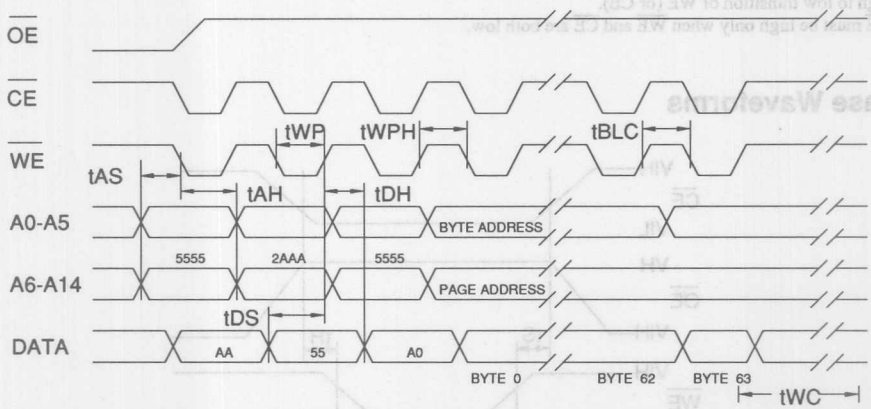


Software Data Protection Disable Algorithm [1]



Notes:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 64 bytes of data are loaded.

Software Protected Write Cycle Waveforms



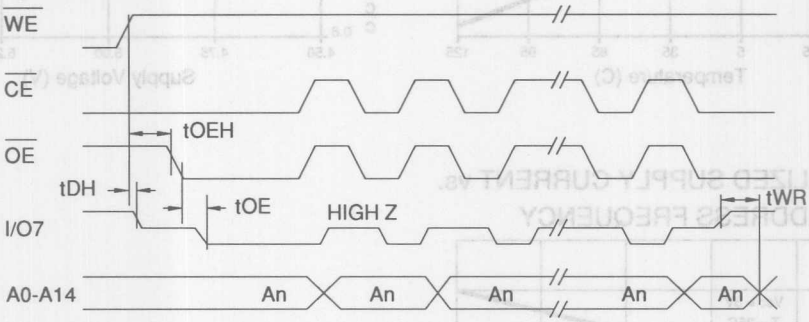
Notes: A6 through A14 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

$\overline{\text{Data}}$ Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	0			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{Data}}$ Polling Waveforms

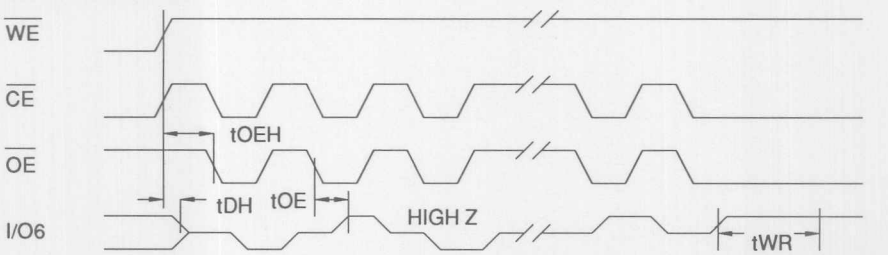


Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

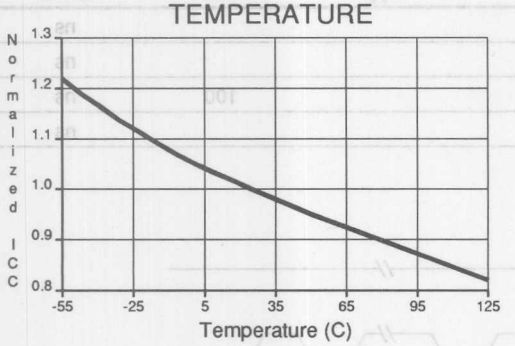
Note: 1. These parameters are characterized and not 100% tested.

Toggle Bit Waveforms

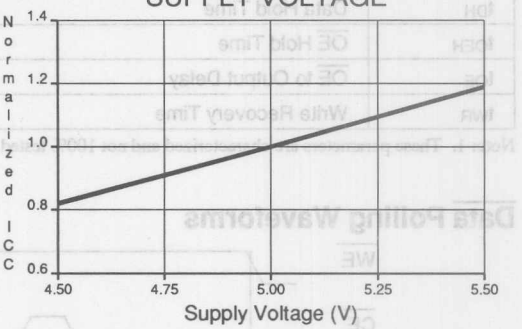


Notes:
1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

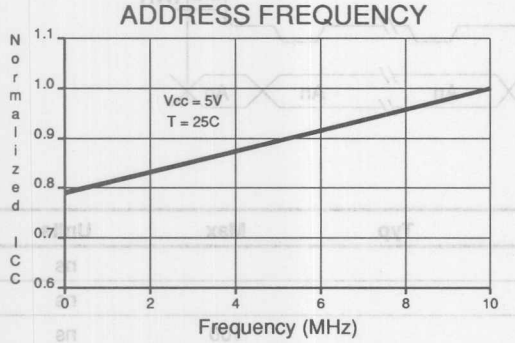
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	80	60	AT28HC256(E,F)-70DC AT28HC256(E,F)-70JC AT28HC256(E,F)-70PC	28D6 32J 28P6	Commercial (0°C to 70°C)
			AT28HC256(E,F)-70DI AT28HC256(E,F)-70JI AT28HC256(E,F)-70PI	28D6 32J 28P6	Industrial (-40°C to 85°C)
90	80	60	AT28HC256(E,F)-90DC AT28HC256(E,F)-90JC AT28HC256(E,F)-90PC AT28HC256(E,F)-90UC	28D6 32J 28P6 28U	Commercial (0°C to 70°C)
			AT28HC256(E,F)-90DI AT28HC256(E,F)-90JI AT28HC256(E,F)-90PI AT28HC256(E,F)-90UI	28D6 32J 28P6 28U	Industrial (-40°C to 85°C)
			AT28HC256(E,F)-90DM/883 AT28HC256(E,F)-90FM/883 AT28HC256(E,F)-90LM/883 AT28HC256(E,F)-90UM/883	28D6 28F 32L 28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	80	60	AT28HC256(E,F)-12DC AT28HC256(E,F)-12JC AT28HC256(E,F)-12PC AT28HC256(E,F)-12TC AT28HC256(E,F)-12UC	28D6 32J 28P6 28T 28U	Commercial (0°C to 70°C)
			AT28HC256(E,F)-12DI AT28HC256(E,F)-12JI AT28HC256(E,F)-12PI AT28HC256(E,F)-12TI AT28HC256(E,F)-12UI	28D6 32J 28P6 28T 28U	Industrial (-40°C to 85°C)
			AT28HC256(E,F)-12DM/883 AT28HC256(E,F)-12FM/883 AT28HC256(E,F)-12LM/883 AT28HC256(E,F)-12UM/883	28D6 28F 32L 28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	80	60	5962-88634 03 UX 5962-88634 03 XX 5962-88634 03 YX 5962-88634 03 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			5962-88634 04 UX 5962-88634 04 XX 5962-88634 04 YX 5962-88634 04 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
28F	28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28T	28 Lead, Plastic Thin Small Outline Package (TSOP)
28U	28 Pin, Ceramic Pin Grid Array (PGA)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms
E	High Endurance Option: Endurance = 100K Write Cycles
F	Fast Write Option: Write Time = 3 ms

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	80	0.3	AT28HC256L(E,F)-90DC AT28HC256L(E,F)-90JC AT28HC256L(E,F)-90PC AT28HC256L(E,F)-90UC	28D6 32J 28P6 28U	Commercial (0°C to 70°C)
			AT28HC256L(E,F)-90DI AT28HC256L(E,F)-90JI AT28HC256L(E,F)-90PI AT28HC256L(E,F)-90UI	28D6 32J 28P6 28U	Industrial (-40°C to 85°C)
120	80	0.3	AT28HC256L(E,F)-12DC AT28HC256L(E,F)-12JC AT28HC256L(E,F)-12PC AT28HC256L(E,F)-12UC AT28HC256L-W	28D6 32J 28P6 28U DIE	Commercial (0°C to 70°C)
			AT28HC256L(E,F)-12DI AT28HC256L(E,F)-12JI AT28HC256L(E,F)-12PI AT28HC256L(E,F)-12UI	28D6 32J 28P6 28U	Industrial (-40°C to 85°C)
			AT28HC256L(E,F)-12DM/883 AT28HC256L(E,F)-12FM/883 AT28HC256L(E,F)-12LM/883 AT28HC256L(E,F)-12UM/883	28D6 28F 32L 28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	80	0.3	5962-88634 01 UX 5962-88634 01 XX 5962-88634 01 YX 5962-88634 01 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			5962-88634 02 UX 5962-88634 02 XX 5962-88634 02 YX 5962-88634 02 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
28F	28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28U	28 Pin, Ceramic Pin Grid Array (PGA)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms
E	High Endurance Option: Endurance = 100K Write Cycles
F	Fast Write Option: Write Time = 3 ms

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	80	0.3	AT28HC256L-(E,F)-90DC AT28HC256L-(E,F)-90JC AT28HC256L-(E,F)-90PC AT28HC256L-(E,F)-90UC	28DB 32J 28P6 28U	Commercial (0°C to 70°C)
			AT28HC256L-(E,F)-90DI AT28HC256L-(E,F)-90JI AT28HC256L-(E,F)-90PI AT28HC256L-(E,F)-90UI	28DB 32J 28P6 28U	Industrial (-40°C to 85°C)
120	80	0.3	AT28HC256L-(E,F)-12DC AT28HC256L-(E,F)-12JC AT28HC256L-(E,F)-12PC AT28HC256L-(E,F)-12UC AT28HC256L-W	28DB 32J 28P6 28U DIE	Commercial (0°C to 70°C)
			AT28HC256L-(E,F)-12DI AT28HC256L-(E,F)-12JI AT28HC256L-(E,F)-12PI AT28HC256L-(E,F)-12UI	28DB 32J 28P6 28U	Industrial (-40°C to 85°C)
			AT28HC256L-(E,F)-12DM/883 AT28HC256L-(E,F)-12FM/883 AT28HC256L-(E,F)-12LM/883 AT28HC256L-(E,F)-12UM/883	28DB 28F 32L 28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	80	0.3	5962-88634 01 UX 5962-88634 01 XX 5962-88634 01 YX 5962-88634 01 ZX	28U 28DB 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			5962-88634 02 UX 5962-88634 02 XX 5962-88634 02 YX 5962-88634 02 ZX	28U 28DB 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
28DB	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
28F	28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28U	28 Pin, Ceramic Pin Grid Array (PGA)
W	Die

Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms
E	High Endurance Option: Endurance = 100K Write Cycles
F	Fast Write Option: Write Time = 3 ms

1 Megabit (64K x 16) Paged CMOS E²PROM

Features

- Fast Read Access Time - 120 ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 64 Words
  - Internal Control Timer
- Fast Write Cycle Times
  - Page Write Cycle Time: 10 ms maximum
  - 1 to 64 Word Page Write Operation
- Low Power Dissipation
  - 100 mA Active Current
  - 400 µA CMOS Standby Current
- Hardware and Software Data Protection
- DATA Polling for End of Write Detection
- High Reliability CMOS Technology
  - Endurance: 10^4 or 10^5 Cycles
  - Data Retention: 10 years
- Single 5 V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Word-Wide Pinout
- Full Military, Commercial, and Industrial Temperature Ranges

Description

The AT28C1024 is a high performance Electrically Erasable and Programmable Read Only Memory. Its 1 megabit of memory is organized as 65,536 words by 16 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times down to 120 ns with power dissipation of just 550 mW. When the device is deselected, the CMOS standby current is less than 400 µA.

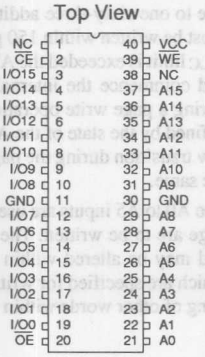
The AT28C1024 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-word page register to allow writing of up to 64 words simultaneously. During a write cycle, the addresses and 1 to 64 words of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{\text{DATA}}$ polling of I/O7 or I/O15. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's 28C1024 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64 words of E²PROM for device identification or tracking.

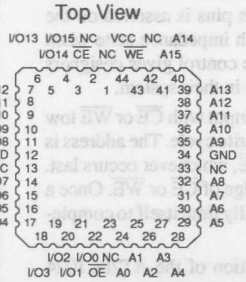
Pin Configurations

Pin Name	Function
A0 - A15	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O15	Data Inputs/Outputs
NC	No Connect

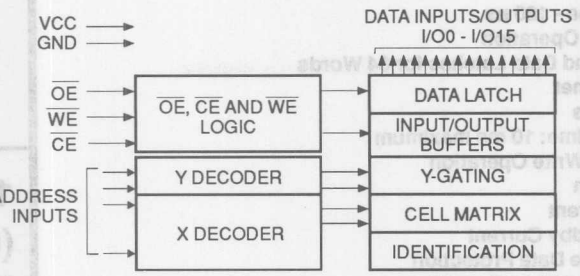
Top View



Top View



Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6 V to +6.25 V
All Output Voltages with Respect to Ground	-0.6 V to V_{CC} +0.6 V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6 V to 13.5 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: The AT28C1024 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a write has been started it will automatically time itself to completion.

PAGE WRITE: The page write operation of the AT28C1024 allows one to one hundred sixty-four wordss of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a single word write; the first eord written can then be followed by one to one sixty-three additional words. Each successive word must be written within 150 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded the AT28C1024 will cease accepting data and commence the internal programming operation. All data during a page write operation must reside on the same page as defined by the state of the A6-A15 inputs. For each $\overline{WE}$ high to low transition during the page write operation, A6-A15 must be the same.

The A0 to A5 inputs are used to specify which words within the page are to be written. The words may be loaded in any order and may be altered within the same load period. Only words which are specified for writing will be written; unnecessary cycling of other words within the page does not occur.

(continued on next page)

Device Operation (Continued)

$\overline{\text{DATA}}$ POLLING: The AT28C1024 features $\overline{\text{DATA}}$ Polling to indicate the end of a write cycle. During a single word or page write cycle an attempted read of the last data written will result in the complement of the written data to be presented on I/O7 and I/O15. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{\text{DATA}}$ Polling may begin at anytime during the write cycle.

TOGGLE BIT: In addition to $\overline{\text{DATA}}$ Polling the AT28C1024 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O14 toggling between one and zero. Once the write has completed, I/O14 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Atmel has incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE PROTECTION: Hardware features protect against inadvertent writes to the AT28C1024 in the following ways: (a) V_{CC} sense - if V_{CC} is below 3.8 V (typical) the write function is inhibited; (b) V_{CC} power-on delay - once V_{CC} has reached 3.8 V the device will automatically time out 5 ms (typical) before allowing a write: (c) write inhibit - holding any one of $\overline{\text{OE}}$ low, $\overline{\text{CE}}$ high or $\overline{\text{WE}}$ high inhibits write cycles; (d) noise filter - pulses of less than 15 ns (typical) on the $\overline{\text{WE}}$ or $\overline{\text{CE}}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature has been implemented on the AT28C1024. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the AT28C1024 is shipped from Atmel with SDP disabled.

SDP is enabled by the host system issuing a series of three write commands; three specific data words are written to three specific addresses (refer to Software Data Protection Algorithm). After writing the three word command sequence and after twc the entire AT28C1024 will be protected against inadvertent write operations. It should be noted, that once protected the host may still perform a single word or page write to the AT28C1024. This is done by preceding the data to be written by the same three word command sequence used to enable SDP.

Once set, SDP will remain active unless the disable command sequence is issued. Power transitions do not disable SDP and SDP will protect the AT28C1024 during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not written to the device and the memory addresses used in the sequence may be written with data in either a single word or page write operation.

After setting SDP, any attempt to write to the device without the three word command sequence will start the internal write timers. No data will be written to the device; however, for the duration of twc, read operations will effectively be polling operations.

DEVICE IDENTIFICATION: An extra 64 words of E^2PROM memory are available to the user for device identification. By raising A9 to 12 V ± 0.5 V and using address locations FFC0H to FFFFH the additional words may be written to or read from in the same manner as the regular memory array.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	10	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Note: 1. This parameter is characterized and is not 100% tested.

D.C. and A.C. Operating Range

		AT28C1024-12	AT28C1024-15	AT28C1024-20	AT28C0124-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 10%	5 V ± 10%	5 V ± 10%	5 V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.

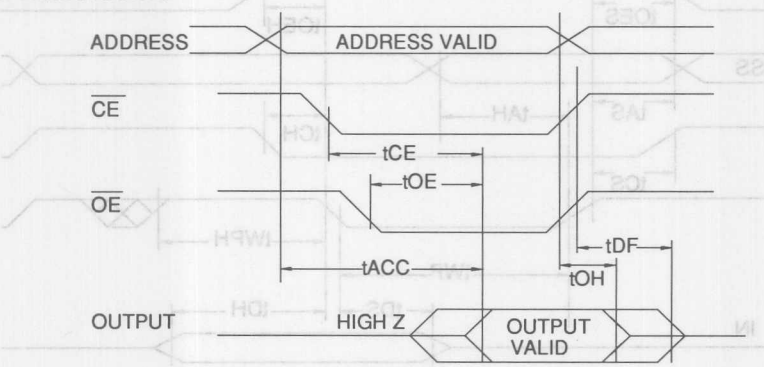
D.C. Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC} + 1 V		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0 V to V_{CC}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC}-0.3 V to V_{CC} + 1 V		400	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0 V to V_{CC} + 1 V		5	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA		100	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		.45	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V

A.C. Read Characteristics

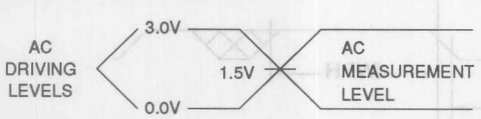
Symbol	Parameter	AT28C1024-12 Min	AT28C1024-12 Max	AT28C1024-15 Min	AT28C1024-15 Max	AT28C1024-20 Min	AT28C1024-20 Max	AT28C1024-25 Min	AT28C1024-25 Max	Units
t_{ACC}	Address to Output Delay		120		150		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		120		150		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	60	0	70	0	80	0	100	ns
t_{DF} (3,4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	55	0	55	0	60	0	70	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		ns

A.C. Read Waveforms



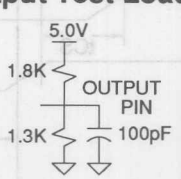
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

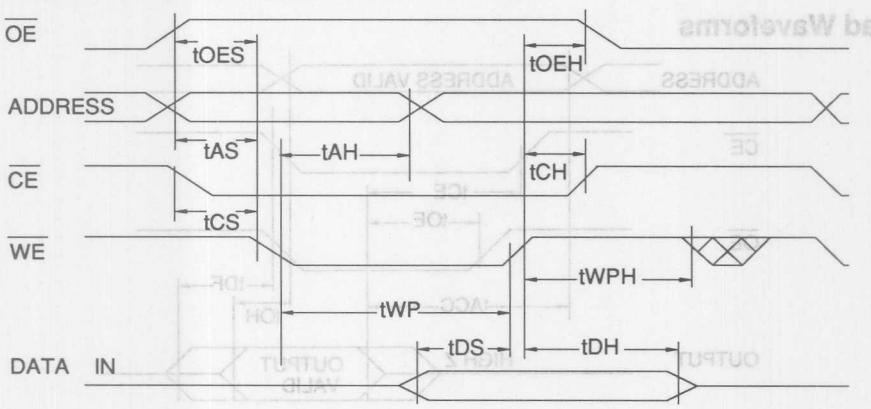
Output Test Load



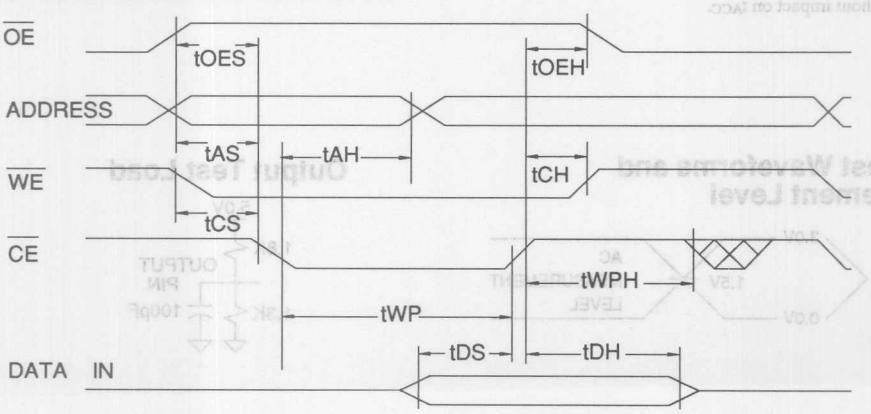
A.C. Write Characteristics

Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{WC}	Write Cycle Time		10	ms

A.C. Write Waveforms- $\overline{WE}$ Controlled



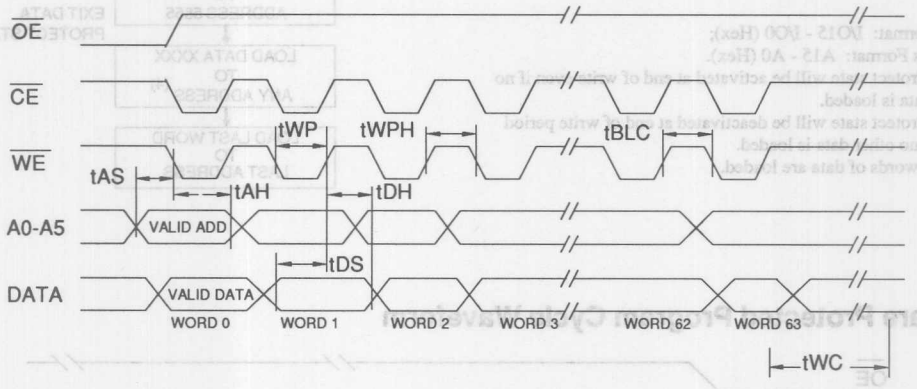
A.C. Write Waveforms- $\overline{CE}$ Controlled



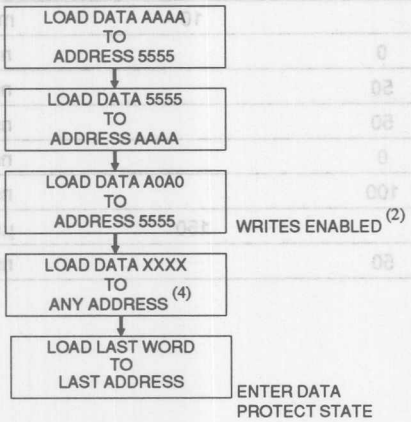
Page Mode Characteristics

Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	100		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	50		ns

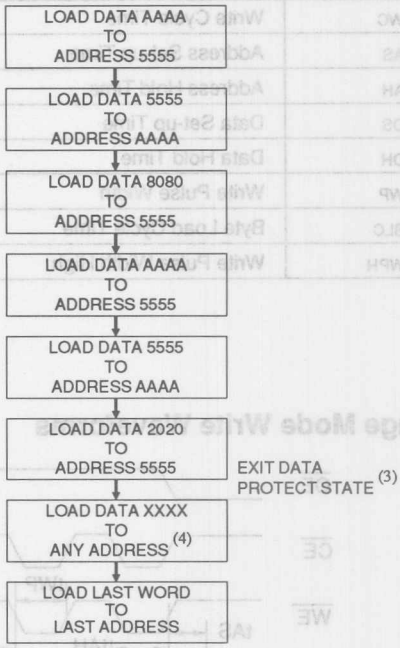
Page Mode Write Waveforms



Software Data Protection Enable Algorithm [1]

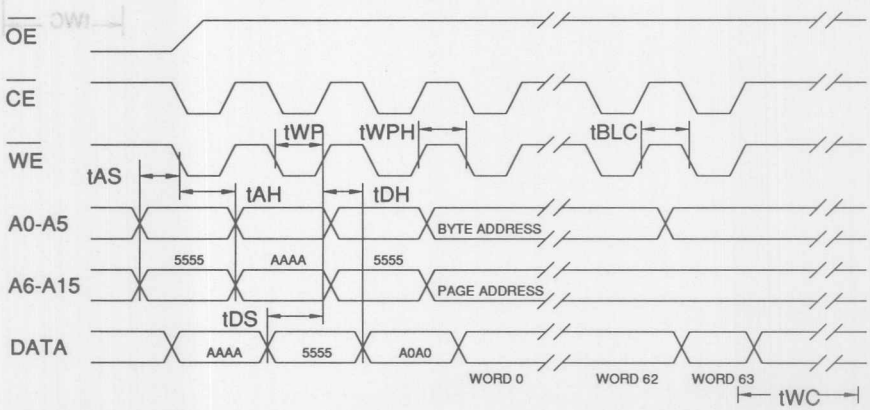


Software Data Protection Disable Algorithm [1]



Notes:
1. Data Format: I/O15 - I/O0 (Hex);
   Address Format: A15 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 64 words of data are loaded.

Software Protected Program Cycle Waveform



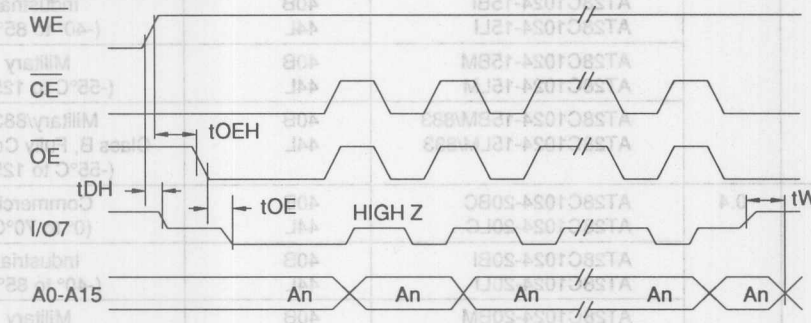
Notes: A6 through A15 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

$\overline{\text{Data}}$ Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	0			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{Data}}$ Polling Waveforms

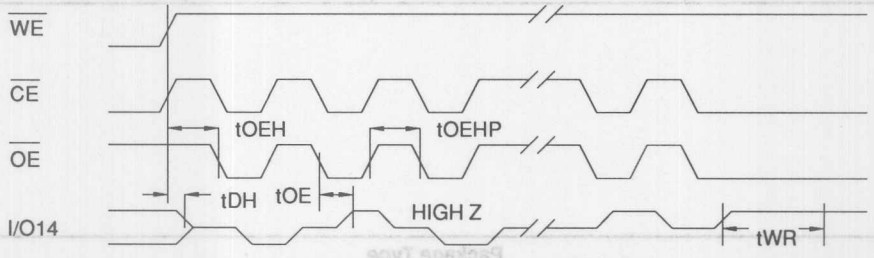


Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

Toggle Bit Waveforms



Notes:
1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O14 will vary.
3. Any address location may be used but the address should not vary.

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	100	0.4	AT28C1024-12BC AT28C1024-12LC	40B 44L	Commercial (0° to 70°C)
			AT28C1024-12BI AT28C1024-12LI	40B 44L	Industrial (-40° to 85°C)
150	100	0.4	AT28C1024-15BC AT28C1024-15LC	40B 44L	Commercial (0° to 70°C)
			AT28C1024-15BI AT28C1024-15LI	40B 44L	Industrial (-40° to 85°C)
			AT28C1024-15BM AT28C1024-15LM	40B 44L	Military (-55°C to 125°C)
			AT28C1024-15BM/883 AT28C1024-15LM/883	40B 44L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	100	0.4	AT28C1024-20BC AT28C1024-20LC	40B 44L	Commercial (0° to 70°C)
			AT28C1024-20BI AT28C1024-20LI	40B 44L	Industrial (-40° to 85°C)
			AT28C1024-20BM AT28C1024-20LM	40B 44L	Military (-55°C to 125°C)
			AT28C1024-20BM/883 AT28C1024-20LM/883	40B 44L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	100	0.4	AT28C1024-25BC AT28C1024-25LC AT28C1024-W	40B 44L DIE	Commercial (0° to 70°C)
			AT28C1024-25BI AT28C1024-25LI	40B 44L	Industrial (-40° to 85°C)
			AT28C1024-25BM AT28C1024-25LM	40B 44L	Military (-55°C to 125°C)
			AT28C1024-25BM/883 AT28C1024-25LM/883	40B 44L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
40B	40 Lead, 0.600" Wide, Ceramic Side Braze Dual Inline (Side Braze)
44L	44 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
W	Die

1 Megabit (128K x 8) Paged CMOS E²PROM

Features

- Fast Read Access Time - 120 ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 128 Bytes
  - Internal Control Timer
- Fast Write Cycle Time
  - Page Write Cycle Time - 10 ms maximum
  - 1 to 128 Byte Page Write Operation
- Low Power Dissipation
  - 80 mA Active Current
  - 300 µA CMOS Standby Current
- Hardware and Software Data Protection
- DATA Polling for End of Write Detection
- High Reliability CMOS Technology
  - Endurance: 10^4 or 10^5 Cycles
  - Data Retention: 10 years
- Single 5 V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-Wide Pinout
- Full Military, Commercial and Industrial Temperature Ranges

Description

The AT28C010 is a high-performance Electrically Erasable and Programmable Read Only Memory. Its one megabit of memory is organized as 131,072 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 120 ns with power dissipation of just 440 mW. When the device is deselected, the CMOS standby current is less than 300 µA.

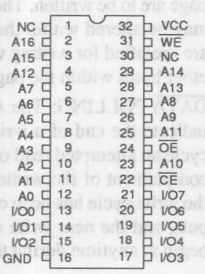
The AT28C010 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 128-byte page register to allow writing of up to 128 bytes simultaneously. During a write cycle, the address and 1 to 128 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{\text{DATA}}$ polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's 28C010 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 128 bytes of E²PROM for device identification or tracking.

Pin Configurations

Pin Name	Function
A0 - A16	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

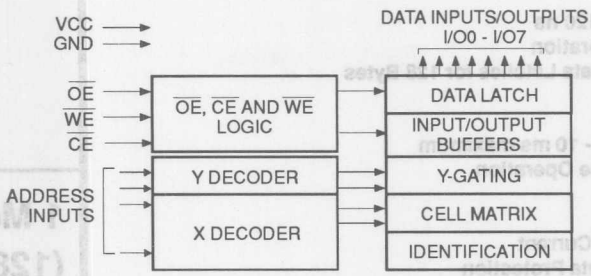
Top View



Top View



Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6 V to +6.25 V
All Output Voltages with Respect to Ground	-0.6 V to V_{CC} +0.6 V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6 V to +13.5 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: The AT28C010 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

BYTE WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started it will automatically time itself to completion.

PAGE WRITE: The page write operation of the AT28C010 allows one to one hundred twenty-eight bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; the first byte written can then be followed by one to one hundred twenty-seven additional bytes. Each successive byte must be written within 150 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded the AT28C010 will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A7-A16 inputs. For each $\overline{WE}$ high to low transition during the page write operation, A7 - A16 must be the same.

The A0 to A6 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The AT28C010 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{DATA}$ Polling may begin at anytime during the write cycle.

(continued on next page)

Device Operation (Continued)

TOGGLE BIT: In addition to $\overline{\text{DATA}}$ Polling the AT28C010 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Atmel has incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE PROTECTION: Hardware features protect against inadvertent writes to the AT28C010 in the following ways: (a) V_{CC} sense - if V_{CC} is below 3.8 V (typical) the write function is inhibited; (b) V_{CC} power-on delay - once V_{CC} has reached 3.8 V the device will automatically time out 5 ms (typical) before allowing a write: (c) write inhibit - holding any one of $\overline{\text{OE}}$ low, $\overline{\text{CE}}$ high or $\overline{\text{WE}}$ high inhibits write cycles; (d) noise filter - pulses of less than 15 ns (typical) on the $\overline{\text{WE}}$ or $\overline{\text{CE}}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature has been implemented on the AT28C010. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the AT28C010 is shipped from Atmel with SDP disabled.

SDP is enabled by the host system issuing a series of three write commands; three specific bytes of data are written to three specific addresses (refer to Software Data Protection Algorithm). After writing the three byte command sequence and after twc the entire AT28C010 will be protected against inadvertent write operations. It should be noted, that once protected the host may still perform a byte or page write to the AT28C010. This is done by preceding the data to be written by the same three byte command sequence used to enable SDP.

Once set, SDP will remain active unless the disable command sequence is issued. Power transitions do not disable SDP and SDP will protect the AT28C010 during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not written to the device and the memory addresses used in the sequence may be written with data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the three byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of twc, read operations will effectively be polling operations.

DEVICE IDENTIFICATION: An extra 128 bytes of E^2PROM memory are available to the user for device identification. By raising A9 to 12 V ± 0.5 V and using address locations 1FF80H to 1FFFFH the bytes may be written to or read from in the same manner as the regular memory array.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	10	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Note: 1. This parameter is characterized and is not 100% tested.

D.C. and A.C. Operating Range

		AT28C010-12	AT28C010-15	AT28C010-20	AT28C010-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 10%	5 V ± 10%	5 V ± 10%	5 V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.

D.C. Characteristics

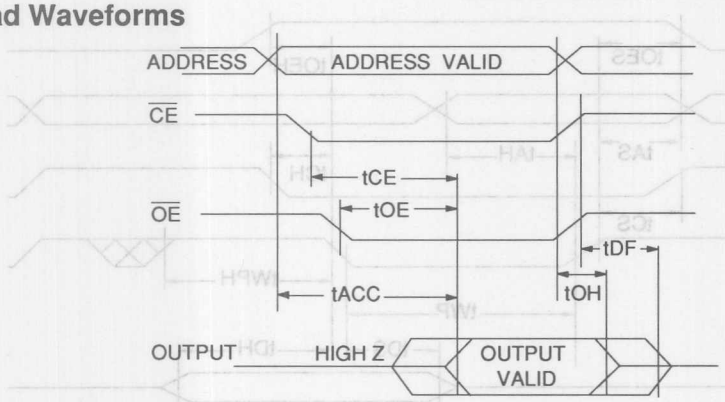
Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC} + 1 V		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0 V to V_{CC}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC}-0.3 V to V_{CC} + 1 V		300	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0 V to V_{CC} + 1 V		3	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA		80	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA	2.4		V
V_{OH2}	Output High Voltage CMOS	I_{OH} =- 100 µA; V_{CC} = 4.5 V	4.2		V

A.C. Read Characteristics

Symbol	Parameter	AT28C010-12 Min	AT28C010-12 Max	AT28C010-15 Min	AT28C010-15 Max	AT28C010-20 Min	AT28C010-20 Max	AT28C010-25 Min	AT28C010-25 Max	Units
t_{ACC}	Address to Output Delay		120		150		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		120		150		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	50	0	55	0	55	0	55	ns
t_{DF} (3,4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	50	0	55	0	55	0	55	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		ns

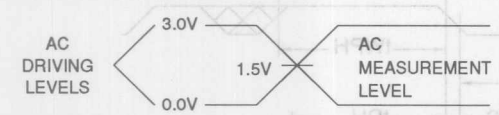
2

A.C. Read Waveforms



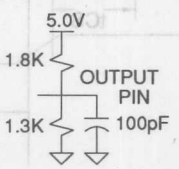
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

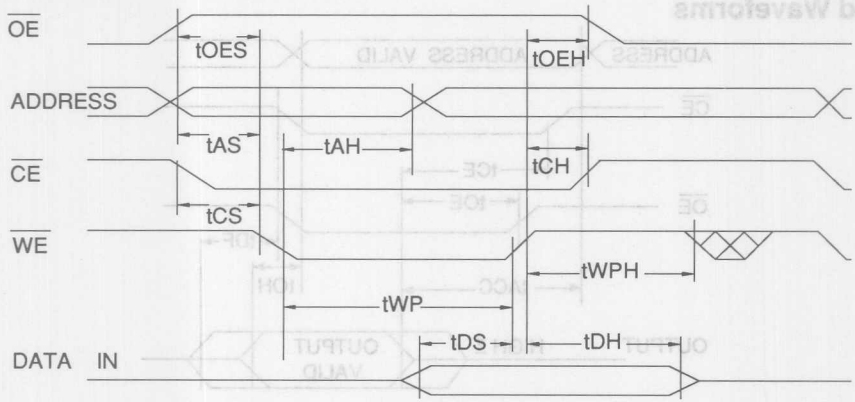
Output Test Load



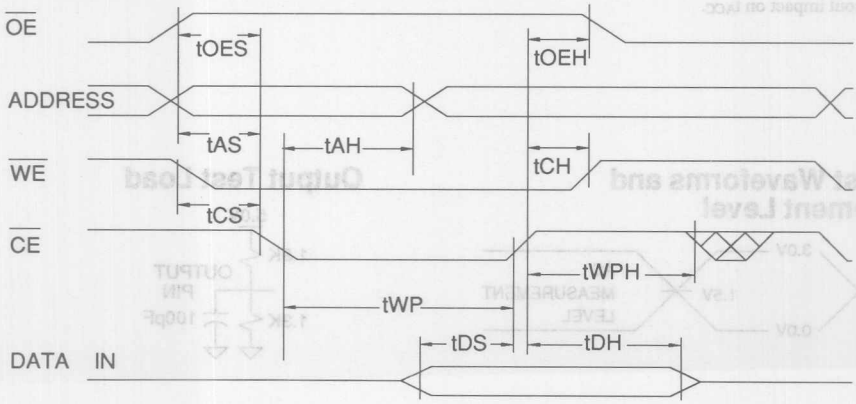
A.C. Write Characteristics

Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{WC}	Write Cycle Time		10	ms

A.C. Write Waveforms- $\overline{WE}$ Controlled



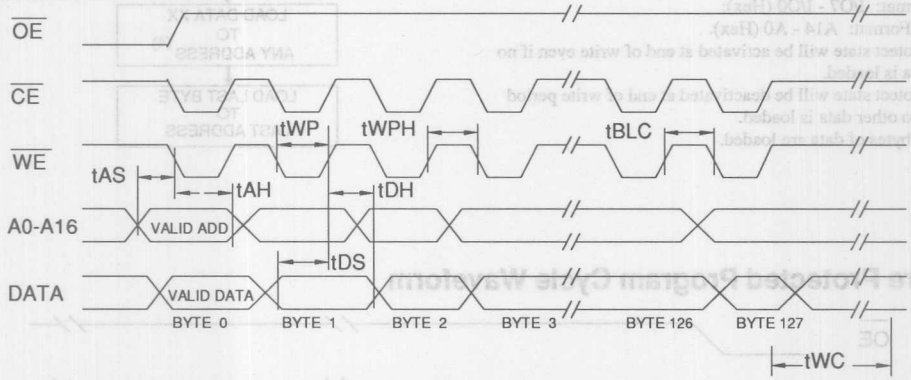
A.C. Write Waveforms- $\overline{CE}$ Controlled



Page Mode Characteristics

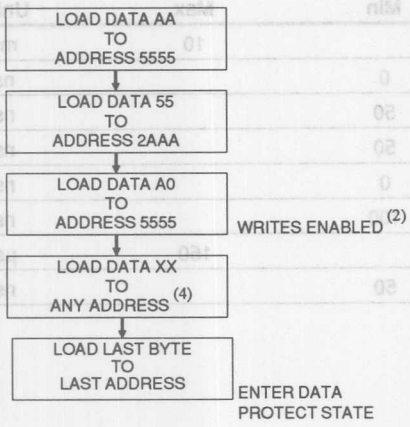
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	100		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	50		ns

Page Mode Write Waveforms

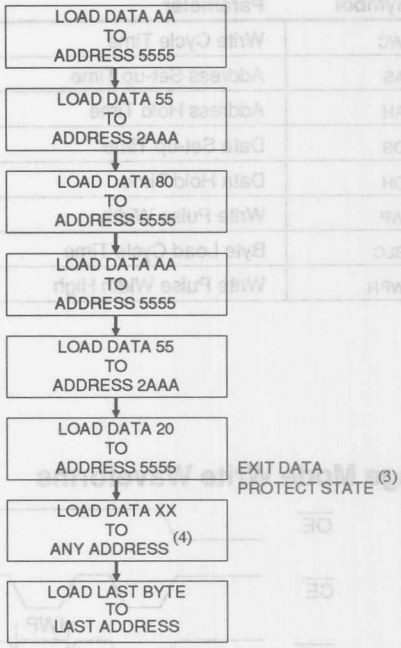


Notes: A7 through A16 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Software Data Protection Enable Algorithm [1]

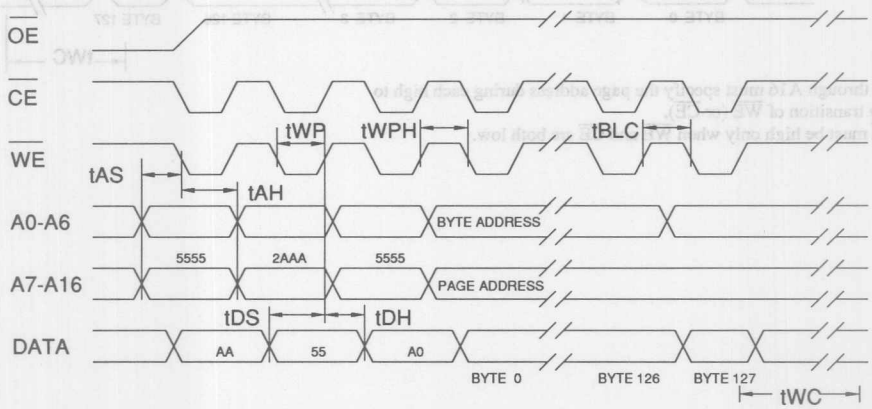


Software Data Protection Disable Algorithm [1]



Notes:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 128 bytes of data are loaded.

Software Protected Program Cycle Waveform



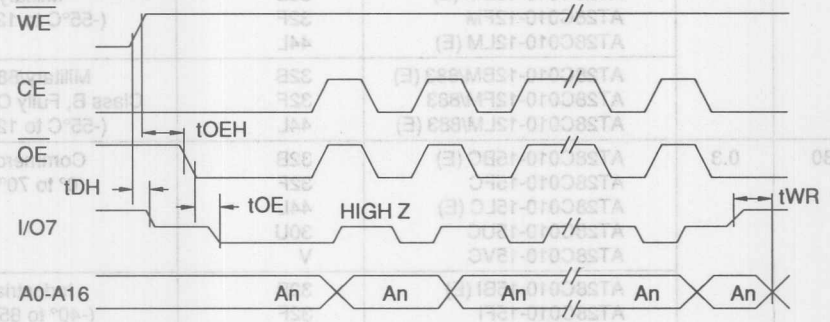
Notes: A0-A14 must conform to the addressing sequence for the first three bytes as shown above. After the command sequence has been issued and a page write operation follows, the page address inputs (A7-A16) must be the same for each high to low transition of $\overline{WE}$ (or $\overline{CE}$). $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

$\overline{\text{Data}}$ Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{Data}}$ Polling Waveforms

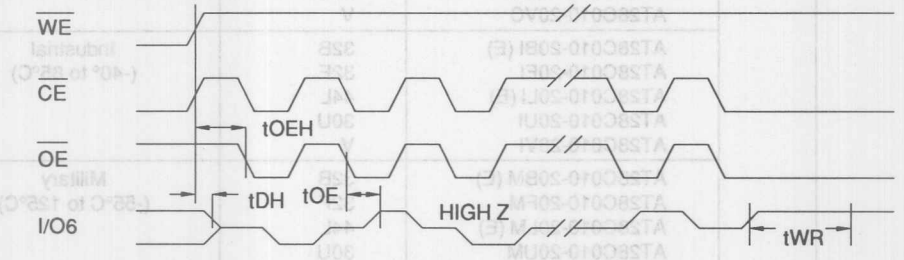


Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

Toggle Bit Waveforms



Notes:
1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	80	0.3	AT28C010-12BC (E) AT28C010-12FC AT28C010-12LC (E)	32B 32F 44L	Commercial (0° to 70°C)
			AT28C010-12BI (E) AT28C010-12FI AT28C010-12LI (E)	32B 32F 44L	Industrial (-40° to 85°C)
			AT28C010-12BM (E) AT28C010-12FM AT28C010-12LM (E)	32B 32F 44L	Military (-55°C to 125°C)
			AT28C010-12BM/883 (E) AT28C010-12FM/883 AT28C010-12LM/883 (E)	32B 32F 44L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	80	0.3	AT28C010-15BC (E) AT28C010-15FC AT28C010-15LC (E) AT28C010-15UC AT28C010-15VC	32B 32F 44L 30U V	Commercial (0° to 70°C)
			AT28C010-15BI (E) AT28C010-15FI AT28C010-15LI (E) AT28C010-15UI AT28C010-15VI	32B 32F 44L 30U V	Industrial (-40° to 85°C)
			AT28C010-15BM (E) AT28C010-15FM AT28C010-15LM (E) AT28C010-15UM AT28C010-15VM	32B 32F 44L 30U V	Military (-55°C to 125°C)
			AT28C010-15BM/883 (E) AT28C010-15FM/883 AT28C010-15LM/883 (E) AT28C010-15UM/883	32B 32F 44L 30U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	80	0.3	AT28C010-20BC (E) AT28C010-20FC AT28C010-20LC (E) AT28C010-20UC AT28C010-20VC	32B 32F 44L 30U V	Commercial (0° to 70°C)
			AT28C010-20BI (E) AT28C010-20FI AT28C010-20LI (E) AT28C010-20UI AT28C010-20VI	32B 32F 44L 30U V	Industrial (-40° to 85°C)
			AT28C010-20BM (E) AT28C010-20FM AT28C010-20LM (E) AT28C010-20UM AT28C010-20VM	32B 32F 44L 30U V	Military (-55°C to 125°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
200	80	0.3	AT28C010-20BM/883 (E) AT28C010-20FM/883 AT28C010-20LM/883 (E) AT28C010-20UM/883	32B 32F 44L 30U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	80	0.3	AT28C010-25BC (E) AT28C010-25FC AT28C010-25LC (E) AT28C010-25UC AT28C010-25VC AT28C010-W	32B 32F 44L 30U V DIE	Commercial (0° to 70°C)
			AT28C010-25BI (E) AT28C010-25FI AT28C010-25LI (E) AT28C010-25UI AT28C010-25VI	32B 32F 44L 30U V	Industrial (-40° to 85°C)
			AT28C010-25BM (E) AT28C010-25FM AT28C010-25LM (E) AT28C010-25UM AT28C010-25VM	32B 32F 44L 30U V	Military (-55°C to 125°C)
			AT28C010-25BM/883 (E) AT28C010-25FM/883 AT28C010-25LM/883 (E) AT28C010-25UM/883	32B 32F 44L 30U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	80	0.3	5962-38267 07M XX 5962-38267 07M YX 5962-38267 07M ZX	32B 44L 32F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	80	0.3	5962-38267 05M XX 5962-38267 05M YX 5962-38267 05M ZX	32B 44L 32F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	80	0.3	5962-38267 03M XX 5962-38267 03M YX 5962-38267 03M ZX	32B 44L 32F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	80	0.3	5962-38267 01M XX 5962-38267 01M YX 5962-38267 01M ZX	32B 44L 32F	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

Package Type	
32B	32 Lead, 0.600" Wide, Ceramic Side Braze Dual Inline (Side Braze)
32F	32 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
44L	44 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
30U	30 Pin, Ceramic Pin Grid Array (PGA)
V	Tape Automated Bond (TAB) Carrier
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms
E	High Endurance Option: Endurance = 100K Write Cycles

2 Megabit (256K x 8) Paged CMOS E²PROM Module

Preliminary

Features

- Fast Read Access Time - 150 ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 128 Bytes
  - Internal Control Timer
- Fast Write Cycle Time
  - Page Write Cycle Time - 10 ms maximum
  - 1 to 128 Byte Page Write Operation
- Low Power Dissipation
  - 80 mA Active Current
  - 5 mA CMOS Standby Current
- Hardware and Software Data Protection
- DATA Polling for End of Write Detection
- High Reliability CMOS Technology
  - Endurance: 10^4 Cycles
  - Data Retention: 10 years
- Single 5 V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-Wide Pinout
- Full Military, Commercial and Industrial Temperature Ranges

Description

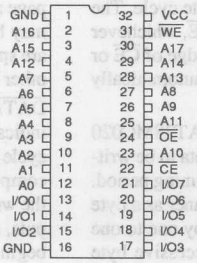
The AT28MC020 is a high-performance Electrically Erasable and Programmable Read Only Memory. Its two megabits of memory is organized as 262,144 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 150 ns with power dissipation of just 440 mW. When the device is deselected, the CMOS standby current is less than 53 mA.

The AT28MC020 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 128-byte page register to allow writing of up to 128 bytes simultaneously. During a write cycle, the address and 1 to 128 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{\text{DATA}}$ polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's 28MC020 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes.

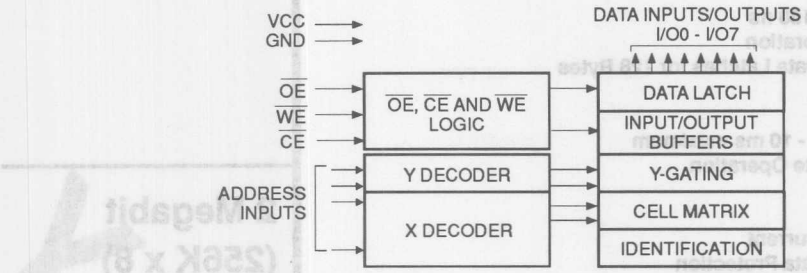
Pin Configurations

Pin Name	Function
A0 - A17	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs



PRELIMINARY

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6 V to +6.25 V
All Output Voltages with Respect to Ground	-0.6 V to V_{CC} +0.6 V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6 V to +13.5 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: The AT28MC020 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

BYTE WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started it will automatically time itself to completion.

PAGE WRITE: The page write operation of the AT28MC020 allows one to one hundred twenty-eight bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; the first byte written can then be followed by one to one hundred twenty-seven additional bytes. Each successive byte must be written within 150 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded the AT28MC020 will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A7-A17 inputs. For each $\overline{WE}$ high to low transition during the page write operation, A7 - A17 must be the same.

The A0 to A6 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The AT28MC020 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{DATA}$ Polling may begin at anytime during the write cycle.

(continued on next page)

Device Operation (Continued)

TOGGLE BIT: In addition to $\overline{\text{DATA}}$ Polling the AT28MC020 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Atmel has incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE PROTECTION: Hardware features protect against inadvertent writes to the AT28MC020 in the following ways: (a) V_{CC} sense - if V_{CC} is below 3.8 V (typical) the write function is inhibited; (b) V_{CC} power-on delay - once V_{CC} has reached 3.8 V the device will automatically time out 5 ms (typical) before allowing a write: (c) write inhibit - holding any one of $\overline{\text{OE}}$ low, $\overline{\text{CE}}$ high or $\overline{\text{WE}}$ high inhibits write cycles; (d) noise filter - pulses of less than 15 ns (typical) on the $\overline{\text{WE}}$ or $\overline{\text{CE}}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature has been implemented on the AT28MC020. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the AT28MC020 is shipped from Atmel with SDP disabled.

SDP is enabled by the host system issuing a series of three write commands; three specific bytes of data are written to three specific addresses (refer to Software Data Protection Algorithm). After writing the three byte command sequence and after t_{WC} the selected quadrant pointed to by A17 will be protected against inadvertent write operations. Because the AT28MC020 is comprised of two discrete memory devices the user must perform the three byte command sequence twice: once to the lower half with A17 = 0; and once to the upper half with A17 = 1.

It should be noted, that once protected the host may still perform a byte or page write to the AT28MC020. This is done by preceding the data to be written by the same three byte command sequence used to protect the device.

Once set, SDP will remain active unless the disable command sequence is issued. Power transitions do not disable SDP and SDP will protect the AT28MC020 during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not written to the device and the memory addresses used in the sequence may be written with data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the three byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, read operations will effectively be polling operations.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	20	40	pF	V_{IN} = 0 V
C_{OUT}	20	40	pF	V_{OUT} = 0 V

Note: 1. This parameter is characterized and is not 100% tested.

D.C. and A.C. Operating Range

		AT28MC020-15	AT28MC020-20	AT28MC020-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 10%	5 V ± 10%	5 V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.

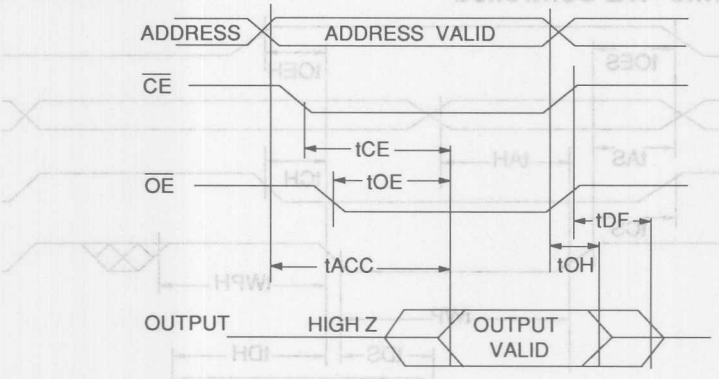
D.C. Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC} + 1 V		20	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0 V to V_{CC}		20	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC}-0.3 V to V_{CC} + 1 V		5	mA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0 V to V_{CC} + 1 V		8	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA		80	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		.45	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V

A.C. Read Characteristics

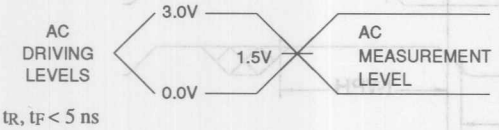
Symbol	Parameter	AT28MC020-15 Min	AT28MC020-15 Max	AT28MC020-20 Min	AT28MC020-20 Max	AT28MC020-25 Min	AT28MC020-25 Max	Units
t_{ACC}	Address to Output Delay		150		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		150		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	70	0	80	0	100	ns
t_{DF} (3,4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	55	0	60	0	70	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

A.C. Read Waveforms



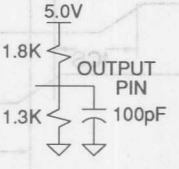
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

Output Test Load

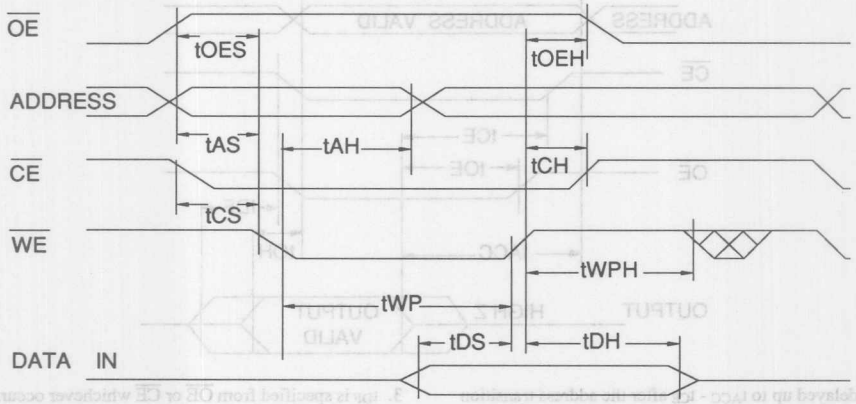


A.C. Write Characteristics

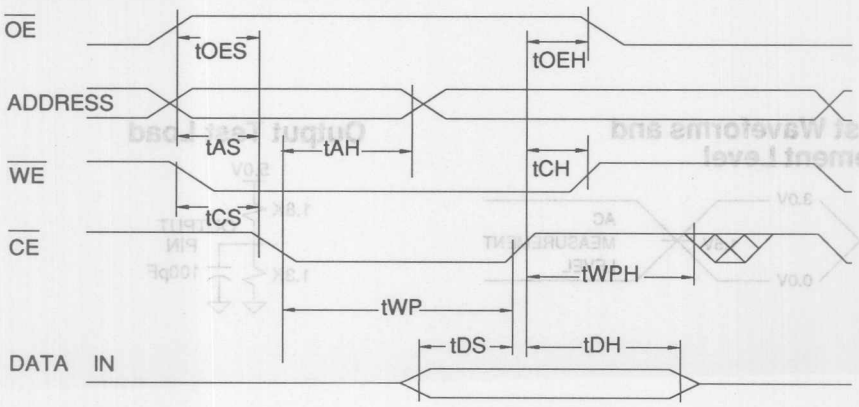
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	10		ns
t_{AH} (1)	Address Hold Time	100		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	150		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	10		ns
t_{WC}	Write Cycle Time		10	ms

Notes: 1. A17 must remain valid throughout the $\overline{WE}$ or $\overline{CE}$ low pulse.

A.C. Write Waveforms- $\overline{WE}$ Controlled



A.C. Write Waveforms- $\overline{CE}$ Controlled

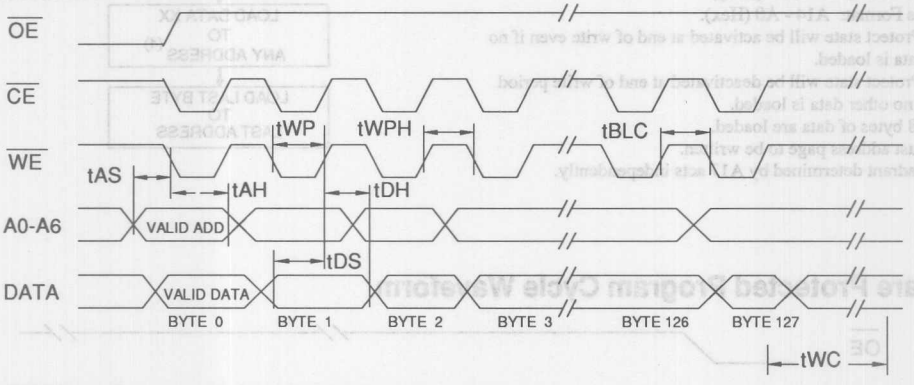


Page Mode Characteristics

Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	10		ns
t_{AH} (1)	Address Hold Time	100		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}	Data Hold Time	10		ns
t_{WP}	Write Pulse Width	150		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	50		ns

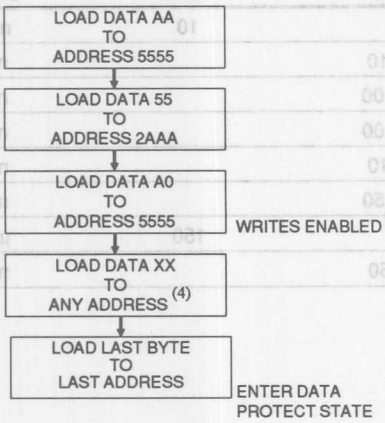
Notes: 1. A17 must remain valid throughout the $\overline{WE}$ or $\overline{CE}$ low pulse.

Page Mode Write Waveforms

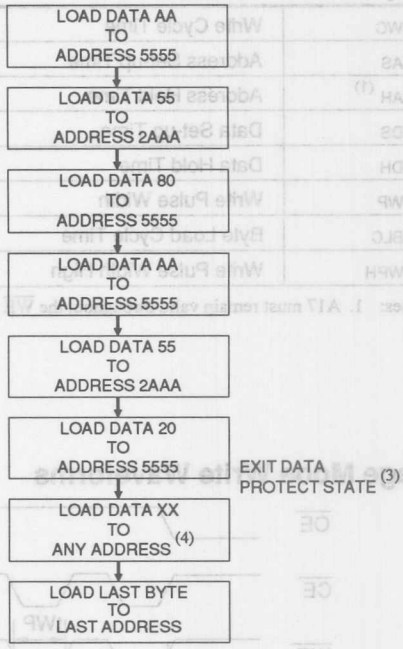


Notes: A7 through A17 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Software Data Protection Enable Algorithm (1,5,6)

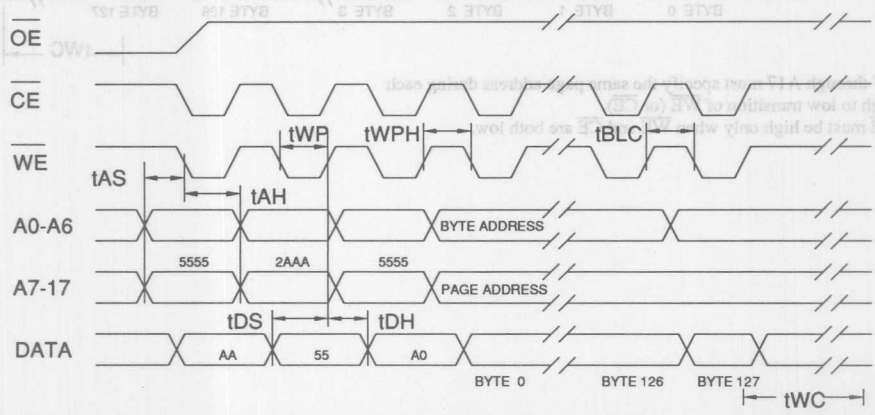


Software Data Protection Disable Algorithm (1,5,6)



Notes:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 128 bytes of data are loaded.
5. A17 must address page to be written.
6. The quadrant determined by A17 acts independently.

Software Protected Program Cycle Waveform



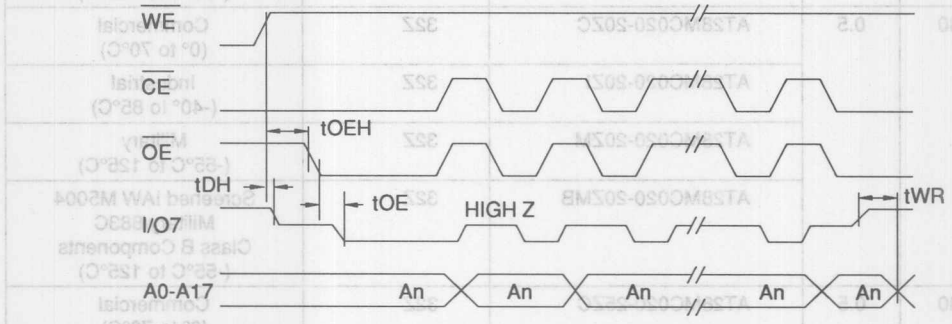
Notes: A0-A14 must conform to the addressing sequence for the first three bytes as shown above. In addition, for each write during this command sequence A17 must be the same.
After the command sequence has been issued and a page write operation follows, the page address inputs (A7-A17) must be the same for each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

$\overline{\text{Data}}$ Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{Data}}$ Polling Waveforms



Notes: For $\overline{\text{DATA}}$ Polling operations the state of A17 must be the same as it was for the byte or page write operation.

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	80	0.5	AT28MC020-15ZC	32Z	Commercial (0° to 70°C)
			AT28MC020-15ZI	32Z	Industrial (-40° to 85°C)
			AT28MC020-15ZM	32Z	Military (-55°C to 125°C)
			AT28MC020-15ZMB	32Z	Screened IAW M5004 Military/883C Class B Components (-55°C to 125°C)
200	80	0.5	AT28MC020-20ZC	32Z	Commercial (0° to 70°C)
			AT28MC020-20ZI	32Z	Industrial (-40° to 85°C)
			AT28MC020-20ZM	32Z	Military (-55°C to 125°C)
			AT28MC020-20ZMB	32Z	Screened IAW M5004 Military/883C Class B Components (-55°C to 125°C)
250	80	0.5	AT28MC020-25ZC	32Z	Commercial (0° to 70°C)
			AT28MC020-25ZI	32Z	Industrial (-40° to 85°C)
			AT28MC020-25ZM	32Z	Military (-55°C to 125°C)
			AT28MC020-25ZMB	32Z	Screened IAW M5004 Military/883C Class B Components (-55°C to 125°C)

Package Type	
32Z	32 Lead, Non-Windowed, Ceramic Dual Inline 32D6 Compatible Multi-Chip Module (MCM)

4 Megabit (512K x 8) Paged CMOS E^2PROM Module

Preliminary

Features

- **Fast Read Access Time - 150 ns**
- **Automatic Page Write Operation**
  - **Internal Address and Data Latches for 128 Bytes**
  - **Internal Control Timer**
- **Fast Write Cycle Time**
  - **Page Write Cycle Time - 10 ms maximum**
  - **1 to 128 Byte Page Write Operation**
- **Low Power Dissipation**
  - **80 mA Active Current**
  - **5 mA CMOS Standby Current**
- **Hardware and Software Data Protection**
- **DATA Polling for End of Write Detection**
- **High Reliability CMOS Technology**
  - **Endurance: 10^4 Cycles**
  - **Data Retention: 10 years**
- **Single 5 V ± 10% Supply**
- **CMOS and TTL Compatible Inputs and Outputs**
- **JEDEC Approved Byte-Wide Pinout**
- **Full Military, Commercial and Industrial Temperature Ranges**

Description

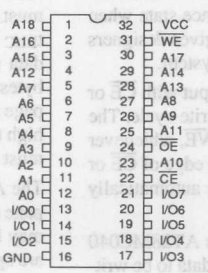
The AT28MC040 is a high-performance Electrically Erasable and Programmable Read Only Memory. Its four megabitS of memory is organized as 524,288 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 150 ns with power dissipation of just 440 mW. When the device is deselected, the CMOS standby current is less than 5 mA.

The AT28MC040 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 128-byte page register to allow writing of up to 128 bytes simultaneously. During a write cycle, the address and 1 to 128 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{\text{DATA}}$ polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's 28MC040 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes.

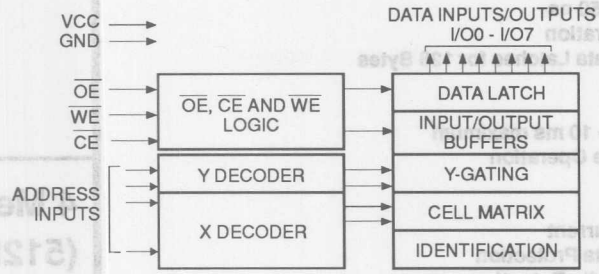
Pin Configurations

Pin Name	Function
A0 - A18	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs



PRELIMINARY

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6 V to +6.25 V
All Output Voltages with Respect to Ground	-0.6 V to V_{CC} +0.6 V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6 V to +13.5 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: The AT28MC040 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

BYTE WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started it will automatically time itself to completion.

PAGE WRITE: The page write operation of the AT28MC040 allows one to one hundred twenty-eight bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; the first byte written can then be followed by one to one hundred twenty-seven additional bytes. Each successive byte must be written within 150 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded the AT28MC040 will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A7-A18 inputs. For each $\overline{WE}$ high to low transition during the page write operation, A7 - A18 must be the same.

The A0 to A6 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

(continued on next page)

Device Operation (Continued)

$\overline{\text{DATA}}$ POLLING: The AT28MC040 features $\overline{\text{DATA}}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{\text{DATA}}$ Polling may begin at anytime during the write cycle.

TOGGLE BIT: in addition to $\overline{\text{DATA}}$ Polling the AT28MC040 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 roggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Atmel has incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE PROTECTION: Hardware features protect against inadvertent writes to the AT28MC040 in the following ways: (a) V_{CC} sense - if V_{CC} is below 3.8 V (typical) the write function is inhibited; (b) V_{CC} power-on delay - once V_{CC} has reached 3.8 V the device will automatically time out 5 ms (typical) before allowing a write: (c) write inhibit - holding any one of $\overline{\text{OE}}$ low, $\overline{\text{CE}}$ high or $\overline{\text{WE}}$ high inhibits write cycles; (d) noise filter - pulses of less than 15 ns (typical) on the $\overline{\text{WE}}$ or $\overline{\text{CE}}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature has been implemented on the AT28MC040. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the AT28MC040 is shipped from Atmel with SDP disabled.

SDP is enabled by the host system issuing a series of three write commands; three specific bytes of data are written to three specific addresses (refer to Software Data Protection Algorithm). After writing the three byte command sequence and after t_{WC} the selected quadrant pointed to by A17 and A18 will be protected against inadvertent write operations. Because the AT28MC040 is comprised of four discrete memory devices, the user must perform the three byte command sequence four times; once to each quadrant selected by the four logic states of A17 and A18.

It should be noted, that once protected the host may still perform a byte or page write to the AT28MC040. This is done by preceding the data to be written by the same three byte command sequence used to enable SDP.

Once set, SDP will remain active unless the disable command sequence is issued. Power transitions do not disable SDP and SDP will protect the AT28MC040 during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not written to the device and the memory addresses used in the sequence may be written with data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the three byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, read operations will effectively be polling operations.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	20	40	pF	V_{IN} = 0 V
C_{OUT}	20	40	pF	V_{OUT} = 0 V

Note: 1. This parameter is characterized and is not 100% tested.

D.C. and A.C. Operating Range

		AT28MC040-15	AT28MC040-20	AT28MC040-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 10%	5 V ± 10%	5 V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.

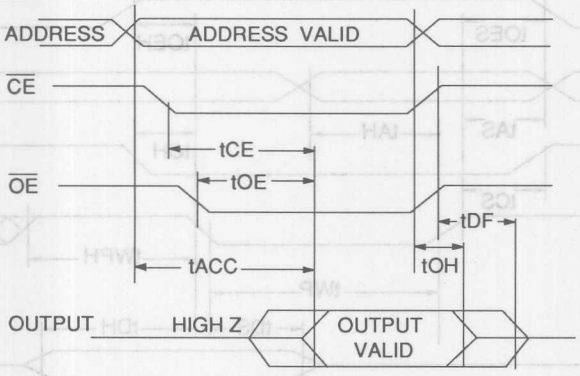
D.C. Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC} + 1 V		20	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0 V to V_{CC}		20	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC}-0.3 V to V_{CC} + 1 V		5	mA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0 V to V_{CC} + 1 V		8	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA		80	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		.45	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V

A.C. Read Characteristics

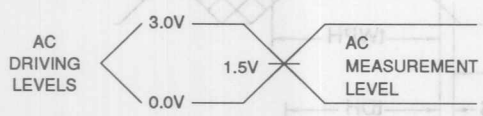
Symbol	Parameter	AT28MC040-15 Min	AT28MC040-15 Max	AT28MC040-20 Min	AT28MC040-20 Max	AT28MC040-25 Min	AT28MC040-25 Max	Units
t_{ACC}	Address to Output Delay		150		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		150		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	70	0	80	0	100	ns
t_{DF} (3,4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	55	0	60	0	70	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

A.C. Read Waveforms



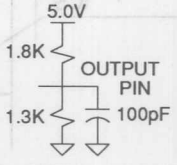
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

Output Test Load

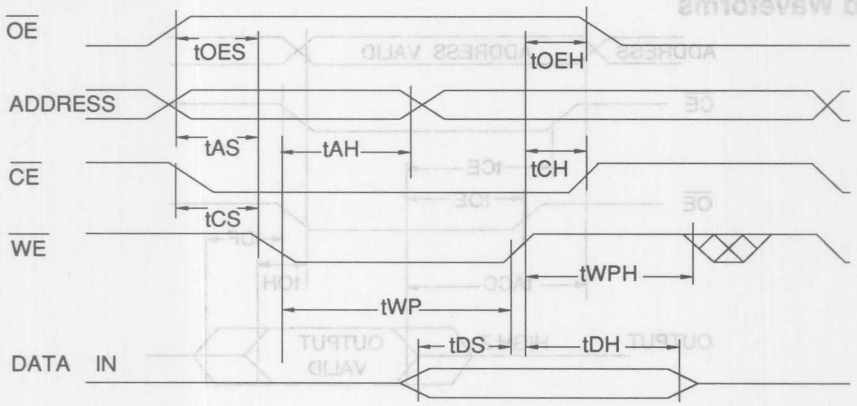


A.C. Write Characteristics

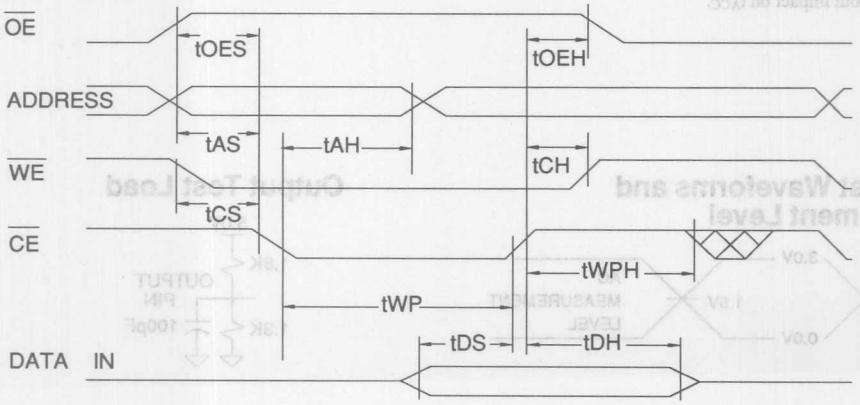
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	10		ns
t_{AH} (1)	Address Hold Time	100		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	150		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	10		ns
t_{WC}	Write Cycle Time		10	ms

Notes: 1. A17 and A18 must remain valid throughout the $\overline{WE}$ or $\overline{CE}$ low pulse.

A.C. Write Waveforms- $\overline{WE}$ Controlled



A.C. Write Waveforms- $\overline{CE}$ Controlled

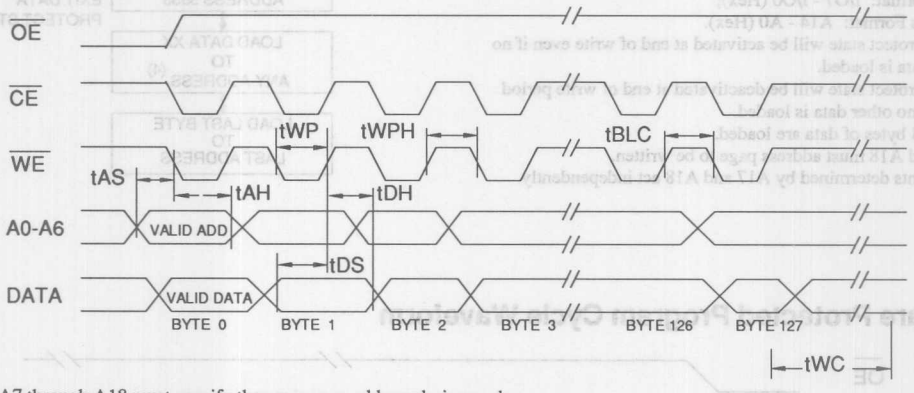


Page Mode Characteristics

Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	10		ns
t_{AH} (1)	Address Hold Time	100		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}	Data Hold Time	10		ns
t_{WP}	Write Pulse Width	150		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	50		ns

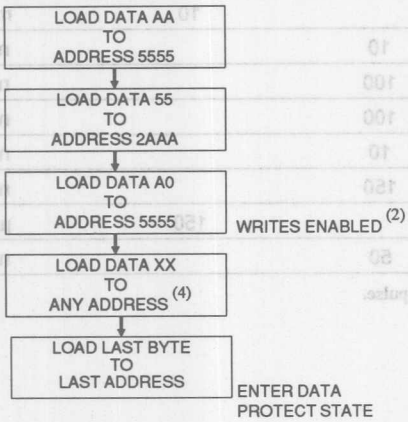
Notes: 1. A17 and A18 must remain valid throughout the $\overline{WE}$ or $\overline{CE}$ low pulse.

Page Mode Write Waveforms

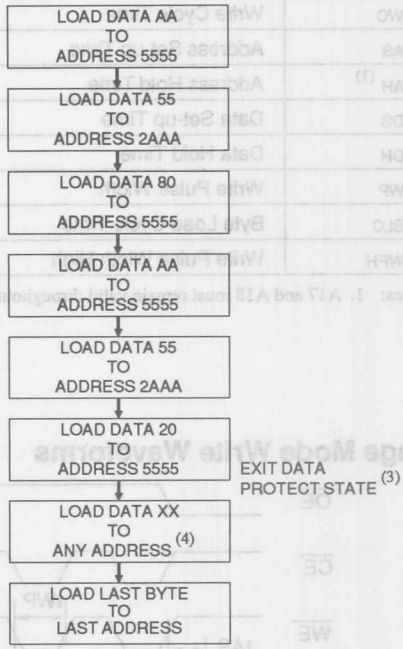


Notes: A7 through A18 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Software Data Protection Enable Algorithm (1,5,6)

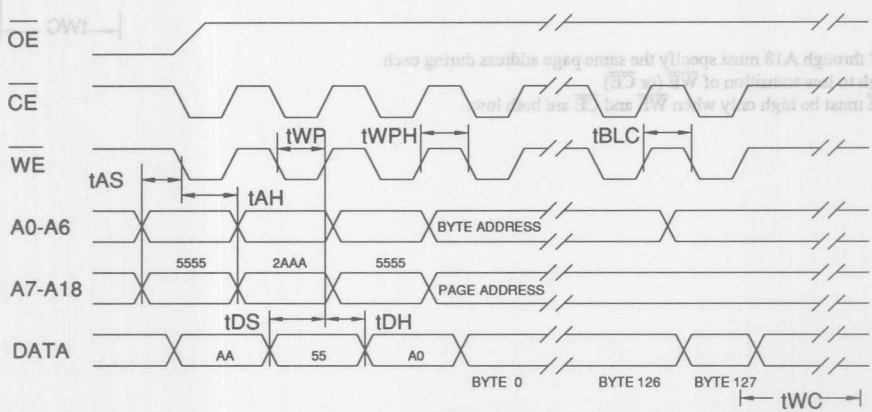


Software Data Protection Disable Algorithm (1,5,6)



Notes:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 128 bytes of data are loaded.
5. A17 and A18 must address page to be written.
6. Quadrants determined by A17 and A18 act independently.

Software Protected Program Cycle Waveform



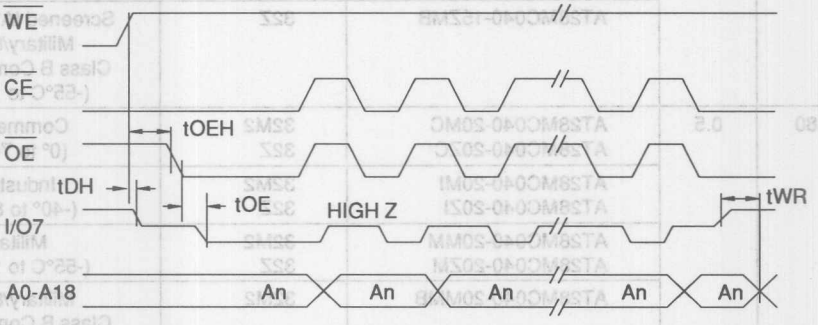
Notes: A0-A14 must conform to the addressing sequence for the first three bytes as shown above. In addition, for each write during this command sequence A17 and A18 must be the same.
After the command sequence has been issued and a page write operation follows, the page address inputs (A7-A18) must be the same for each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Data Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

Data Polling Waveforms



Notes: For DATA Polling operations the states of A17 and A18 must be the same as they were for the byte or page write operation.

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	80	0.5	AT28MC040-15MC AT28MC040-15ZC	32M2 32Z	Commercial (0° to 70°C)
			AT28MC040-15MI AT28MC040-15ZI	32M2 32Z	Industrial (-40° to 85°C)
			AT28MC040-15MM AT28MC040-15ZM	32M2 32Z	Military (-55°C to 125°C)
			AT28MC040-15MMB	32M2	Military/883C Class B Components (-55°C to 125°C)
			AT28MC040-15ZMB	32Z	Screened IAW M5004 Military/883C Class B Components (-55°C to 125°C)
200	80	0.5	AT28MC040-20MC AT28MC040-20ZC	32M2 32Z	Commercial (0° to 70°C)
			AT28MC040-20MI AT28MC040-20ZI	32M2 32Z	Industrial (-40° to 85°C)
			AT28MC040-20MM AT28MC040-20ZM	32M2 32Z	Military (-55°C to 125°C)
			AT28MC040-20MMB	32M2	Military/883C Class B Components (-55°C to 125°C)
			AT28MC040-20ZMB	32Z	Screened IAW M5004 Military/883C Class B Components (-55°C to 125°C)
250	80	0.5	AT28MC040-25MC AT28MC040-25ZC	32M2 32Z	Commercial (0° to 70°C)
			AT28MC040-25MI AT28MC040-25ZI	32M2 32Z	Industrial (-40° to 85°C)
			AT28MC040-25MM AT28MC040-25ZM	32M2 32Z	Military (-55°C to 125°C)
			AT28MC040-25MMB	32M2	Military/883C Class B Components (-55°C to 125°C)
			AT28MC040-25ZMB	32Z	Screened IAW M5004 Military/883C Class B Components (-55°C to 125°C)

Package Type	
32M2	32 Lead, Non-Windowed, Ceramic Dual Inline 32D6 Compatible Flatpack Module (Module)
32Z	32 Lead, Non-Windowed, Ceramic Dual Inline 32D6 Compatible Multi-Chip Module (MCM)

Using Atmel's CMOS E²PROMs

E²PROMs offer many features desired for present day memory systems. They are non-volatile, preserving data for years whether or not power is applied. They provide high density memory storage, with one-megabit devices now available. They offer high speed reads and can be re-written on a byte or page basis.

Five-volt-only signals are used to operate the devices. When writing new data only the data bytes that are desired to be changed need be rewritten. No erasure steps are required before rewriting any memory location. Since all of Atmel's products are made with CMOS technology, the supply current required to operate Atmel E²PROMs is low. Other features such as $\overline{\text{DATA}}$ polling, internal error correction and software data protection make Atmel E²PROMs the correct solution for many memory systems.

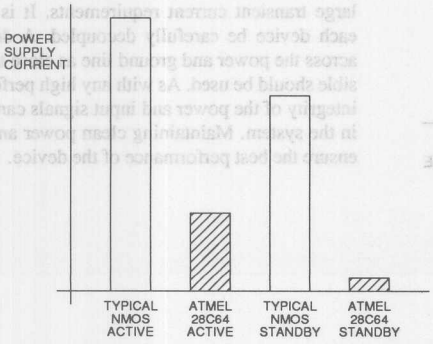
CMOS Versus NMOS E²PROMs

CMOS is quickly becoming the dominant MOS technology. Many systems however, have been designed without the use of CMOS products, and therefore do not have the benefits of this advanced process technology. The most obvious advantage of CMOS is in the power savings. Figure 1 shows a comparison of a typical 64K NMOS E²PROM current specification versus that of Atmel's AT28C64. The power advantage of CMOS is quite clear. The power savings actually does more than just reduce the drain on the power supply. The low power consumption helps to keep system temperatures lower, reducing the need for cooling and allowing for greater packing density on boards. With less internally generated heat, CMOS products can be more reliable than their NMOS counterparts.

The TTL and CMOS compatible inputs and outputs of Atmel's CMOS E²PROMs offer additional advantages. The input stages consume no active power when the input voltage is at ground or the positive supply level. Figure 2 shows the typical power consumption curve for an Atmel input stage versus input voltage. By using full CMOS input levels to the device, the active power consumption can be reduced below the specified levels.

The outputs of Atmel E²PROMs drive to the full limits of the supply voltage. When driving other CMOS input stages, this full swing drive capability can actually reduce the power consumed by other devices within

Figure 1. Comparison of typical NMOS 64K E²PROM current consumption to that of Atmel's AT28C64.



the system! Also, by driving to the high power supply limit, Atmel devices improve the noise margin of the high input level of the device they are driving as compared to typical NMOS devices which do not drive to the high supply level (Figure 3).

Upgrading from NMOS to CMOS

It is generally quite easy to upgrade a system using NMOS devices to use CMOS parts. In most cases, NMOS E^{2}PROM devices organized from 512 by 8 to 32K by 8 may be directly replaced by an Atmel CMOS device of the same density and pinout. No hardware or software changes need necessarily be made when upgrading the system.

In some cases, power switching transistors have been used to power-down NMOS E^{2}PROMs while the rest of the system remains active. In such a state, the DATA lines of the NMOS E^{2}PROM do not load the DATA bus of the system. A CMOS device in such a configuration may show substantial input current through the DATA pins if the DATA bus is higher than the E^{2}PROM's power supply input. To permit CMOS devices to work properly in such a system, it is recommended that the switching transistor be removed from the power supply of the E^{2}PROM. With the low power standby mode of Atmel's E^{2}PROMs, the power switching is not necessary. The low power consumption of the CMOS device will not adversely affect the system power consumption and there will be negligible input leakage at the E^{2}PROM DATA pins. Additionally, the power consumption of the E^{2}PROM will be much lower when selected and, with the removal of the switching transistor, the number of devices in the system will be reduced.

Figure 2. Typical power consumption curve for Atmel input stage versus input level.

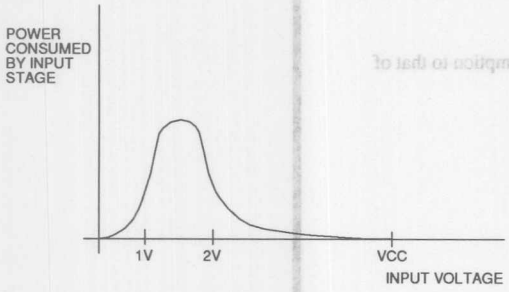
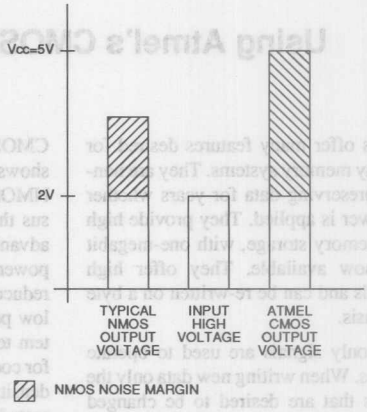


Figure 3. High input voltage noise margin comparison of typical NMOS output to Atmel CMOS output.



Read Cycle

The E^{2}PROM read cycle is controlled by the $\overline{CE}$ and $\overline{OE}$ signals. When $\overline{CE}$ and $\overline{OE}$ are both low, data is read from the device. The address inputs specify the memory location being read. The address and data lines are not latched during a read cycle; changing the address while $\overline{CE}$ and $\overline{OE}$ are low will result in the output of the device changing. If $\overline{CE}$ or $\overline{OE}$ is high, the outputs are put in a high impedance state. This dual-line control allows for flexibility in avoiding bus line contention. There is no need for periodic refresh of the memory; E^{2}PROMs retain their data whether or not power is applied. Addresses may be randomly selected; there are no restrictions on address lines.

When $\overline{CE}$ is high, the internal power consumption of the device is greatly reduced; the device is said to be in the standby mode. The power reduction is achieved by turning off the internal circuits of the device. When $\overline{CE}$ is returned low, the internal circuits are again powered on and a new read is performed.

Atmel E^{2}PROMs are designed to provide the fastest access times available among like devices. They therefore may have large transient current requirements. It is recommended that each device be carefully decoupled. A decoupling capacitor across the power and ground line as close to the device as possible should be used. As with any high performance device, the integrity of the power and input signals can affect its operation in the system. Maintaining clean power and input signals will ensure the best performance of the device.

Byte Write Cycle

Writing to Atmel E²PROMs has been designed to minimize the time that the system must spend in issuing commands to the memory device. The write cycle is controlled by $\overline{OE}$, $\overline{CE}$ and $\overline{WE}$. Initiating a write cycle is done with a short pulse on either the $\overline{WE}$ or $\overline{CE}$ input. With $\overline{OE}$ high and $\overline{CE}$ (or $\overline{WE}$) low, the address to be written is latched on the falling edge of $\overline{WE}$ (or $\overline{CE}$, whichever occurred last). The data to be written is latched on the rising edge of $\overline{WE}$ (or $\overline{CE}$, whichever occurred first). The latching of the address and data inputs allows the address and data busses to be used to access other devices while the write is in progress. During its write cycle, data may not be read from the E²PROM (the device may however be polled to see if the write is completed).

Internal to the E²PROM device, the write cycle can be divided into two steps. The first is to load the data into a temporary buffer; this operation can be done very quickly (measured in nanoseconds). The second step is to perform the nonvolatile storage. It takes considerably longer for this step (up to several milliseconds). After the nonvolatile storage is completed, a new read or write cycle may begin immediately.

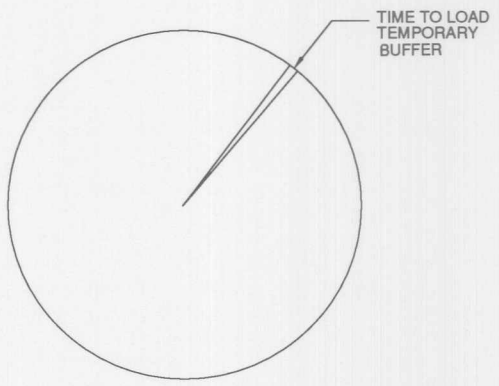
Page Write Cycle

To improve the effective write time when large sections of the memory are being rewritten, some Atmel E²PROMs provide a page write operation. The page write allows a group of bytes to be quickly loaded into the device's temporary buffer and then simultaneously written to the nonvolatile storage elements. Figure 4 is a pie chart showing the time needed for completely loading the temporary 64 byte page buffer of the AT28C256 as a portion of the write cycle time. Clearly, by utilizing the page write with minimum write load times, the write time can effectively be reduced by a factor approximately equal to the page width.

Similar to the writing of a single byte, address location and data to be written are latched on the falling and rising edges of $\overline{WE}$ or $\overline{CE}$. All bytes being written must have the same page address. The page address is determined by the higher order addresses and is specified in the data sheet of each particular device. The page address must be valid during each high to low transition of $\overline{WE}$ or $\overline{CE}$. The $\overline{OE}$ input must be high whenever $\overline{CE}$ and $\overline{WE}$ are low.

During write cycles, only the bytes that are specified to be written are altered; other bytes within the device are not rewritten or otherwise affected. A write cycle will only occur when requested; however, there may be conditions present during such times as power-up or power-down when a system might inadvertently initiate a write cycle. Atmel devices include many features to help prevent inadvertent write cycles. Users of E²PROMs should become familiar with these features.

Figure 4. Time to load 64 bytes to temporary buffer in AT28C256 as a portion of the write cycle time.



Additional Features

Atmel E²PROMs include other features to help ensure reliability and to improve overall system performance. The internal error correction incorporated into Atmel's E²PROMs protects against single bit data errors from appearing in the devices. The user does nothing to utilize the feature; whenever a write or read cycle is performed, parity generation or checking occurs internally to the E²PROM device to help ensure the integrity of the data.

The inputs and outputs of Atmel devices contain circuitry to protect the device from electrostatic damage. Even though the devices do have this protection circuitry, it is strongly recommended that safe handling procedures be used with these devices. All equipment and personnel that may come in contact with the devices should be well grounded. Other features such as $\overline{DATA}$ polling, READY/$\overline{BUSY}$ outputs or toggle bit are available and may be employed by users as required by their particular application.

TIME TO LOAD
TEMPORARY
BUFFER

E^2PROM Data Protection

Advantages of E^2PROMs

E^2PROMs provide the memory solution wherever reprogrammable, nonvolatile memory is required. They are easy to use, requiring little or no support hardware such as refresh clocks or batteries. Each memory location can be selectively changed without impact on any other location; blanket erasure and rewriting of the entire device or a large section of it is not required.

E^2PROMs made at Atmel were designed to provide the best features available. Atmel E^2PROMs provide high speed read access times so that many applications can use them without inserting costly wait states. The page mode write operation of Atmel E^2PROMs allows for the fastest effective write time available in E^2PROM memories. Since all of Atmel's devices are made in CMOS, they offer the benefits of low operating and standby power.

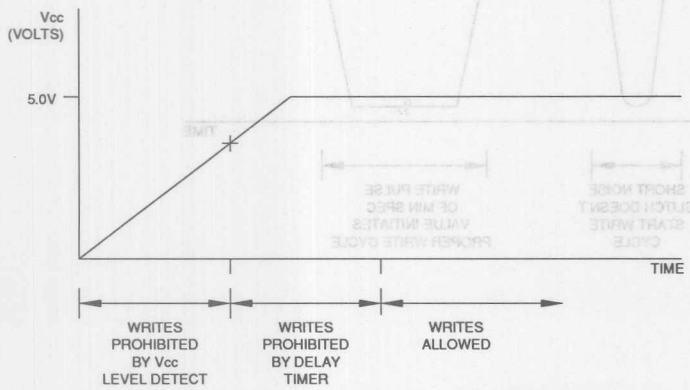
In order to take advantage of all of the benefits of Atmel E^2PROMs, care must be taken to maintain the integrity of the data. While an E^2PROM will retain its data for many years with or without power applied, improper operation of the device could result in data being inadvertently rewritten.

When is Data Susceptible to Corruption

In the use of any memory device, it is expected that the data stored in it is available as it is written. This is especially true of E^2PROMs since their code often controls the operation of the system in which they are contained. Unlike most other memory types that are rewritten in systems, E^2PROMs are often expected to retain their data for a period of many years, with or without power applied and during power transitions. For these reasons, added attention is given to avoid corrupting data in E^2PROMs.

There are a number of situations in which data is particularly prone to corruption. These situations include powering on and off of the devices, noise spikes on the control lines and system glitches. Atmel E^2PROMs include features to help protect against each of these potential sources of inadvertent writes. Atmel data protection features are broken down into two different types: hardware data protection features and software data protection features.

Figure 1.



Atmel Hardware Data Protection Features

Atmel E^2PROMs include four different types of hardware data protection. These features provide protection against most inadvertent writes that might occur in a system. Atmel hardware data protection features include: three line write control, power level sense detector, power on delay timer and noise filters on $\overline{CE}$ and $\overline{WE}$.

THREE-LINE WRITE CONTROL: In order to write a device the $\overline{OE}$ signal must be high with the $\overline{CE}$ and $\overline{WE}$ signals low. Holding any of the three lines in the opposite state will prohibit a write cycle. For example, whenever the $\overline{OE}$ signal is low, a write to the device cannot be started.

POWER LEVEL SENSE DETECTOR: An active circuit in Atmel E^2PROMs monitors the level of the supply voltage to the device. If the supply is below 3.8 volts, typical, write cycles to the devices can not be activated.

POWER ON DELAY TIMER: As power is applied to Atmel E^2PROMs, the power level sense detector will issue an internal signal that indicates that the supply is above the sense level. At this time an internal timer is initiated that times out in typically 5 ms. During this time period, writes to the device cannot be performed. This delay period serves two purposes. First, it allows the supply level additional time to rise to within the standard operating region before writes are permitted. Secondly, it lets the system stabilize and present the correct levels to the control pins of the E^2PROM so that the E^2PROM doesn't react to its inputs before they are actually valid. Figure 1 shows the combined action of the power supply level detector and the delay timer upon writes to the device.

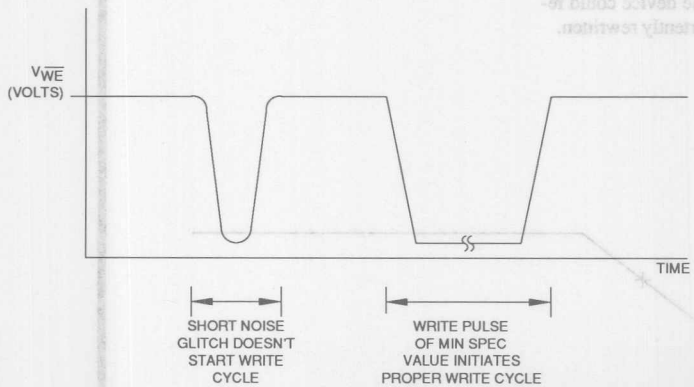
NOISE FILTERS ON $\overline{WE}$ AND $\overline{CE}$: If brief noise pulses below V_{IH} occur on the $\overline{WE}$ or $\overline{CE}$ inputs to the device, a write cycle will not be initiated. Internal to the E^2PROM, a noise filter does not allow the short pulses to activate a write cycle. As shown in Figure 2, write pulses of sufficient length will still initiate writes but short noise spikes on the $\overline{WE}$ or $\overline{CE}$ control lines will not.

Atmel Software Data Protection Feature

Available on some Atmel E^2PROMs is a user selectable feature that requires a software sequence at the beginning of each write cycle in order for a write to be performed. To enable the software data protection feature, a series of three-write commands to specific addresses with specific data must be performed. Once set, the same three-byte code must begin each write request. (A separate write cycle to enable the software feature is not necessary; after any write that is preceded with the three byte code, the software data protection function will be enabled, see Figure 3.) The feature may be disabled by issuing a six-byte code to the device as shown in Figure 4. After being set, the software data protection feature remains active until its disable command is issued. Power transitions will not reset the software data protection feature, but the feature will prevent against inadvertent writes during power transitions.

The software data protection feature protects data against various causes of inadvertent writes. Since it is active during power transitions it protects data when powering on or off the device. Noise spikes that occur on the control lines will be ignored since they will not show the correct address and data needed to start a write cycle. Even for system malfunctions, such as when write pulses of adequate length are given to the device, the software feature can prevent the corruption of the data in the E^2PROM. The address locations used for the software code are not sacrificed from the usable memory array. The device recognizes the software code and does not alter the data stored at the address locations of the code. Byte locations of code are still usable, and don't have to be rewritten.

Figure 2.



System Design Considerations

Designing systems with data integrity in mind can greatly reduce the chance of lost data. The amount of attention needed depends upon the nature of the design. Following are a few areas that might need special attention in certain designs.

External Power On Protection

Many systems will have a PON (power on) signal to control the operation of the system. Such a signal can be gated with the logic creating the $\overline{OE}$ signal to the E²PROM, holding $\overline{OE}$ low when the PON signal is false. Similarly, a PON-type signal could be gated with the $\overline{WE}$ or $\overline{CE}$ logic, forcing $\overline{WE}$ or $\overline{CE}$ high when writes should not be allowed.

If the system does not include a PON-type signal, one can be created from various programmable voltage reference devices. With such a device, the user can select the voltage supply level below which the device cannot be written. It should be noted that in many systems, using Atmel's E²PROMS with their internal power level detection and power delay timer, no additional power on circuitry is required for the device.

Multiple Power Supplies

In systems that utilize more than one power supply, extra care must be taken during power transitions to both the E²PROM and the devices controlling the inputs to the E²PROM. Power on rates of the different supplies are likely to vary. Using programmable voltage reference devices to detect the power level of both supplies and forcing the $\overline{OE}$ pin low when either line is below the desired level may be used in such situations to avoid inadvertent writes.

Memory Cards

Since memory cards are often pushed into and pulled out of systems that are already powered on, they have additional chances of inadvertent writes. If the edge connector is arranged such that power and control lines are not asserted in a prescribed manner, false writes to the device may occasionally occur depending upon how the card is inserted. To provide proper power on sequencing, a card could be designed with its control pins recessed from the edge of the card. Resistors would be placed on the card to connect $\overline{CE}$ and $\overline{WE}$ to V_{CC} and $\overline{OE}$ to ground. This arrangement insures that power is first applied to the device and that the control pins are not in the write state until each pin is being controlled by the host system. Variations of this technique may be used effectively in different systems; the basic idea is to guarantee systematic application of the power and control pins such that a write state is not entered upon insertion or removal of the card from the host.

Figure 3.

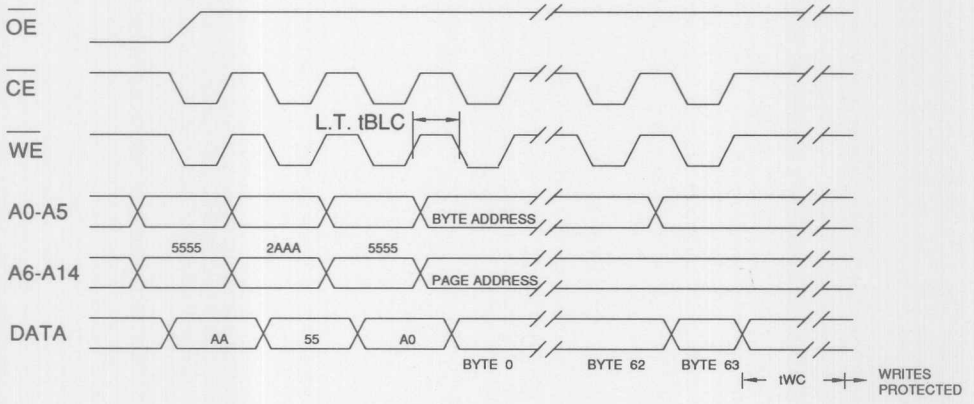
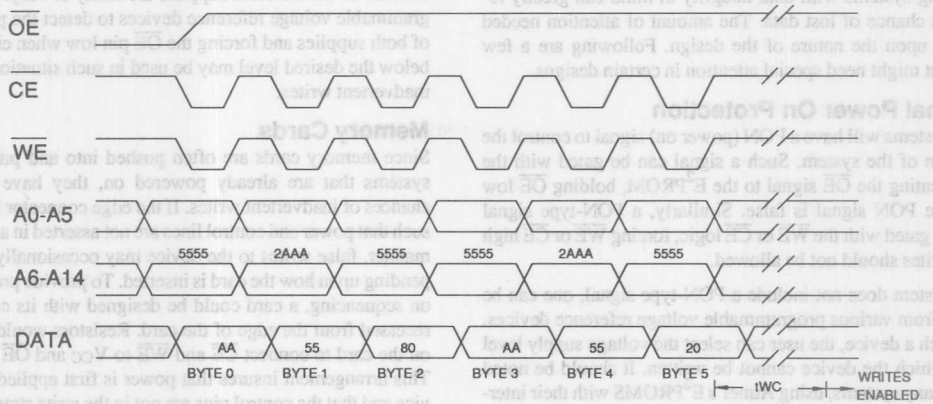


Figure 4.


OE
CE
WE
A0-A5
A6-A14
5555
2AAA
5555
5555
2AAA
5555
DATA
AA
55
80
AA
55
20
BYTE 0
BYTE 1
BYTE 2
BYTE 3
BYTE 4
BYTE 5
tWC
WRITES
ENABLED

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256K (32K x 8) 5-Volt Only CMOS PEROM

Features

- Fast Read Access Time - 90 ns
- Five-Volt-Only Reprogramming
- Page Program Operation
  - Single Cycle Reprogram (Erase and Program)
  - Internal Address and Data Latches for 64 Bytes
- Fast Program Cycle Times
  - Page (64 Byte) Program Time - 10 ms
  - Chip Erase Time - 10 ms
- Internal Program Control Timer
- Low Power Dissipation
  - 80 mA Active Current
  - 300 µA CMOS Standby Current
- Hardware and Software Data Protection
- DATA Polling for End of Program Detection
- High Reliability CMOS Technology
  - 1000 Erase/Program Cycles
  - 10-Year Data Retention
- Single 5 V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- Full Military, Commercial, and Industrial Temperature Ranges

Description

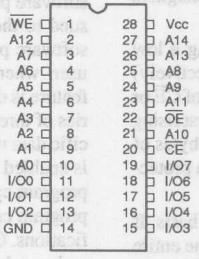
The AT29C256 is a five-volt-only in-system Programmable and Erasable Read Only Memory (PEROM). Its 256K of memory is organized as 32,768 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 90 ns with power dissipation of just 440 mW. When the device is deselected, the CMOS standby current is less than 300 µA.

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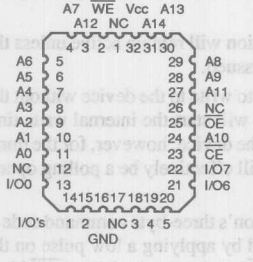
Pin Configurations

Pin Name	Function
A0 - A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

DIP Top View

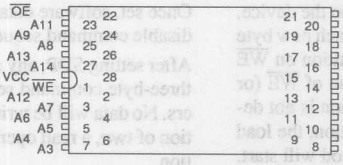


PLCC and LCC Top View



TSOP Top View

Type 1



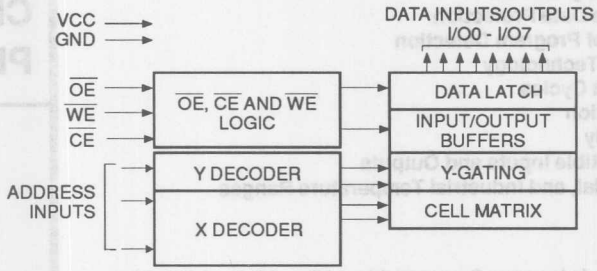
Note: PLCC package pins 1 and 17 are DON'T CONNECT.

Description (Continued)

To allow for simple in-system reprogrammability, the AT29C256 does not require high input voltages for programming. Five-volt-only commands determine the operation of the device. Reading data out of the device is similar to reading from a static RAM. Reprogramming the AT29C256 is performed on a page basis; 64 bytes of data are loaded into the device and then simultaneously programmed. The contents of the entire device may be erased by using a six-byte software code (although erasure before programming is not needed).

During a reprogram cycle, the address locations and 64 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a program cycle, the device will automatically erase the page and then program the latched data using an internal control timer. The end of a program cycle can be detected by $\overline{\text{DATA}}$ polling of I/O7. Once the end of a program cycle has been detected a new access for a read, program or chip erase can begin.

Block Diagram



Device Operation

READ: The AT29C256 is accessed like a static RAM. When $\overline{\text{CE}}$ and $\overline{\text{OE}}$ are low and $\overline{\text{WE}}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{\text{CE}}$ or $\overline{\text{OE}}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

BYTE LOAD: A byte load is performed by applying a low pulse on the $\overline{\text{WE}}$ or $\overline{\text{CE}}$ input with $\overline{\text{CE}}$ or $\overline{\text{WE}}$ low (respectively) and $\overline{\text{OE}}$ high. The address is latched on the falling edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$, whichever occurs last. The data is latched by the first rising edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$. Byte loads are used to enter the 64 bytes of a page to be programmed or the software codes for data protection and chip erasure.

PROGRAM: The device is reprogrammed on a page basis. If a byte of data within a page is to be changed, data for the entire page must be loaded into the device. Any byte that is not loaded during the programming of its page will be erased to read FFh. Once the bytes of a page are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data byte has been loaded into the device, successive bytes are entered in the same manner. Each new byte to be programmed must have its high to low transition on $\overline{\text{WE}}$ (or $\overline{\text{CE}}$) within 150 µs of the low to high transition of $\overline{\text{WE}}$ (or $\overline{\text{CE}}$) of the preceding byte. If a high to low transition is not detected within 150 µs of the last low to high transition, the load period will end and the internal programming period will start. A6 to A14 specify the page address. The page address must be valid during each high to low transition of $\overline{\text{WE}}$ (or $\overline{\text{CE}}$). A0 to A5 specify the byte address within the page. The bytes may be loaded in any order; sequential loading is not required.

SOFTWARE DATA PROTECTION: A software controlled data protection feature is available on the AT29C256. Once the software protection is enabled a software algorithm must be issued to the device before a program may be performed. The software protection feature may be enabled or disabled by the user; when shipped from Atmel, the software data protection feature is disabled. To enable the software data protection, a series of three program commands to specific addresses with specific data must be performed. After the software data protection is enabled the same three program commands must begin each program cycle in order for the programs to occur. All software program commands must obey the page program timing specifications. Once set, the software data protection feature remains active unless its disable command is issued. Power transitions will not reset the software data protection feature, however the software feature will guard against inadvertent program cycles during power transitions.

Once set, software data protection will remain active unless the disable command sequence is issued.

After setting SDP, any attempt to write to the device without the three-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, a read operation will effectively be a polling operation.

After the software data protection's three-byte command code is given, a byte load is performed by applying a low pulse on the $\overline{\text{WE}}$ or $\overline{\text{CE}}$ input with $\overline{\text{CE}}$ or $\overline{\text{WE}}$ low (respectively) and $\overline{\text{OE}}$ high.

continued on next page

Device Operation (Continued)

The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$.

The 64 bytes of data must be loaded into each sector. Any byte that is not loaded during the programming of its sector will be erased to read FFh. Once the bytes of a sector are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data byte has been loaded into the device, successive bytes are entered in the same manner. Each new byte to be programmed must have its high to low transition on $\overline{WE}$ (or $\overline{CE}$) within 150 µs of the low to high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding byte. If a high to low transition is not detected within 150 µs of the last low to high transition, the load period will end and the internal programming period will start. A6 to A14 specify the sector address. The sector address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A5 specify the byte address within the sector. The bytes may be loaded in any order; sequential loading is not required.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT29C256 in the following ways: (a) V_{CC} sense— if V_{CC} is below 3.8 V (typical), the program function is inhibited. (b) V_{CC} power on delay— once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 5 ms (typical) before programming. (c) Program inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (d) Noise filter— pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer and may be accessed by a hardware operation. For details, see Operating Modes or Product Identification.

$\overline{DATA}$ POLLING: The AT29C256 features $\overline{DATA}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{DATA}$ polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ polling the AT29C256 provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

OPTIONAL CHIP ERASE MODES: The entire device may be erased by either using a six-byte software code or high voltage. For details, please contact Atmel.

3

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6 V to +6.25 V
All Output Voltages with Respect to Ground	-0.6 V to V_{CC} +0.6 V
Voltage on $\overline{OE}$ with Respect to Ground	-0.6 V to +13.5 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Note: 1. This parameter is characterized and is not 100% tested.

D.C. and A.C. Operating Range

		AT29C256-90	AT29C256-12	AT29C256-15	AT29C256-20	AT29C256-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.		-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V± 10%	5 V± 10%	5 V± 10%	5 V ± 10%	5 V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Ai	D_{OUT}
Program[2]	V_{IL}	V_{IH}	V_{IL}	Ai	D_{IN}
5V Chip Erase	V_{IL}	V_{IH}	V_{IL}	Ai	
Standby/Write Inhibit	V_{IH}	X[1]	X	X	High Z
Write Inhibit	X	X	V_{IH}		
Write Inhibit	X	V_{IL}	X		
Output Disable	X	V_{IH}	X		High Z
High Voltage Chip Erase	V_{IL}	V_H [3]	V_{IL}	X	High Z
Product Identification	V_{IL}	V_{IL}	V_{IH}	A1-A14 = V_{IL}, A9 = V_H, A0 = V_{IL}	Manufacturer Code[4]
				A1-A14 = V_{IL}, A9 = V_H, A0 = V_{IH}	Device Code[4]

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.
3. V_H = 12.0 V ± 0.5 V.
4. Manufacturer Code: 1F, Device Code: DC

D.C. Characteristics

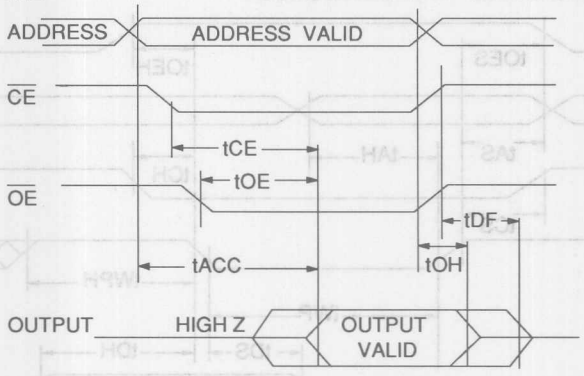
Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0 V to V_{CC}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC}-0.3 V to V_{CC}		300	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0 V to V_{CC}		3	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA		80	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA	2.4		V
V_{OH2}	Output High Voltage CMOS	I_{OH} = -100 µA; V_{CC} = 4.5 V	4.2		V

A.C. Read Characteristics

Symbol	Parameter	AT29C256-90 Min	AT29C256-90 Max	AT29C256-12 Min	AT29C256-12 Max	AT29C256-15 Min	AT29C256-15 Max	AT29C256-20 Min	AT29C256-20 Max	AT29C256-25 Min	AT29C256-25 Max	Units
t_{ACC}	Address to Output Delay		90		120		150		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		90		120		150		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	40	0	50	0	70	0	80	0	100	ns
t_{DF} (3,4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	40	0	40	0	50	0	55	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		0		ns

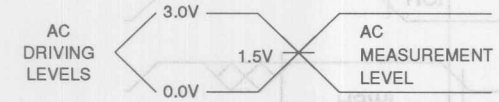
3

A.C. Read Waveforms



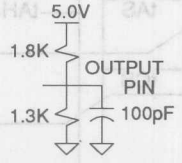
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

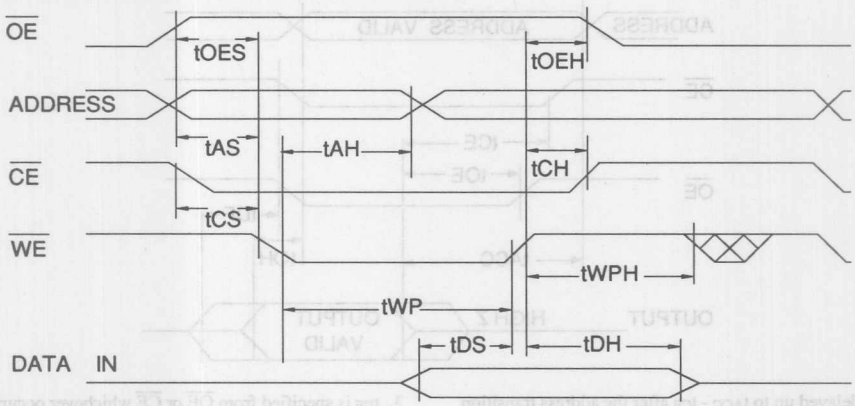
Output Test Load



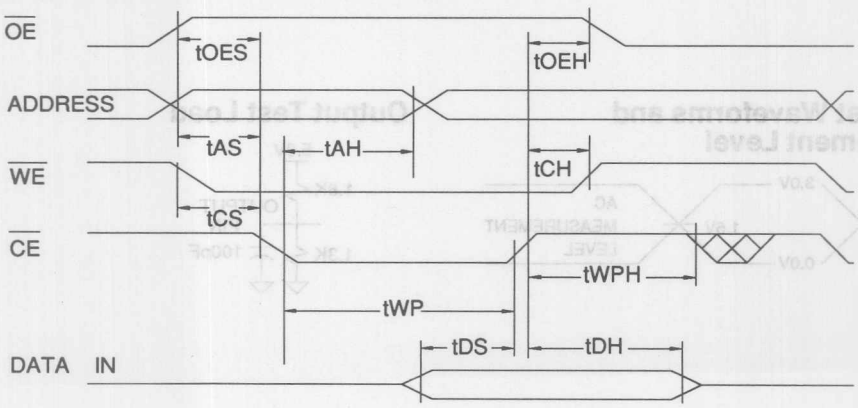
A.C. Byte Load Characteristics

Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	90		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{WC}	Write Cycle Time		10	ms

A.C. Byte Load Waveforms- $\overline{WE}$ Controlled



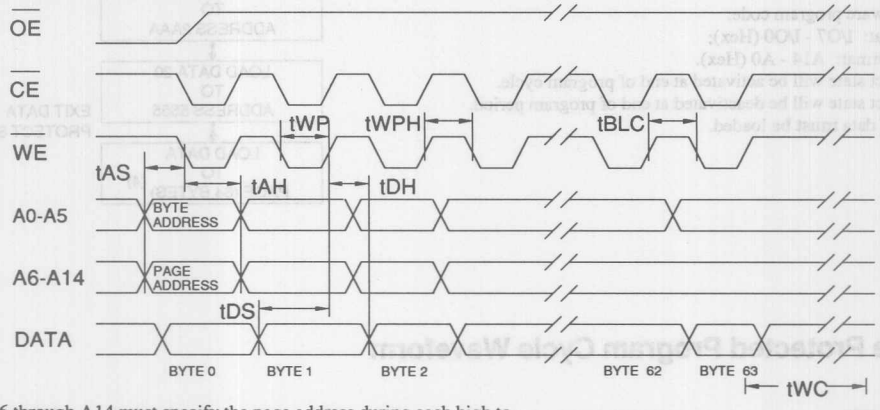
A.C. Byte Load Waveforms- $\overline{CE}$ Controlled



Program Cycle Characteristics

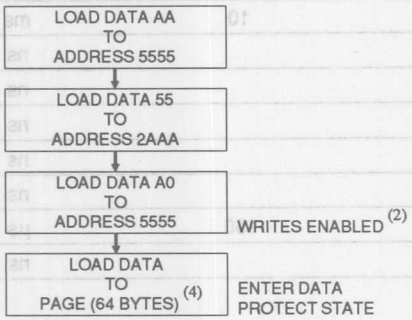
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	120		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	100		ns

Program Cycle Waveforms

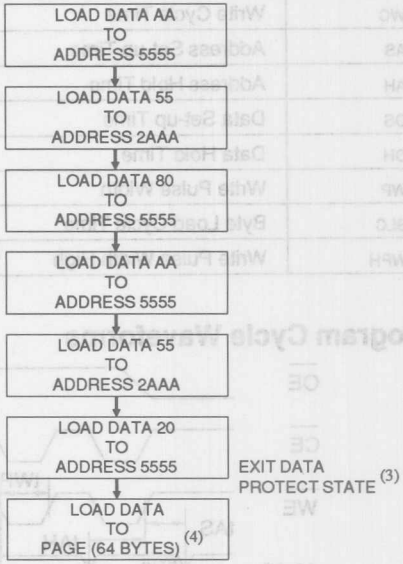


Notes: A6 through A14 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
All bytes that are not loaded within the page being programmed will be erased to FF.

Software Data Protection Enable Algorithm [1]

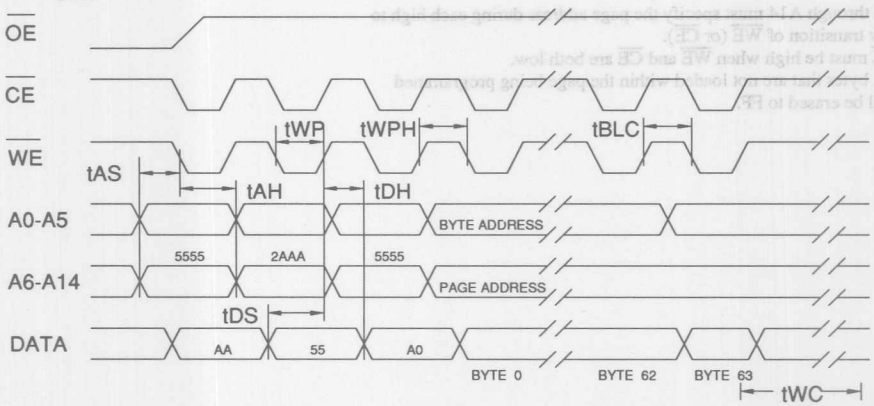


Software Data Protection Disable Algorithm [1]



Notes for software program code:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Data Protect state will be activated at end of program cycle.
3. Data Protect state will be deactivated at end of program period.
4. 64 bytes of data **must be** loaded.

Software Protected Program Cycle Waveform



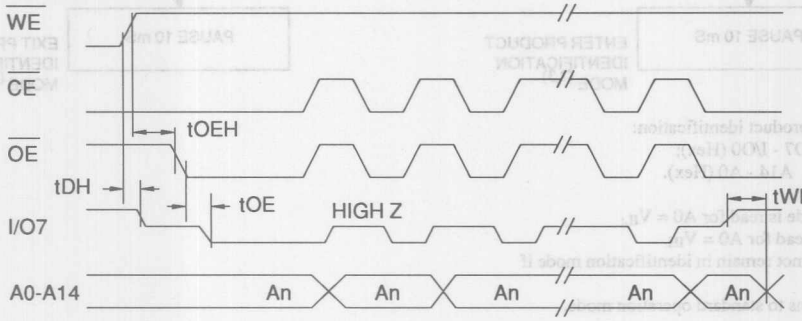
Notes:
1. A6 through A14 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
2. $\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
3. **All bytes that are not loaded within the page being programmed will be erased to FF.**

$\overline{\text{Data}}$ Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{Data}}$ Polling Waveforms

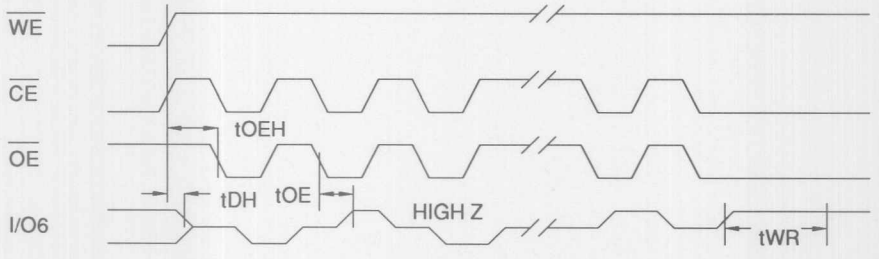


Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

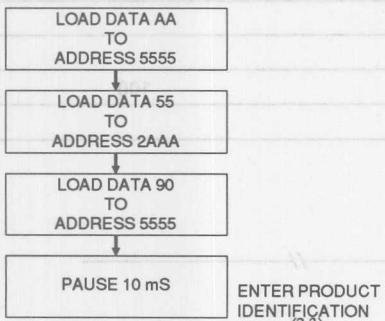
Note: 1. These parameters are characterized and not 100% tested.

Toggle Bit Waveforms

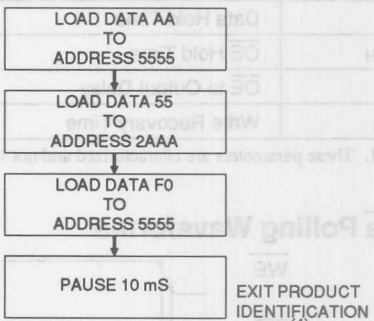


Notes:
1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry (1)



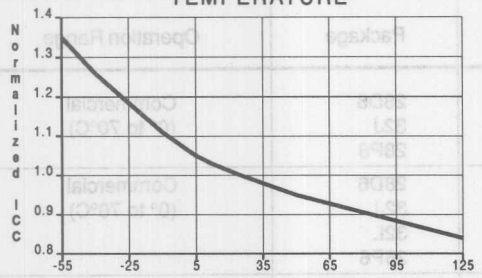
Software Product Identification Exit (1)



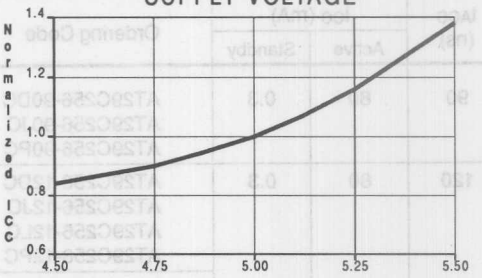
Notes for software product identification:

1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. A1 - A14 = V_{IL}.
   Manufacture Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.

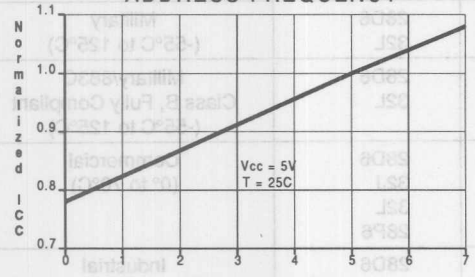
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	80	0.3	AT29C256-90DC AT29C256-90JC AT29C256-90PC	28D6 32J 28P6	Commercial (0° to 70°C)
120	80	0.3	AT29C256-12DC AT29C256-12JC AT29C256-12LC AT29C256-12PC	28D6 32J 32L 28P6	Commercial (0° to 70°C)
			AT29C256-12DI AT29C256-12JI AT29C256-12LI AT29C256-12PI	28D6 32J 32L 28P6	Industrial (-40° to 85°C)
			AT29C256-12DM AT29C256-12LM	28D6 32L	Military (-55°C to 125°C)
			AT29C256-12DM/883 AT29C256-12LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	80	0.3	AT29C256-15DC AT29C256-15JC AT29C256-15LC AT29C256-15PC	28D6 32J 32L 28P6	Commercial (0° to 70°C)
			AT29C256-15DI AT29C256-15JI AT29C256-15LI AT29C256-15PI	28D6 32J 32L 28P6	Industrial (-40° to 85°C)
			AT29C256-15DM AT29C256-15LM	28D6 32L	Military (-55°C to 125°C)
			AT29C256-15DM/883 AT29C256-15LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	80	0.3	AT29C256-20DC AT29C256-20JC AT29C256-20LC AT29C256-20PC	28D6 32J 32L 28P6	Commercial (0° to 70°C)
			AT29C256-20DI AT29C256-20JI AT29C256-20LI AT29C256-20PI	28D6 32J 32L 28P6	Industrial (-40° to 85°C)
			AT29C256-20DM AT29C256-20LM	28D6 32L	Military (-55°C to 125°C)
			AT29C256-20DM/883 AT29C256-20LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	80	0.3	AT29C256-25DC AT29C256-25JC AT29C256-25LC AT29C256-25PC	28D6 32J 32L 28P6	Commercial (0° to 70°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
250	80	0.3	AT29C256-25DI AT29C256-25JI AT29C256-25LI AT29C256-25PI	28D6 32J 32L 28P6	Industrial (-40° to 85°C)
			AT29C256-25DM AT29C256-25LM	28D6 32L	Military (-55°C to 125°C)
			AT29C256-25DM/883 AT29C256-25LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	80	0.3	AT29C256-12TC	28T	Commercial (0° to 70°C)
150	80	0.3	AT29C256-15TC	28T	Commercial (0° to 70°C)

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28T	28 Lead, Thin Small Outline Package (TSOP)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
250	80	0.3	AT29C256-25DI AT29C256-25JI AT29C256-25LI AT29C256-25PI	28DB 32J 32L 28P6	Industrial (-40° to 85°C)
			AT29C256-25DM AT29C256-25LM	28DB 32L	Military (-55°C to 125°C)
			AT29C256-25DM/883 AT29C256-25LM/883	28DB 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	80	0.3	AT29C256-12TC	28T	Commercial (0° to 70°C)
150	80	0.3	AT29C256-15TC	28T	Commercial (0° to 70°C)

Package Type	
28DB	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28T	28 Lead, Thin Small Outline Package (TSOP)

Features

- Single 3.3 V ± 10% Supply
- Three-Volt-Only Read and Write Operation
- Software Protected Programming
- Low Power Dissipation
  - 15 mA Active Current
  - 20 µA CMOS Standby Current
- Fast Read Access Time - 200 ns
- Sector Program Operation
  - Single Cycle Reprogram (Erase and Program)
  - 512 Sectors (64 bytes/sector)
  - Internal Address and Data Latches for 64 Bytes
- Fast Sector Program Cycle Time - 20 ms Max.
- Internal Program Control and Timer
- DATA Polling for End of Program Detection
- High Reliability CMOS Technology
  - 1000 Program Cycles per Sector
  - 10-Year Data Retention
- CMOS and TTL Compatible Inputs and Outputs
- Commercial and Industrial Temperature Ranges

Description

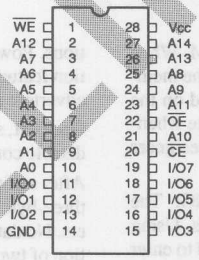
The AT29LV256 is a three-volt-only in-system Programmable Erasable Read Only Memory (PEROM). Its 256K of memory is organized as 32,768 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 200 ns with power dissipation of just 54 mW over the commercial temperature range. When the device is deselected, the CMOS standby current is less than 20 µA.

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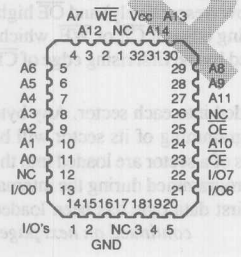
Pin Configurations

Pin Name	Function
A0 - A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

DIP Top View

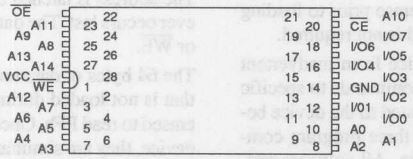


PLCC, LCC Top View



Note: PLCC package pins 1 and 17 are DON'T CONNECT.

TSOP Top View
Type 1



256K (32K x 8) 3-Volt Only CMOS PEROM

Preliminary

3

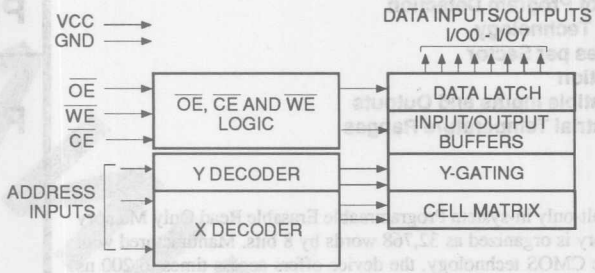
PRELIMINARY

Description (Continued)

To allow for simple in-system reprogrammability, the AT29LV256 does not require high input voltages for programming. Three-volt-only commands determine the operation of the device. Reading data out of the device is similar to reading from an EPROM. Reprogramming the AT29LV256 is performed on a sector basis; 64 bytes of data are loaded into the device and then simultaneously programmed.

During a reprogram cycle, the address locations and 64 bytes of data are captured at microprocessor speed and internally latched, freeing the address and data bus for other operations. Following the initiation of a program cycle, the device will automatically erase the sector and then program the latched data using an internal control timer. The end of a program cycle can be detected by $\overline{\text{DATA}}$ polling of I/O7. Once the end of a program cycle has been detected, a new access for a read or program can begin.

Block Diagram



Device Operation

READ: The AT29LV256 is accessed like an EPROM. When $\overline{\text{CE}}$ and $\overline{\text{OE}}$ are low and $\overline{\text{WE}}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{\text{CE}}$ or $\overline{\text{OE}}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

SOFTWARE DATA PROTECTION PROGRAMMING: The AT29LV256 has 512 individual sectors, each 64 bytes. Using the software data protection feature, byte loads are used to enter the 64 bytes of a sector to be programmed. The AT29LV256 can only be programmed or reprogrammed using the software data protection feature. The device is programmed on a sector basis. If a byte of data within the sector is to be changed, data for the entire 64-byte sector must be loaded into the device. The AT29LV256 automatically does a sector erase prior to loading the data into the sector. An erase command is not required.

Software data protection protects the device from inadvertent programming. A series of three program commands to specific addresses with specific data must be presented to the device before programming may occur. The same three program commands must begin each program operation. All software program commands must obey the sector program timing specifications. Power transitions will not reset the software data protection feature, however the software feature will guard against inadvertent program cycles during power transitions.

Once set, software data protection will remain active unless the disable command sequence is issued.

After setting SDP, any attempt to write to the device without the three-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, a read operation will effectively be a polling operation.

After the software data protection's three-byte command code is given, a byte load is performed by applying a low pulse on the $\overline{\text{WE}}$ or $\overline{\text{CE}}$ input with $\overline{\text{CE}}$ or $\overline{\text{WE}}$ low (respectively) and $\overline{\text{OE}}$ high. The address is latched on the falling edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$, whichever occurs last. The data is latched by the first rising edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$.

The 64 bytes of data must be loaded into each sector. Any byte that is not loaded during the programming of its sector will be erased to read FFh. Once the bytes of a sector are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data byte has been loaded

continued on next page

Device Operation (Continued)

into the device, successive bytes are entered in the same manner. Each new byte to be programmed must have its high to low transition on $\overline{WE}$ (or $\overline{CE}$) within 150 µs of the low to high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding byte. If a high to low transition is not detected within 150 µs of the last low to high transition, the load period will end and the internal programming period will start. A6 to A14 specify the sector address. The sector address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A5 specify the byte address within the sector. The bytes may be loaded in any order; sequential loading is not required.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT29LV256 in the following ways: (a) V_{CC} sense— if V_{CC} is below 1.8 V (typical), the program function is inhibited. (b) V_{CC} power on delay— once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 10 ms (typical) before programming. (c) Program inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (d) Noise filter— pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle.

INPUT LEVELS: While operating with a 3.3 V ±10% power supply, the address inputs and control inputs ($\overline{OE}$, $\overline{CE}$ and $\overline{WE}$) may be driven from 0 to 5.5 V without adversely affecting the operation of the device. The I/O lines can only be driven from 0 to 3.6 volts.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product. In addition, users may wish to use the software product identification mode to identify the part (i.e. using the device code), and have the system software use the appropriate sector size for program operations. In this manner, the user can have a common board design for 256K to 4-megabit densities and, with each density's sector size in a memory map, have the system software apply the appropriate sector size.

For details, see Operating Modes (for hardware operation) or Software Product Identification. The manufacturer and device code is the same for both modes.

$\overline{DATA}$ POLLING: The AT29LV256 features $\overline{DATA}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{DATA}$ polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ polling the AT29LV256 provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

OPTIONAL CHIP ERASE MODES: The entire device may be erased by either using a six-byte software code or high voltage. For details, please contact Atmel.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6 V to +6.25 V
All Output Voltages with Respect to Ground	-0.6 V to V_{CC} +0.6 V
Voltage on A9 (including N.C. Pins) with Respect to Ground	-0.6 V to +13.5 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Note: 1. These parameters are characterized and not 100% tested.

D.C. and A.C. Operating Range

		AT29LV256-20	AT29LV256-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		3.3 V ± 0.3 V	3.3 V ± 0.3 V

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Ai	D_{OUT}
Program[2]	V_{IL}	V_{IH}	V_{IL}	Ai	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	X	High Z
Program Inhibit	X	X	V_{IH}		
Program Inhibit	X	V_{IL}	X		
Output Disable	X	V_{IH}	X		High Z
Product Identification	V_{IL}	V_{IL}	V_{IH}	A1-A14 = V_{IL}, A9 = V_H[3], A0 = V_{IL}	Manufacturer Code[4]
				A1-A14 = V_{IL}, A9 = V_H[3], A0 = V_{IH}	Device Code[4]

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.
3. V_H = 12.0 V ± 0.5 V.
4. Manufacturer Code: 1F, Device Code: BC.

D.C. Characteristics

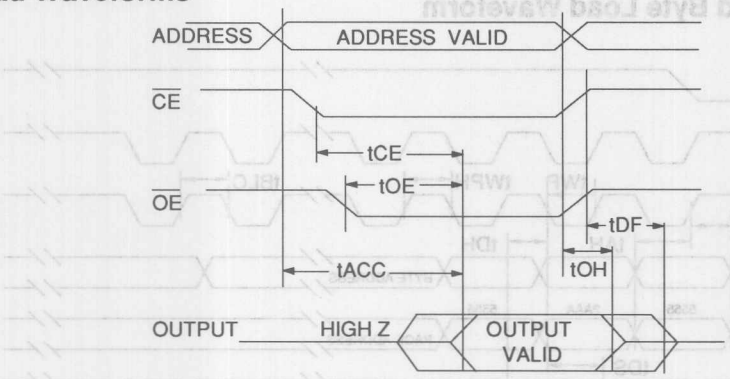
Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}			1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0 V to V_{CC}			1	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3 V to V_{CC}	Com.		20	µA
			Ind.		50	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0 V to V_{CC}			1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6 V			15	mA
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA; V_{CC} = 3.0 V			.45	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA; V_{CC} = 3.0 V		2.4		V

A.C. Read Characteristics

Symbol	Parameter	AT29LV256-20 Min	AT29LV256-20 Max	AT29LV256-25 Min	AT29LV256-25 Max	Units
t_{ACC}	Address to Output Delay		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	100	0	120	ns
t_{DF} (3,4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	55	0	80	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		ns

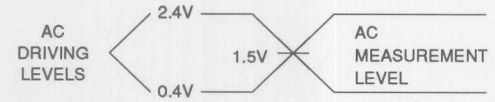
3

A.C. Read Waveforms



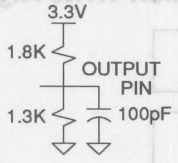
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

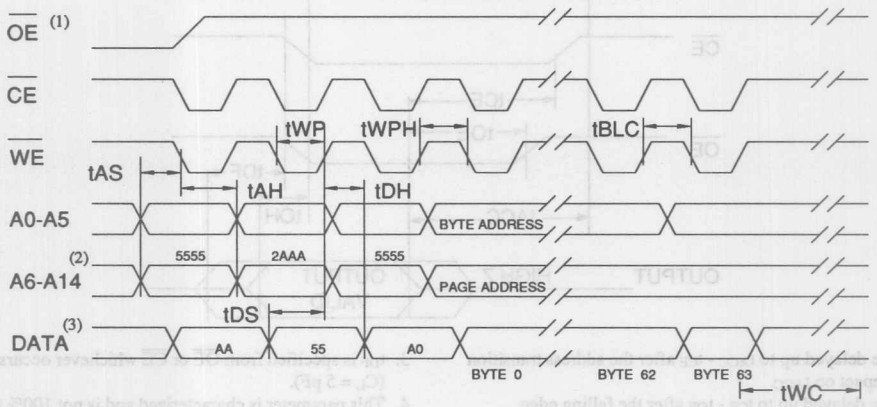
Output Test Load



Program Cycle Characteristics

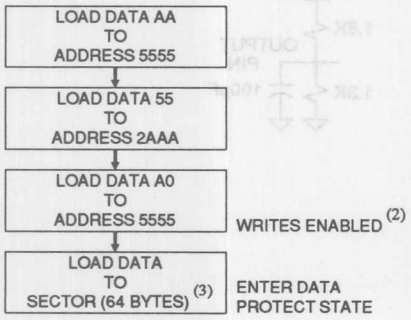
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		20	ms
t_{AS}	Address Set-up Time	10		ns
t_{AH}	Address Hold Time	100		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}	Data Hold Time	10		ns
t_{WP}	Write Pulse Width	200		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	200		ns

Software Protected Byte Load Waveform



Notes:
1. $\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
2. A6 through A14 must specify the sector address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
3. **All bytes that are not loaded within the sector being programmed will be erased to FF.**

Software Data Protection Write Algorithm (1)



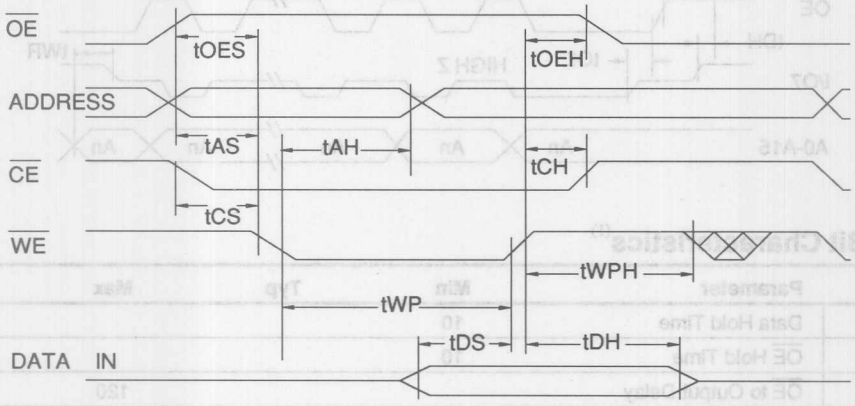
Notes for software program code:
1. Data Format: I/O7–I/O0 (Hex);
   Address Format: A14–A0 (Hex).
2. Data Protect state will be re-activated at end of program cycle.
3. 64 bytes of data MUST BE loaded.

A.C. Byte Load Characteristics

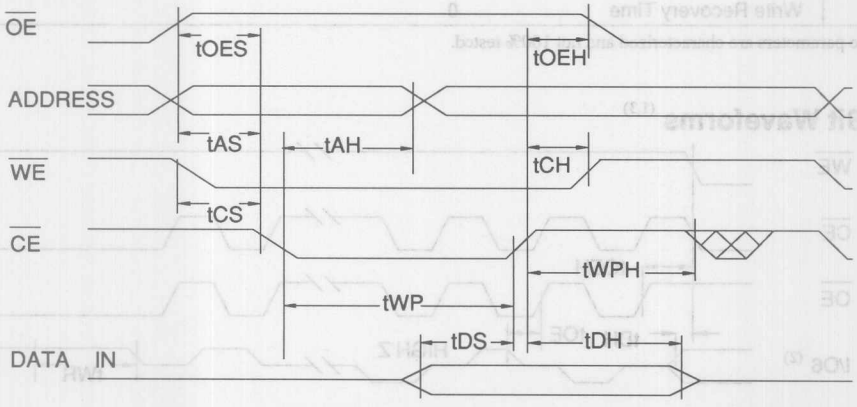
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	10		ns
t_{AH}	Address Hold Time	100		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	200		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time	10		ns
t_{WC}	Write Cycle Time		20	ms

A.C. Byte Load Waveforms During Software Protection [1,2]

$\overline{WE}$ Controlled



$\overline{CE}$ Controlled



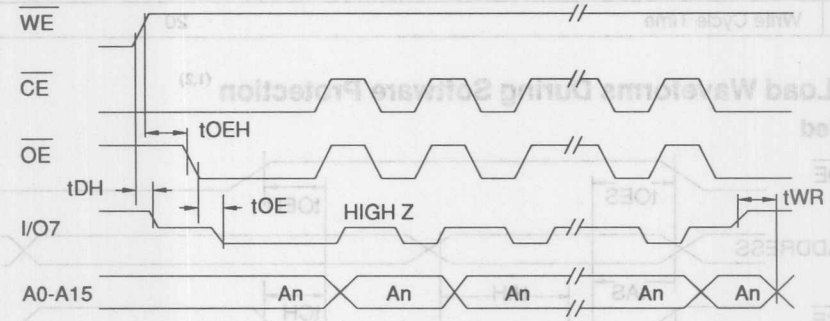
Notes:
1. The software data protection commands must be applied prior to byte loads.
2. A complete sector (64 bytes) should be loaded using these waveforms as shown in the Software Protected Byte Load waveforms (see previous page).

$\overline{\text{Data}}$ Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			120	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{Data}}$ Polling Waveforms

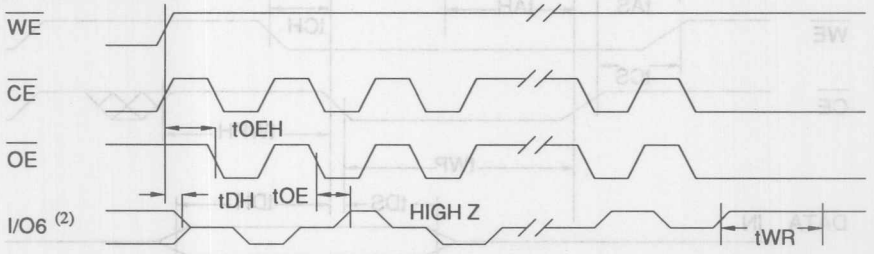


Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			120	ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

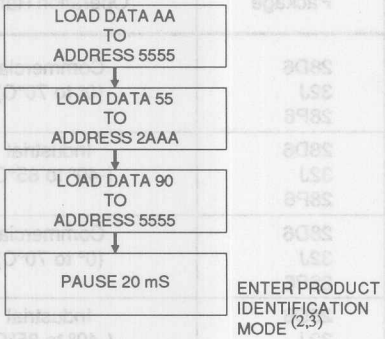
Note: 1. These parameters are characterized and not 100% tested.

Toggle Bit Waveforms [1,3]

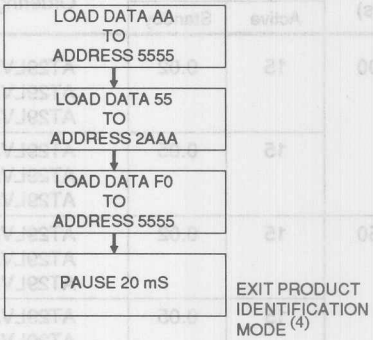


Notes:
1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry [1]



Software Product Identification Exit [1]



Notes for software product identification:

1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. A1 - A14 = V_{IL}.
   Manufacture Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
200	15	0.02	AT29LV256-20DC AT29LV256-20JC AT29LV256-20PC	28D6 32J 28P6	Commercial (0° to 70°C)
	15	0.05	AT29LV256-20DI AT29LV256-20JI AT29LV256-20PI	28D6 32J 28P6	Industrial (-40° to 85°C)
250	15	0.02	AT29LV256-25DC AT29LV256-25JC AT29LV256-25PC	28D6 32J 28P6	Commercial (0° to 70°C)
	15	0.05	AT29LV256-25DI AT29LV256-25JI AT29LV256-25PI	28D6 32J 28P6	Industrial (-40° to 85°C)

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
200	15	0.02	AT29LV256-20TC	28T	Commercial (0° to 70°C)
250	15	0.02	AT29LV256-25TC	28T	Commercial (0° to 70°C)

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28T	28 Lead, Thin Small Outline Package (TSOP)

256K (32K x 8) 5-Volt Only CMOS PEROM

Features

- Fast Read Access Time - 90 ns
- Five-Volt-Only Reprogramming
- Page Program Operation
  - Single Cycle Reprogram (Erase and Program)
  - Internal Address and Data Latches for 64 Bytes
- Fast Program Cycle Times
  - Page (64 Byte) Program Time - 10 ms
  - Chip Erase Time - 10 ms
- Internal Program Control Timer
- Low Power Dissipation
  - 80 mA Active Current
  - 300 µA CMOS Standby Current
- Hardware and Software Data Protection
- DATA Polling for End of Program Detection
- High Reliability CMOS Technology
  - 1000 Erase/Program Cycles
  - 10 Year Data Retention
- Single 5 V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- Full Military, Commercial, and Industrial Temperature Ranges
- Pin-Compatible with 29C010 and 29C512 for Easy System Upgrades

Description

The AT29C257 is a five-volt-only in-system Programmable and Erasable Read Only Memory (PEROM). Its 256K of memory is organized as 32,768 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 90 ns with power dissipation of just 440 mW. When the device is deselected, the CMOS standby current is less than 300 µA.

To allow for simple in-system reprogrammability, the AT29C257 does not require high input voltages for programming. Five-volt-only commands determine the operation of the device. Reading data out of the device is similar to reading from a static RAM. Reprogramming the AT29C257 is performed on a page basis; 64 bytes of data are loaded into the device and then simultaneously programmed. The contents of the entire device may be erased by using a six-byte software code (although erasure before programming is not needed).

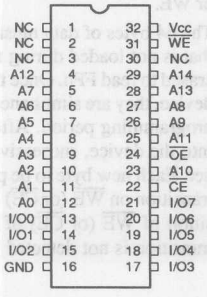
During a reprogram cycle, the address locations and 64 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a program cycle, the device will automatically erase the page and then program the latched data using an internal control timer. The end of a program cycle can be detected by $\overline{\text{DATA}}$ polling of I/O7. Once the end of a program cycle has been detected a new access for a read, program or chip erase can begin.

Pin Configurations

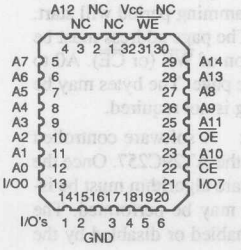
Pin Name	Function
A0 - A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

Notes:
1. PLCC package pin 30 is a DON'T CONNECT.
2. To upgrade to the 1-Mbit 29C010, pin 3 is A15 and pin 2 is A16.

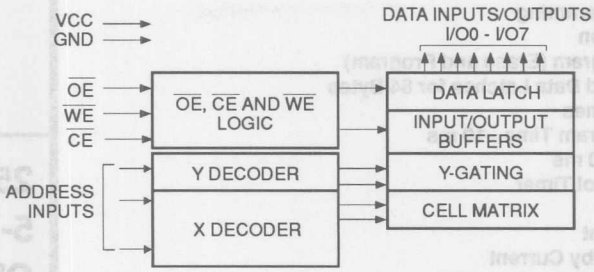
DIP Top View



PLCC and LCC Top View



Block Diagram



Device Operation

READ: The AT29C257 is accessed like a static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

BYTE LOAD: A byte load is performed by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Byte loads are used to enter the 64 bytes of a page to be programmed or the software codes for data protection and chip erasure.

PROGRAM: The device is reprogrammed on a page basis. If a byte of data within a page is to be changed, data for the entire page must be loaded into the device. Any byte that is not loaded during the programming of its page will be erased to read FFh. Once the bytes of a page are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data byte has been loaded into the device, successive bytes are entered in the same manner. Each new byte to be programmed must have its high to low transition on $\overline{WE}$ (or $\overline{CE}$) within 150 µs of the low to high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding byte. If a high to low transition is not detected within 150 µs of the last low to high transition, the load period will end and the internal programming period will start. A6 to A14 specify the page address. The page address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A5 specify the byte address within the page. The bytes may be loaded in any order; sequential loading is not required.

SOFTWARE DATA PROTECTION: A software controlled data protection feature is available on the AT29C257. Once the software protection is enabled a software algorithm must be issued to the device before a program may be performed. The software protection feature may be enabled or disabled by the user; when shipped from Atmel, the software data protection feature is disabled. To enable the software data protection, a series of three program commands to specific addresses with specific data must be performed. After the software data protection is enabled the same three program commands must begin each program cycle in order for the programs to occur. All software program commands must obey the page program timing specifications. Once set, the software data protection feature remains active unless its disable command is issued. Power transitions will not reset the software data protection feature, however the software feature will guard against inadvertent program cycles during power transitions.

Once set, software data protection will remain active unless the disable command sequence is issued.

After setting SDP, any attempt to write to the device without the three-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, a read operation will effectively be a polling operation.

After the software data protection's three-byte command code is given, a byte load is performed by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$.

The 64 bytes of data must be loaded into each sector. Any byte that is not loaded during the programming of its sector will be erased to read FFh. Once the bytes of a sector are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data byte has been loaded into the device, successive bytes are entered in the same manner. Each new byte to be programmed must have its high to low transition on $\overline{WE}$ (or $\overline{CE}$) within 150 µs of the low to high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding byte. If a high to low transition is not detected within 150 µs of the last low to high

continued on next page

Device Operation (Continued)

transition, the load period will end and the internal programming period will start. A6 to A14 specify the sector address. The sector address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A5 specify the byte address within the sector. The bytes may be loaded in any order; sequential loading is not required.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT29C257 in the following ways: (a) V_{CC} sense— if V_{CC} is below 3.8 V (typical), the program function is inhibited. (b) V_{CC} power on delay— once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 5 ms (typical) before programming. (c) Program inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (d) Noise filter— pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer and may be accessed by a hardware or software operation. For details, see Operating Modes or Software Product Identification.

$\overline{DATA}$ POLLING: The AT29C257 features $\overline{DATA}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{DATA}$ polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ polling the AT29C257 provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

OPTIONAL CHIP ERASE MODES: The entire device may be erased by either using a six-byte software code or high voltage. For details, please contact Atmel.

3

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6 V to +6.25 V
All Output Voltages with Respect to Ground	-0.6 V to V_{CC} +0.6 V
Voltage on $\overline{OE}$ with Respect to Ground	-0.6 V to +13.5 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Note: 1. This parameter is characterized and is not 100% tested.

D.C. and A.C. Operating Range

		AT29C257-90	AT29C257-12	AT29C257-15	AT29C257-20	AT29C257-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.		-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5 V ± 10%	5 V ± 10%	5 V ± 10%	5 V ± 10%	5 V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Ai	D_{OUT}
Program[2]	V_{IL}	V_{IH}	V_{IL}	Ai	D_{IN}
5V Chip Erase	V_{IL}	V_{IH}	V_{IL}	Ai	
Standby/Write Inhibit	V_{IH}	X[1]	X	X	High Z
Write Inhibit	X	X	V_{IH}		
Write Inhibit	X	V_{IL}	X		
Output Disable	X	V_{IH}	X		High Z
High Voltage Chip Erase	V_{IL}	V_H [3]	V_{IL}	X	High Z
Product Identification	V_{IL}	V_{IL}	V_{IH}	A1-A14 = V_{IL}, A9 = V_H, A0 = V_{IL}	Manufacturer Code[4]
				A1-A14 = V_{IL}, A9 = V_H, A0 = V_{IH}	Device Code[4]

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.
3. V_H = 12.0 V ± 0.5 V.
4. Manufacturer Code: 1F, Device Code: DC

D.C. Characteristics

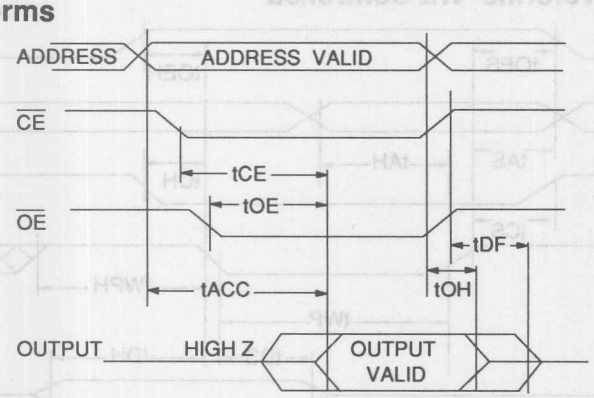
Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0 V to V_{CC}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC}-0.3V to V_{CC}		300	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0 V to V_{CC}		3	mA
I_{CC}	V_{CC} Active Current	f= 5 MHz; I_{OUT} = 0 mA		50	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA	2.4		V
V_{OH2}	Output High Voltage CMOS	I_{OH} = -100 µA; V_{CC} = 4.5V	4.2		V

A.C. Read Characteristics

Symbol	Parameter	AT29C257-90 Min	AT29C257-90 Max	AT29C257-12 Min	AT29C257-12 Max	AT29C257-15 Min	AT29C257-15 Max	AT29C257-20 Min	AT29C257-20 Max	AT29C257-25 Min	AT29C257-25 Max	Units
t_{ACC}	Address to Output Delay		90		120		150		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		90		120		150		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	40	0	50	0	70	0	80	0	100	ns
t_{DF} (3,4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	40	0	40	0	50	0	55	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		0		ns

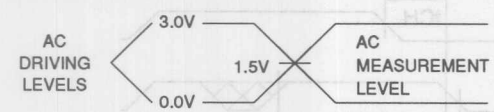
3

A.C. Read Waveforms



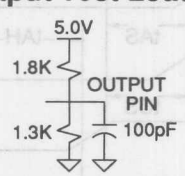
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

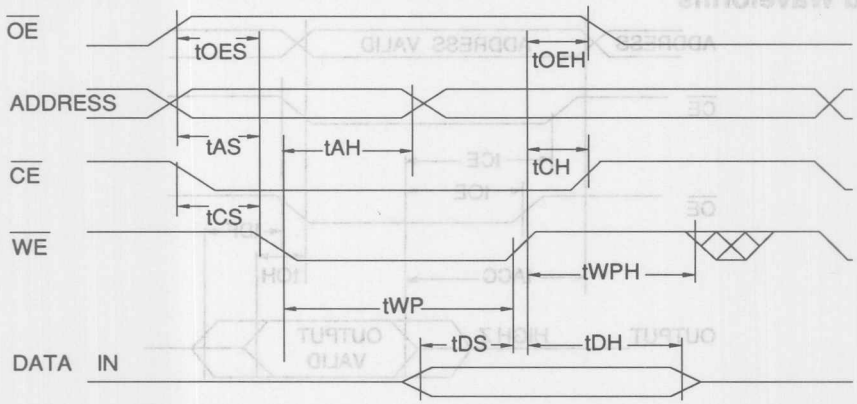
Output Test Load



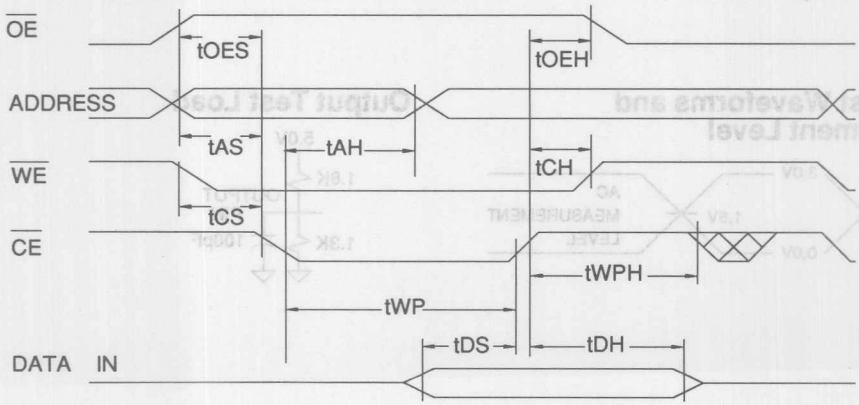
A.C. Byte Load Characteristics

Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	90		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{WC}	Write Cycle Time		10	ms

A.C. Byte Load Waveforms- $\overline{WE}$ Controlled



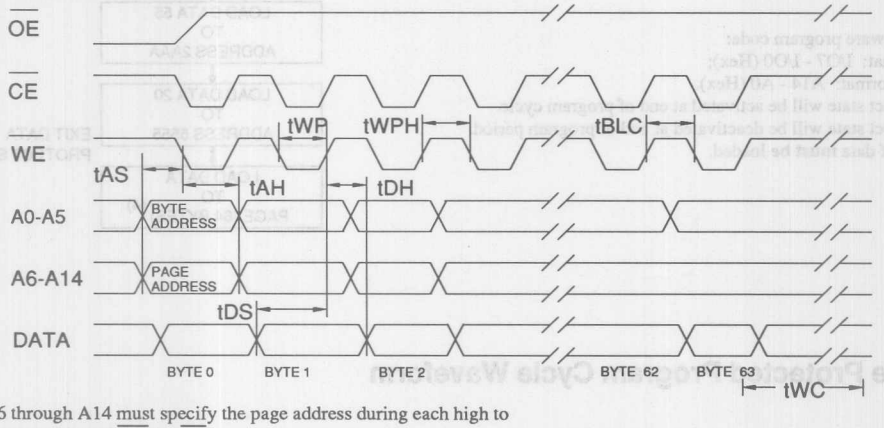
A.C. Byte Load Waveforms- $\overline{CE}$ Controlled



Program Cycle Characteristics

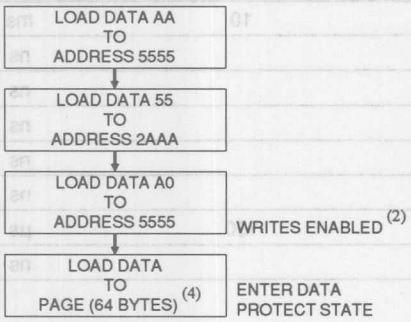
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	120		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	100		ns

Program Cycle Waveforms

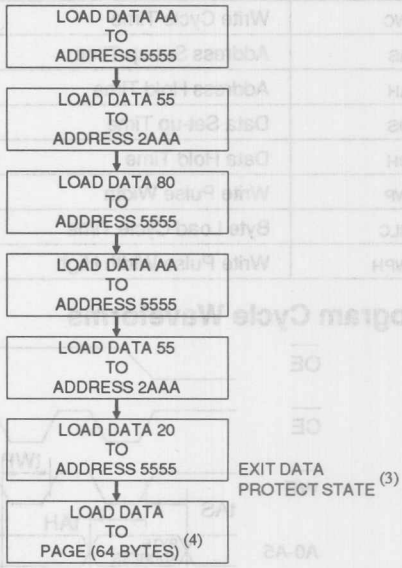


Notes: A6 through A14 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
All bytes that are not loaded within the page being programmed will be erased to FF.

Software Data Protection Enable Algorithm [1]

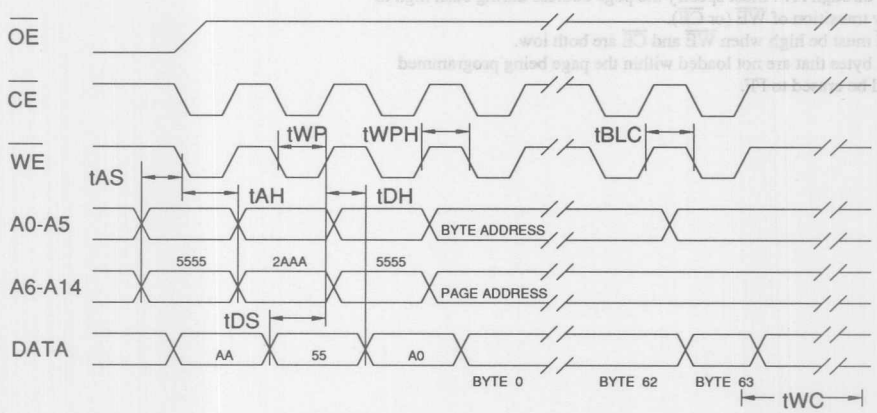


Software Data Protection Disable Algorithm [1]



Notes for software program code:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Data Protect state will be activated at end of program cycle.
3. Data Protect state will be deactivated at end of program period.
4. 64 bytes of data **must be** loaded.

Software Protected Program Cycle Waveform



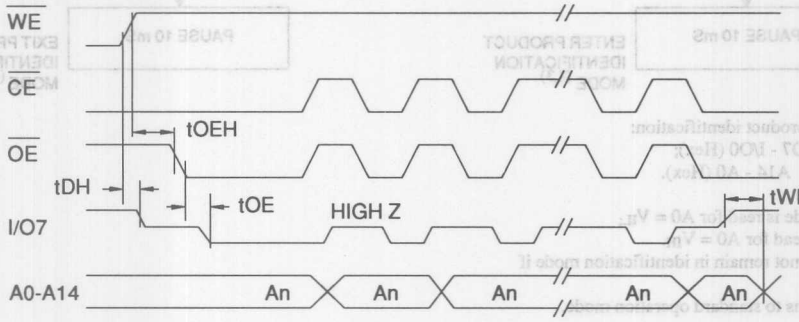
Notes: 1. A6 through A14 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
2. $\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
3. **All bytes that are not loaded within the page being programmed will be erased to FF.**

$\overline{\text{Data}}$ Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{Data}}$ Polling Waveforms

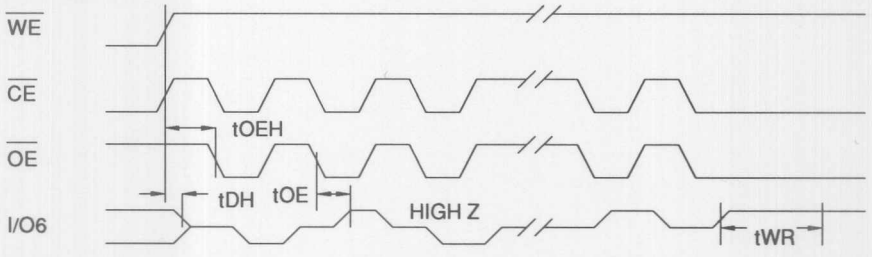


Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

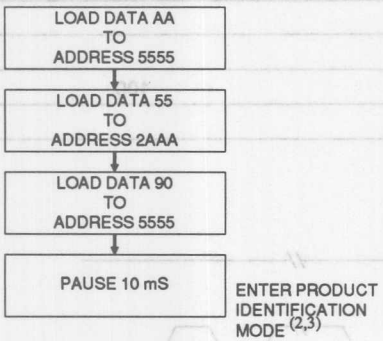
Note: 1. These parameters are characterized and not 100% tested.

Toggle Bit Waveforms

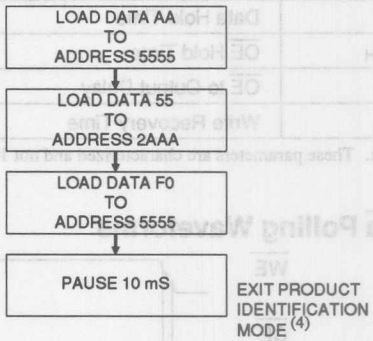


Notes:
1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry [1]



Software Product Identification Exit [1]

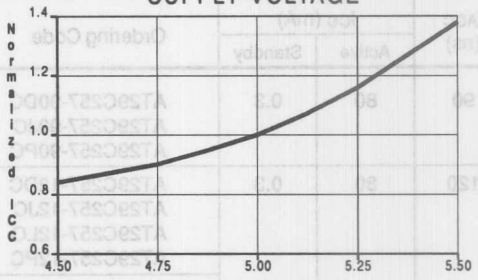


Notes for software product identification:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. A1 - A14 = V_{IL}.
   Manufacture Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.

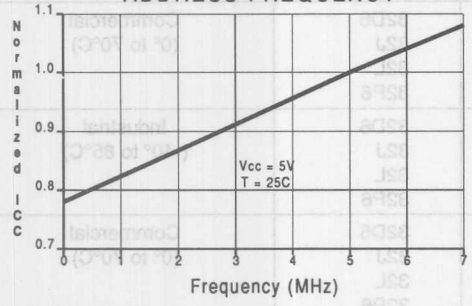
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	80	0.3	AT29C257-90DC AT29C257-90JC AT29C257-90PC	32D6 32J 32P6	Commercial (0° to 70°C)
120	80	0.3	AT29C257-12DC AT29C257-12JC AT29C257-12LC AT29C257-12PC	32D6 32J 32L 32P6	Commercial (0° to 70°C)
			AT29C257-12DI AT29C257-12JI AT29C257-12LI AT29C257-12PI	32D6 32J 32L 32P6	Industrial (-40° to 85°C)
150	80	0.3	AT29C257-15DC AT29C257-15JC AT29C257-15LC AT29C257-15PC	32D6 32J 32L 32P6	Commercial (0° to 70°C)
			AT29C257-15DI AT29C257-15JI AT29C257-15LI AT29C257-15PI	32D6 32J 32L 32P6	Industrial (-40° to 85°C)
200	80	0.3	AT29C257-20DC AT29C257-20JC AT29C257-20LC AT29C257-20PC	32D6 32J 32L 32P6	Commercial (0° to 70°C)
			AT29C257-20DI AT29C257-20JI AT29C257-20LI AT29C257-20PI	32D6 32J 32L 32P6	Industrial (-40° to 85°C)
250	80	0.3	AT29C257-25DC AT29C257-25JC AT29C257-25LC AT29C257-25PC	32D6 32J 32L 32P6	Commercial (0° to 70°C)
250	80	0.3	AT29C257-25DI AT29C257-25JI AT29C257-25LI AT29C257-25PI	32D6 32J 32L 32P6	Industrial (-40° to 85°C)

Package Type	
32D6	32 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)

512K (64K x 8) 5-Volt Only CMOS PEROM

Features

- **Fast Read Access Time - 90 ns**
- **Five-Volt-Only Reprogramming**
- **Sector Program Operation**
  - **Single Cycle Reprogram (Erase and Program)**
  - **512 Sectors (128 bytes/sector)**
  - **Internal Address and Data Latches for 128 Bytes**
- **Fast Sector Program Cycle Time - 10 ms**
- **Internal Program Control and Timer**
- **Low Power Dissipation**
  - **50 mA Active Current**
  - **100 µA CMOS Standby Current**
- **Hardware and Software Data Protection**
- **DATA Polling for End of Program Detection**
- **High Reliability CMOS Technology**
  - **1000 Program Cycles per Sector**
  - **10-Year Data Retention**
- **Single 5 V ±10% Supply**
- **CMOS and TTL Compatible Inputs and Outputs**
- **Full Military, Commercial, and Industrial Temperature Ranges**

Description

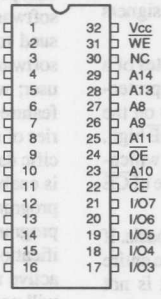
The AT29C512 is a five-volt-only in-system Programmable and Erasable Read Only Memory (PEROM). Its 512K of memory is organized as 65,536 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 90 ns with power dissipation of just 275 mW over the commercial temperature range. When the device is deselected, the CMOS standby current is less than 100 µA.

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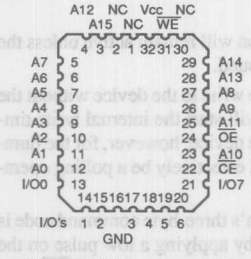
Pin Configurations

Pin Name	Function
A0 - A15	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

DIP Top View



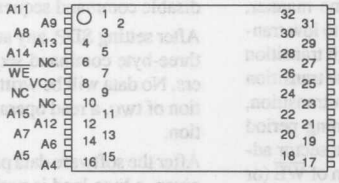
PLCC and LCC Top View



Note: PLCC package pin 30 is a DON'T CONNECT.

TSOP Top View

Type 1

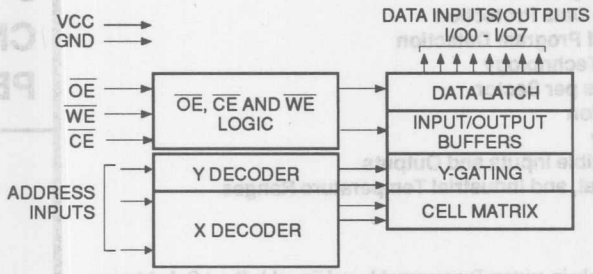


Description (Continued)

To allow for simple in-system reprogrammability, the AT29C512 does not require high input voltages for programming. Five-volt-only commands determine the operation of the device. Reading data out of the device is similar to reading from an EPROM. Reprogramming the AT29C512 is performed on a sector basis; 128 bytes of data are loaded into the device and then simultaneously programmed.

During a reprogram cycle, the address locations and 128 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a program cycle, the device will automatically erase the sector and then program the latched data using an internal control timer. The end of a program cycle can be detected by $\overline{\text{DATA}}$ polling of I/O7. Once the end of a program cycle has been detected, a new access for a read or program can begin.

Block Diagram



Device Operation

READ: The AT29C512 is accessed like an EPROM. When $\overline{\text{CE}}$ and $\overline{\text{OE}}$ are low and $\overline{\text{WE}}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{\text{CE}}$ or $\overline{\text{OE}}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

BYTE LOAD: Byte loads are used to enter the 128 bytes of a sector to be programmed or the software codes for data protection. A byte load is performed by applying a low pulse on the $\overline{\text{WE}}$ or $\overline{\text{CE}}$ input with $\overline{\text{CE}}$ or $\overline{\text{WE}}$ low (respectively) and $\overline{\text{OE}}$ high. The address is latched on the falling edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$, whichever occurs last. The data is latched by the first rising edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$.

PROGRAM: The device is reprogrammed on a sector basis. If a byte of data within a sector is to be changed, data for the entire sector must be loaded into the device. Any byte that is not loaded during the programming of its sector will be erased to read FFh. Once the bytes of a sector are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data byte has been loaded into the device, successive bytes are entered in the same manner. Each new byte to be programmed must have its high to low transition on $\overline{\text{WE}}$ (or $\overline{\text{CE}}$) within 150 µs of the low to high transition of $\overline{\text{WE}}$ (or $\overline{\text{CE}}$) of the preceding byte. If a high to low transition is not detected within 150 µs of the last low to high transition, the load period will end and the internal programming period will start. A7 to A15 specify the sector address. The sector address must be valid during each high to low transition of $\overline{\text{WE}}$ (or $\overline{\text{CE}}$). A0 to A6 specify the byte address within the sector. The bytes may be loaded in any order; sequential loading is not required.

SOFTWARE DATA PROTECTION: A software controlled data protection feature is available on the AT29C512. Once the software protection is enabled a software algorithm must be issued to the device before a program may be performed. The software protection feature may be enabled or disabled by the user; when shipped from Atmel, the software data protection feature is disabled. To enable the software data protection, a series of three program commands to specific addresses with specific data must be performed. After the software data protection is enabled the same three program commands must begin each program cycle in order for the programs to occur. All software program commands must obey the sector program timing specifications. Once set, the software data protection feature remains active unless its disable command is issued. Power transitions will not reset the software data protection feature, however the software feature will guard against inadvertent program cycles during power transitions.

Once set, software data protection will remain active unless the disable command sequence is issued.

After setting SDP, any attempt to write to the device without the three-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, a read operation will effectively be a polling operation.

After the software data protection's three-byte command code is given, a byte load is performed by applying a low pulse on the $\overline{\text{WE}}$ or $\overline{\text{CE}}$ input with $\overline{\text{CE}}$ or $\overline{\text{WE}}$ low (respectively) and $\overline{\text{OE}}$ high.

continued on next page

Device Operation (Continued)

The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$.

The 128 bytes of data must be loaded into each sector. Any byte that is not loaded during the programming of its sector will be erased to read FFh. Once the bytes of a sector are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data byte has been loaded into the device, successive bytes are entered in the same manner. Each new byte to be programmed must have its high to low transition on $\overline{WE}$ (or $\overline{CE}$) within 150 µs of the low to high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding byte. If a high to low transition is not detected within 150 µs of the last low to high transition, the load period will end and the internal programming period will start. A7 to A15 specify the sector address. The sector address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A6 specify the byte address within the sector. The bytes may be loaded in any order; sequential loading is not required.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT29C512 in the following ways: (a) V_{CC} sense— if V_{CC} is below 3.8 V (typical), the program function is inhibited. (b) V_{CC} power on delay— once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 5 ms (typical) before programming. (c) Program inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (d) Noise filter— pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product. In addition, users may wish to use the software product identification mode to identify the part (i.e. using the device code), and have the system software use the appropriate sector size for program operations. In this manner, the user can have a common board design for 256K to 4-megabit densities and, with each density's sector size in a memory map, have the system software apply the appropriate sector size.

For details, see Operating Modes (for hardware operation) or Software Product Identification. The manufacturer and device code is the same for both modes.

$\overline{DATA}$ POLLING: The AT29C512 features $\overline{DATA}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{DATA}$ polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ polling the AT29C512 provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

OPTIONAL CHIP ERASE MODES: The entire device may be erased by either using a six-byte software code or high voltage. For details, please contact Atmel.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6 V to +6.25 V
All Output Voltages with Respect to Ground	-0.6 V to V_{CC} +0.6 V
Voltage on $\overline{OE}$ with Respect to Ground	-0.6 V to +13.5 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Notes: 1. This parameter is characterized and is not 100% tested.

D.C. and A.C. Operating Range

		AT29C512-90	AT29C512-12	AT29C512-15	AT29C512-20
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 10%	5 V ± 10%	5 V ± 10%	5 V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	AI	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Ai	D_{OUT}
Program[2]	V_{IL}	V_{IH}	V_{IL}	Ai	D_{IN}
5V Chip Erase	V_{IL}	V_{IH}	V_{IL}	Ai	
Standby/Write Inhibit	V_{IH}	X[1]	X	X	High Z
Program Inhibit	X	X	V_{IH}		
Program Inhibit	X	V_{IL}	X		
Output Disable	X	V_{IH}	X		High Z
Product Identification	V_{IL}	V_{IL}	V_{IH}	A1-A15 = V_{IL}, A9 = V_H,[3] A0 = V_{IL}	Manufacturer Code[4]
				A1-A15 = V_{IL}, A9 = V_H,[3] A0 = V_{IH}	Device Code[4]

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.
3. V_H = 12.0 V ± 0.5 V
4. Manufacturer Code: 1F, Device Code: 5D

D.C. Characteristics

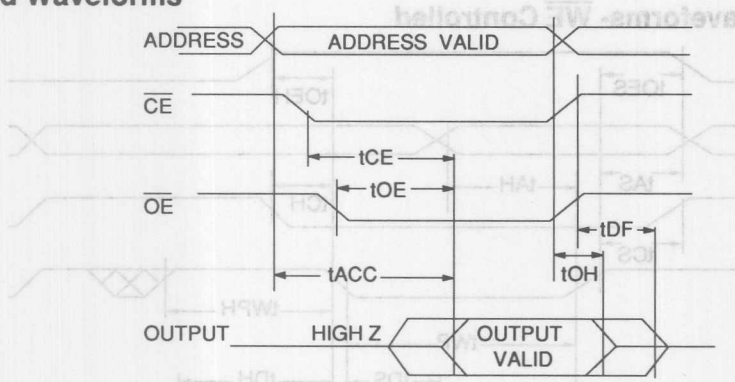
Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0 V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3 V to V_{CC}	Com.		100	µA
			Ind., Mil.		300	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0 V to V_{CC}			3	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA			50	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA		2.4		V
V_{OH2}	Output High Voltage CMOS	I_{OH} = -100 µA; V_{CC} = 4.5 V		4.2		V

A.C. Read Characteristics

Symbol	Parameter	AT29C512-90		AT29C512-12		AT29C512-15		AT29C512-20		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		90		120		150		200	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		90		120		150		200	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	40	0	50	0	70	0	80	ns
t_{DF} (3,4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	40	0	40	0	50	0	55	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		ns

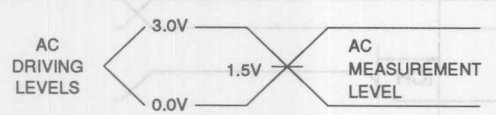
3

A.C. Read Waveforms



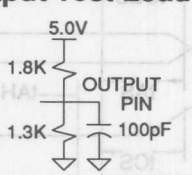
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

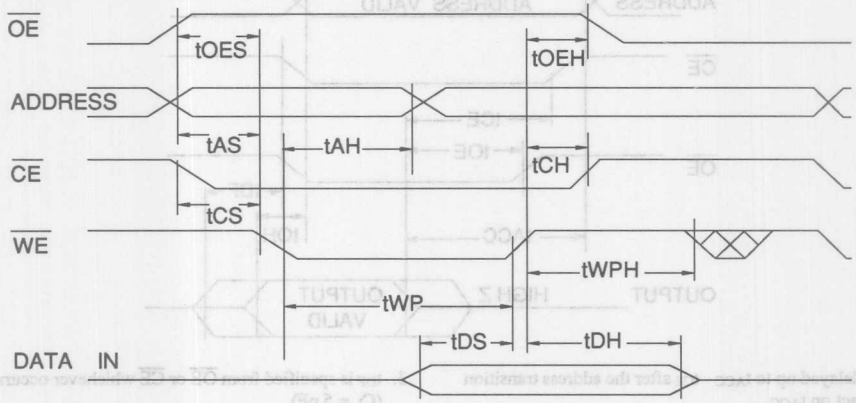
Output Test Load



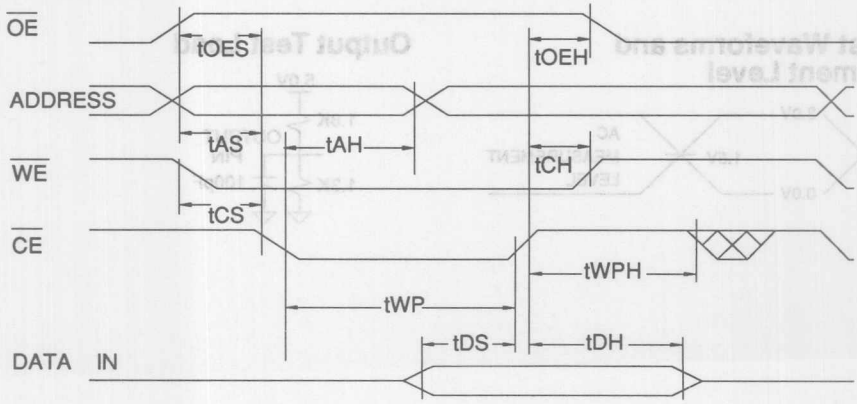
A.C. Byte Load Characteristics

Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	90		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{WC}	Write Cycle Time		10	ms

A.C. Byte Load Waveforms- $\overline{WE}$ Controlled



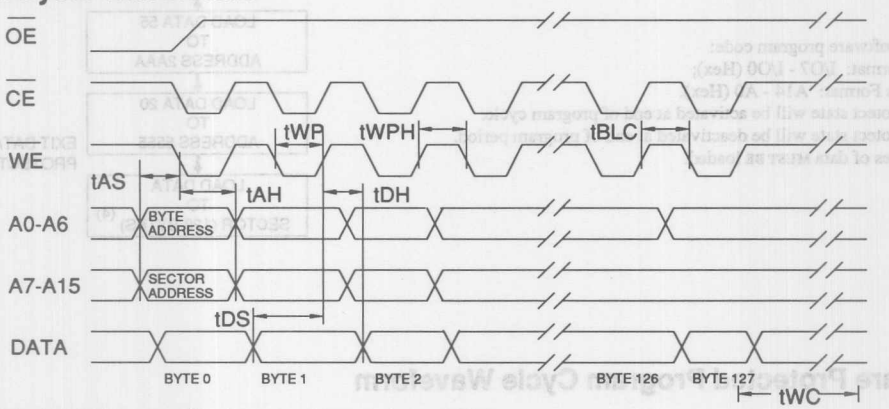
A.C. Byte Load Waveforms- $\overline{CE}$ Controlled



Program Cycle Characteristics

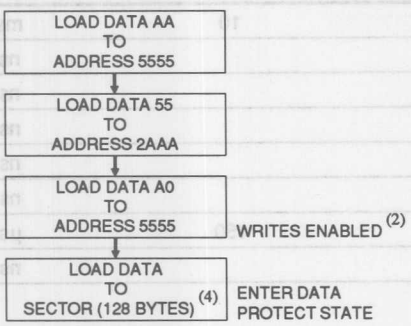
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	90		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	100		ns

Program Cycle Waveforms

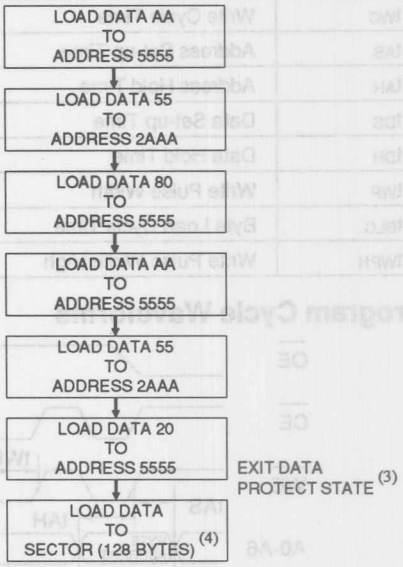


Notes: A7 through A15 must specify the sector address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
All bytes that are not loaded within the sector being programmed will be erased to FF.

Software Data Protection Enable Algorithm (1)

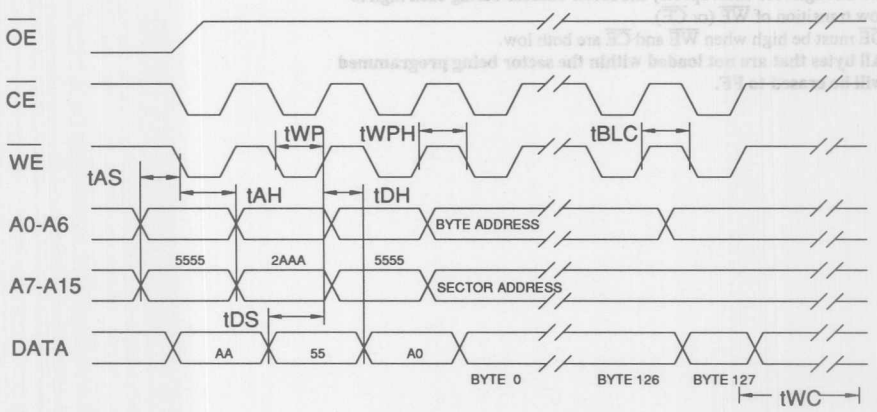


Software Data Protection Disable Algorithm (1)



Notes for software program code:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Data Protect state will be activated at end of program cycle.
3. Data Protect state will be deactivated at end of program period.
4. 128 bytes of data MUST BE loaded.

Software Protected Program Cycle Waveform



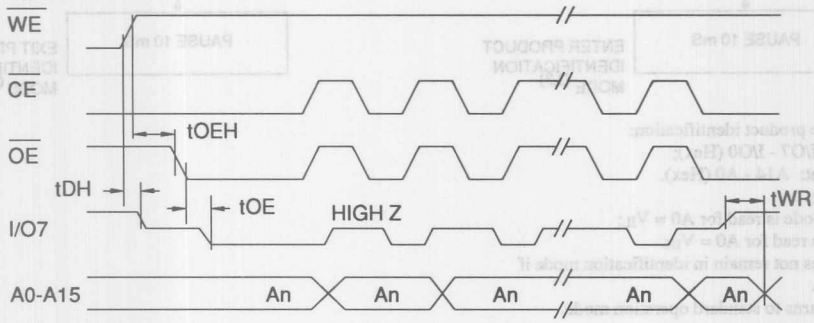
Notes: A7 through A15 must specify the sector address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
$\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
All bytes that are not loaded within the sector being programmed will be erased to FF.

$\overline{\text{Data}}$ Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{Data}}$ Polling Waveforms

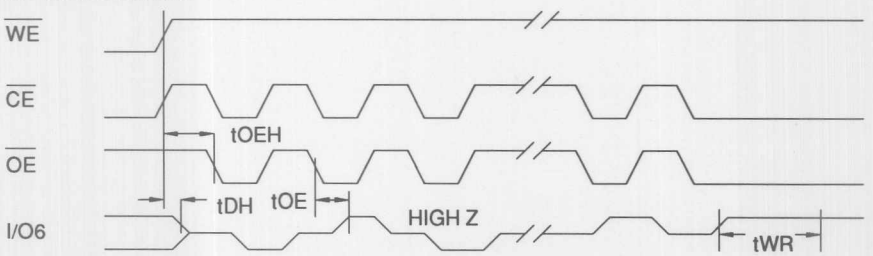


Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

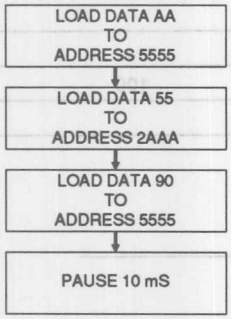
Note: 1. These parameters are characterized and not 100% tested.

Toggle Bit Waveforms



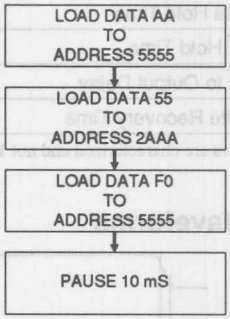
Notes:
1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry [1]



ENTER PRODUCT IDENTIFICATION MODE [2,3]

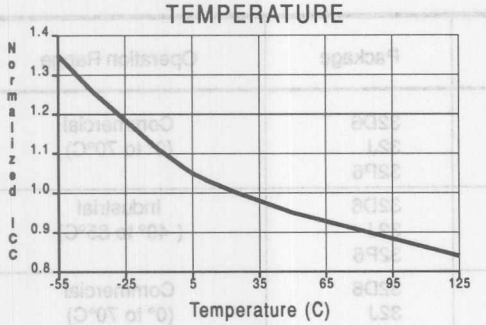
Software Product Identification Exit [1]



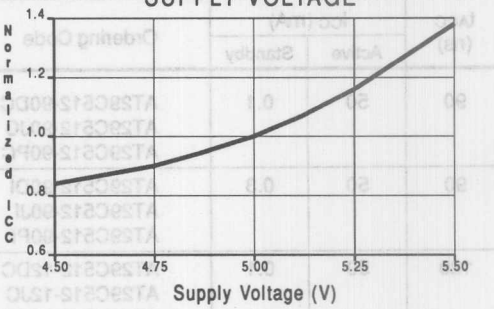
EXIT PRODUCT IDENTIFICATION MODE [4]

Notes for software product identification:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. A1 - A15 = V_{IL}.
   Manufacture Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.

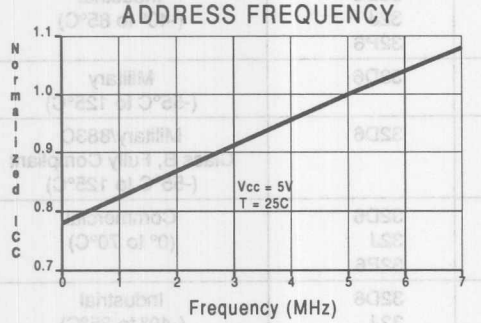
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	50	0.1	AT29C512-90DC AT29C512-90JC AT29C512-90PC	32D6 32J 32P6	Commercial (0° to 70°C)
90	50	0.3	AT29C512-90DI AT29C512-90JI AT29C512-90PI	32D6 32J 32P6	Industrial (-40° to 85°C)
120	50	0.1	AT29C512-12DC AT29C512-12JC AT29C512-12PC	32D6 32J 32P6	Commercial (0° to 70°C)
120	50	0.3	AT29C512-12DI AT29C512-12JI AT29C512-12PI	32D6 32J 32P6	Industrial (-40° to 85°C)
			AT29C512-12DM	32D6	Military (-55°C to 125°C)
			AT29C512-12DM/883	32D6	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	50	0.1	AT29C512-15DC AT29C512-15JC AT29C512-15PC	32D6 32J 32P6	Commercial (0° to 70°C)
150	50	0.3	AT29C512-15DI AT29C512-15JI AT29C512-15PI	32D6 32J 32P6	Industrial (-40° to 85°C)
			AT29C512-15DM	32D6	Military (-55°C to 125°C)
			AT29C512-15DM/883	32D6	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	50	0.1	AT29C512-20DC AT29C512-20JC AT29C512-20PC	32D6 32J 32P6	Commercial (0° to 70°C)
200	50	0.3	AT29C512-20DI AT29C512-20JI AT29C512-20PI	32D6 32J 32P6	Industrial (-40° to 85°C)
			AT29C512-20DM	32D6	Military (-55°C to 125°C)
			AT29C512-20DM/883	32D6	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	50	0.1	AT29C512-12TC	32T	Commercial (0° to 70°C)
150	50	0.1	AT29C512-15TC	32T	Commercial (0° to 70°C)

Package Type	
32D6	32 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
32T	32 Lead, Thin Small Outline Package (TSOP)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	50	0.1	AT29C512-12TC	32T	Commercial (0° to 70°C)
150	50	0.1	AT29C512-15TC	32T	Commercial (0° to 70°C)

Package Type	
32DB	32 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
32T	32 Lead, Thin Small Outline Package (TSOP)

512K (64K x 8) 3-Volt Only CMOS PEROM

Features

- **Single 3.3 V ± 10% Supply**
- **Three-Volt-Only Read and Write Operation**
- **Software Protected Programming**
- **Low Power Dissipation**
  - **15 mA Active Current**
  - **20 µA CMOS Standby Current**
- **Fast Read Access Time - 200 ns**
- **Sector Program Operation**
  - **Single Cycle Reprogram (Erase and Program)**
  - **512 Sectors (128 bytes/sector)**
  - **Internal Address and Data Latches for 128 Bytes**
- **Fast Sector Program Cycle Time - 20 ms Max.**
- **Internal Program Control and Timer**
- **DATA Polling for End of Program Detection**
- **High Reliability CMOS Technology**
  - **1000 Program Cycles per Sector**
  - **10-Year Data Retention**
- **CMOS and TTL Compatible Inputs and Outputs**
- **Commercial and Industrial Temperature Ranges**

Description

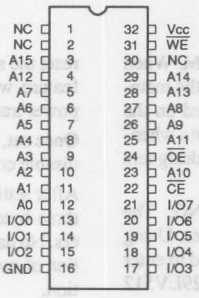
The AT29LV512 is a three-volt-only in-system Programmable Erasable Read Only Memory (PEROM). Its 512K of memory is organized as 65,536 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 200 ns with power dissipation of just 54 mW over the commercial temperature range. When the device is deselected, the CMOS standby current is less than 20 µA.

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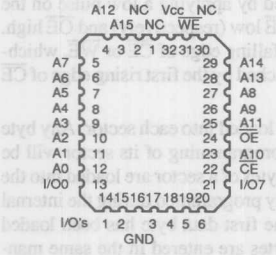
Pin Configurations

Pin Name	Function
A0 - A15	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

DIP Top View

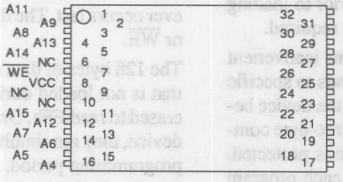


PLCC, LCC Top View



Note: PLCC package pin 30 is a DON'T CONNECT.

TSOP Top View
Type 1

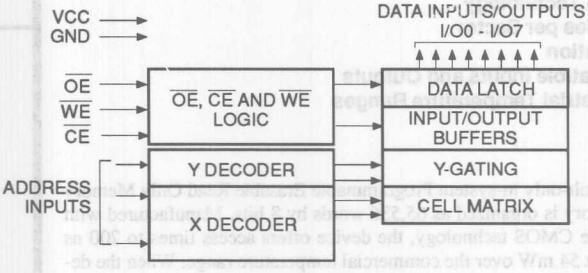


Description (Continued)

To allow for simple in-system reprogrammability, the AT29LV512 does not require high input voltages for programming. Three-volt-only commands determine the operation of the device. Reading data out of the device is similar to reading from an EPROM. Reprogramming the AT29LV512 is performed on a sector basis; 128 bytes of data are loaded into the device and then simultaneously programmed.

During a reprogram cycle, the address locations and 128 bytes of data are captured at microprocessor speed and internally latched, freeing the address and data bus for other operations. Following the initiation of a program cycle, the device will automatically erase the sector and then program the latched data using an internal control timer. The end of a program cycle can be detected by $\overline{\text{DATA}}$ polling of I/O7. Once the end of a program cycle has been detected, a new access for a read or program can begin.

Block Diagram



Device Operation

READ: The AT29LV512 is accessed like an EPROM. When $\overline{\text{CE}}$ and $\overline{\text{OE}}$ are low and $\overline{\text{WE}}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{\text{CE}}$ or $\overline{\text{OE}}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

SOFTWARE DATA PROTECTION PROGRAMMING: The AT29LV512 has 512 individual sectors, each 128 bytes. Using the software data protection feature, byte loads are used to enter the 128 bytes of a sector to be programmed. The AT29LV512 can only be programmed or reprogrammed using the software data protection feature. The device is programmed on a sector basis. If a byte of data within the sector is to be changed, data for the entire 128-byte sector must be loaded into the device. The AT29LV512 automatically does a sector erase prior to loading the data into the sector. An erase command is not required.

Software data protection protects the device from inadvertent programming. A series of three program commands to specific addresses with specific data must be presented to the device before programming may occur. After writing the three-byte command sequence (and after t_{WC}), the entire device is protected. The same three program commands must begin each program operation. All software program commands must obey the sector program timing specifications. Power transitions will not reset the software data protection feature, however the software feature will guard against inadvertent program cycles during power transitions.

Once set, software data protection will remain active unless the disable command sequence is issued.

After setting SDP, any attempt to write to the device without the three-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, a read operation will effectively be a polling operation.

After the software data protection's three-byte command code is given, a byte load is performed by applying a low pulse on the $\overline{\text{WE}}$ or $\overline{\text{CE}}$ input with $\overline{\text{CE}}$ or $\overline{\text{WE}}$ low (respectively) and $\overline{\text{OE}}$ high. The address is latched on the falling edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$, whichever occurs last. The data is latched by the first rising edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$.

The 128 bytes of data must be loaded into each sector. Any byte that is not loaded during the programming of its sector will be erased to read FFh. Once the bytes of a sector are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data byte has been loaded into the device, successive bytes are entered in the same manner. Each new byte to be programmed must have its high to low

continued on next page

Device Operation (Continued)

transition on $\overline{WE}$ (or $\overline{CE}$) within 150 µs of the low to high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding byte. If a high to low transition is not detected within 150 µs of the last low to high transition, the load period will end and the internal programming period will start. A7 to A15 specify the sector address. The sector address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A6 specify the byte address within the sector. The bytes may be loaded in any order; sequential loading is not required.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT29LV512 in the following ways: (a) V_{CC} sense— if V_{CC} is below 1.8 V (typical), the program function is inhibited. (b) V_{CC} power on delay— once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 10 ms (typical) before programming. (c) Program inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (d) Noise filter— pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle.

INPUT LEVELS: While operating with a 3.3 V ±10% power supply, the address inputs and control inputs ($\overline{OE}$, $\overline{CE}$ and $\overline{WE}$) may be driven from 0 to 5.5 V without adversely affecting the operation of the device. The I/O lines can only be driven from 0 to 3.6 volts.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product. In addition, users may wish to use the software product identification mode to identify the part (i.e. using the device code), and have the system software use the appropriate sector size for program operations. In this manner, the user can have a common board design for 256K to 4-megabit densities and, with each density's sector size in a memory map, have the system software apply the appropriate sector size.

For details, see Operating Modes (for hardware operation) or Software Product Identification. The manufacturer and device code is the same for both modes.

$\overline{DATA}$ POLLING: The AT29LV512 features $\overline{DATA}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{DATA}$ polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ polling the AT29LV512 provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

OPTIONAL CHIP ERASE MODES: The entire device may be erased by either using a six-byte software code or high voltage. For details, please contact Atmel.

3

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6 V to +6.25 V
All Output Voltages with Respect to Ground	-0.6 V to V_{CC} +0.6 V
Voltage on A9 (including N.C. Pins) with Respect to Ground	-0.6 V to +13.5 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Note: 1. These parameters are characterized and not 100% tested.

D.C. and A.C. Operating Range

		AT29LV512-20	AT29LV512-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		3.3 V ± 0.3 V	3.3 V ± 0.3 V

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	AI	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Ai	D_{OUT}
Program[2]	V_{IL}	V_{IH}	V_{IL}	Ai	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	X	High Z
Program Inhibit	X	X	V_{IH}		
Program Inhibit	X	V_{IL}	X		
Output Disable	X	V_{IH}	X		High Z
Product Identification	V_{IL}	V_{IL}	V_{IH}	A1-A15 = V_{IL}, A9 = V_H[3], A0 = V_{IL}	Manufacturer Code[4]
				A1-A15 = V_{IL}, A9 = V_H[3], A0 = V_{IH}	Device Code[4]

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.
3. V_H = 12.0 V ± 0.5 V.
4. Manufacturer Code: 1F, Device Code: 3D.

D.C. Characteristics

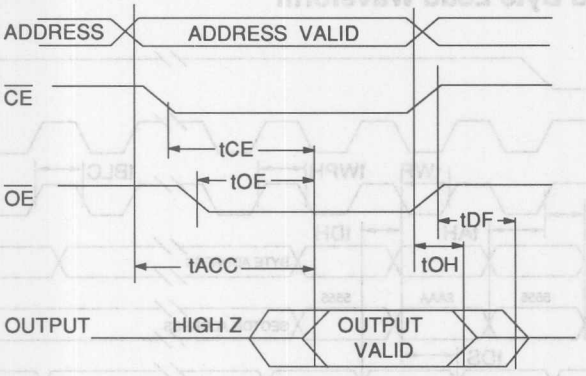
Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}			1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0 V to V_{CC}			1	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3 V to V_{CC}	Com.		20	µA
			Ind.		50	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0 V to V_{CC}			1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6 V			15	mA
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA; V_{CC} = 3.0 V			.45	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA; V_{CC} = 3.0 V		2.4		V

A.C. Read Characteristics

Symbol	Parameter	AT29LV512-20 Min	AT29LV512-20 Max	AT29LV512-25 Min	AT29LV512-25 Max	Units
t_{ACC}	Address to Output Delay		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	100	0	120	ns
t_{DF} (3,4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	55	0	80	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		ns

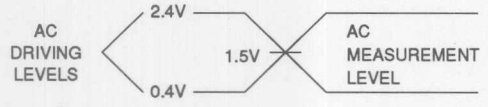
3

A.C. Read Waveforms



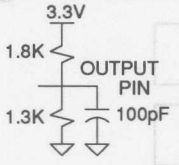
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

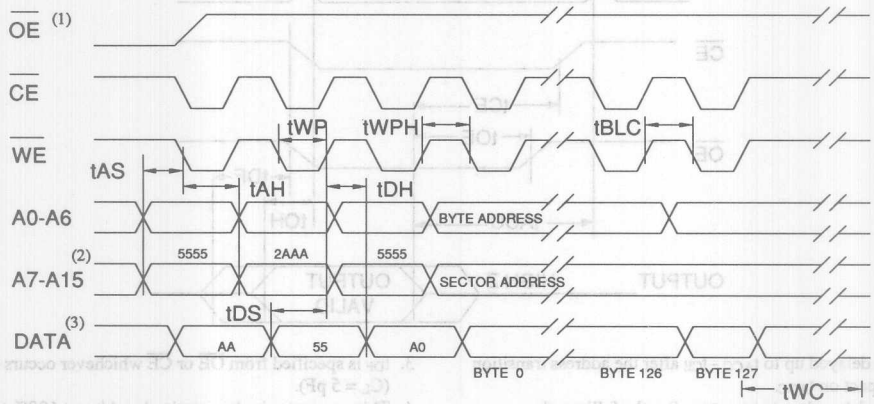
Output Test Load



Program Cycle Characteristics

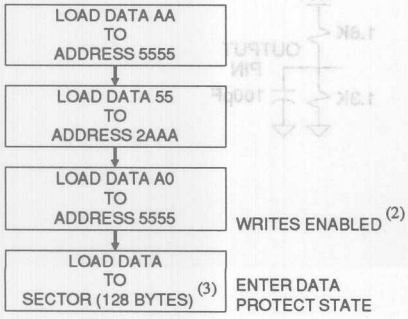
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		20	ms
t_{AS}	Address Set-up Time	10		ns
t_{AH}	Address Hold Time	100		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}	Data Hold Time	10		ns
t_{WP}	Write Pulse Width	200		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	200		ns

Software Protected Byte Load Waveform



Notes:
1. $\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
2. A7 through A15 must specify the sector address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
3. **All bytes that are not loaded within the sector being programmed will be erased to FF.**

Software Data Protection Write Algorithm (1)



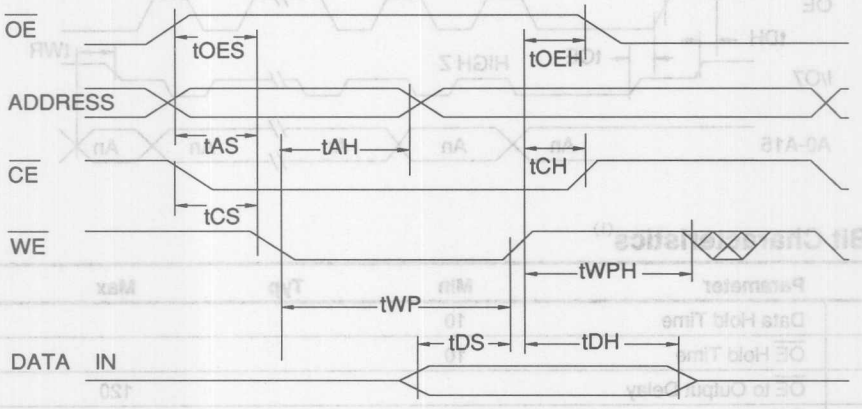
Notes for software program code:
1. Data Format: I/O7–I/O0 (Hex);
   Address Format: A14–A0 (Hex).
2. Data Protect state will be re-activated at end of program cycle.
3. 128 bytes of data **MUST BE** loaded.

A.C. Byte Load Characteristics

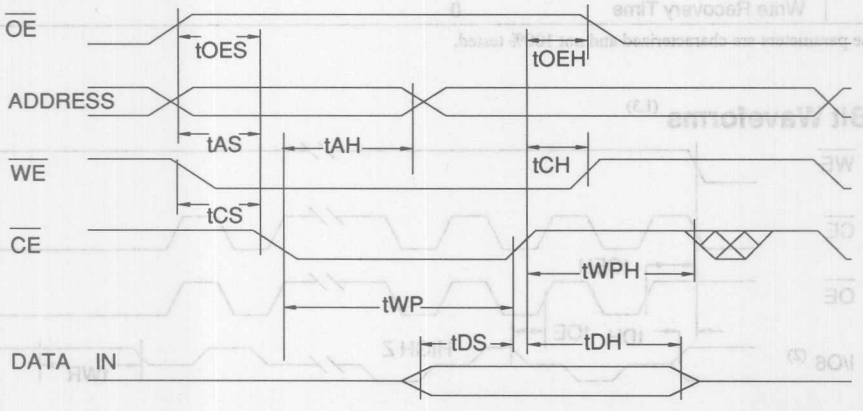
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	10		ns
t_{AH}	Address Hold Time	100		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	200		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time	10		ns
t_{WC}	Write Cycle Time		20	ms

A.C. Byte Load Waveforms During Software Protection [1,2]

$\overline{WE}$ Controlled



$\overline{CE}$ Controlled



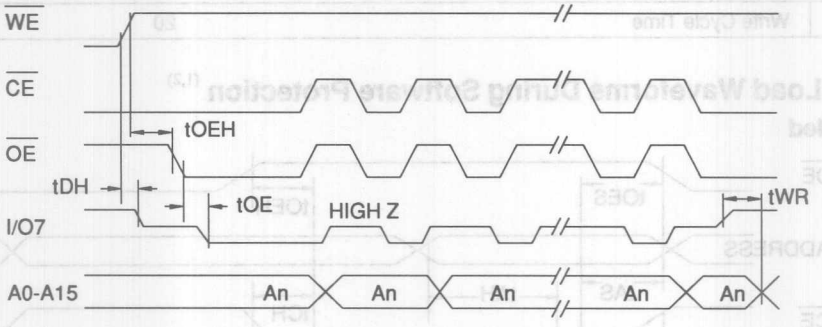
Notes:
1. The software data protection commands must be applied prior to byte loads.
2. A complete sector (128 bytes) should be loaded using these waveforms as shown in the Software Protected Byte Load waveforms (see previous page).

$\overline{\text{Data}}$ Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			120	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{Data}}$ Polling Waveforms

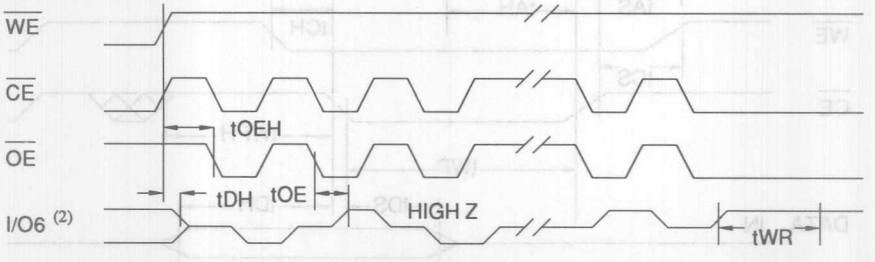


Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			120	ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

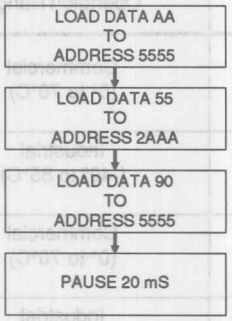
Note: 1. These parameters are characterized and not 100% tested.

Toggle Bit Waveforms [1,3]



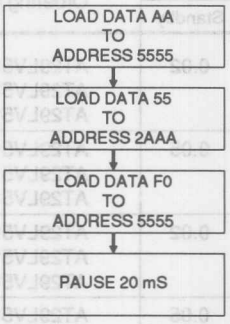
Notes:
1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry [1]



ENTER PRODUCT IDENTIFICATION MODE [2,3]

Software Product Identification Exit [1]



EXIT PRODUCT IDENTIFICATION MODE [4]

Notes for software product identification:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. A1 - A15 = V_{IL}.
   Manufacture Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
200	15	0.02	AT29LV512-20DC AT29LV512-20JC AT29LV512-20PC	32D6 32J 32P6	Commercial (0° to 70°C)
	15	0.05	AT29LV512-20DI AT29LV512-20JI AT29LV512-20PI	32D6 32J 32P6	Industrial (-40° to 85°C)
250	15	0.02	AT29LV512-25DC AT29LV512-25JC AT29LV512-25PC	32D6 32J 32P6	Commercial (0° to 70°C)
	15	0.05	AT29LV512-25DI AT29LV512-25JI AT29LV512-25PI	32D6 32J 32P6	Industrial (-40° to 85°C)

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
200	15	0.02	AT29LV512-20TC	32T	Commercial (0° to 70°C)
250	15	0.02	AT29LV512-25TC	32T	Commercial (0° to 70°C)

Package Type	
32D6	32 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
32T	32 Lead, Thin Small Outline Package (TSOP)

1 Megabit (128K x 8) 5-Volt Only CMOS PEROM

Features

- Fast Read Access Time - 90 ns
- Five-Volt-Only Reprogramming
- Sector Program Operation
  - Single Cycle Reprogram (Erase and Program)
  - 1024 Sectors (128 bytes/sector)
  - Internal Address and Data Latches for 128 Bytes
- Fast Sector Program Cycle Time - 10 ms
- Internal Program Control and Timer
- Low Power Dissipation
  - 50 mA Active Current
  - 100 µA CMOS Standby Current
- Hardware and Software Data Protection
- DATA Polling for End of Program Detection
- High Reliability CMOS Technology
  - 1000 Program Cycles per Sector
  - 10-Year Data Retention
- Single 5 V ±10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- Full Military, Commercial, and Industrial Temperature Ranges

Description

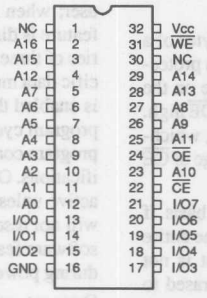
The AT29C010 is a five-volt-only in-system Programmable and Erasable Read Only Memory (PEROM). Its 1 megabit of memory is organized as 131,072 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 90 ns with power dissipation of just 275 mW over the commercial temperature range. When the device is deselected, the CMOS standby current is less than 100 µA.

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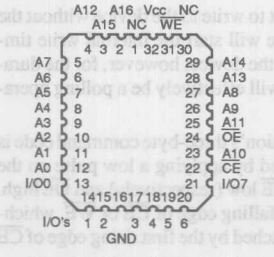
Pin Configurations

Pin Name	Function
A0 - A16	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

DIP Top View

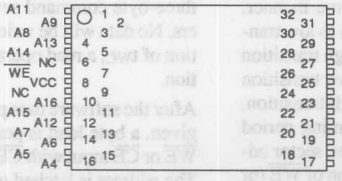


PLCC and LCC Top View



Note: PLCC package pin 30 is a DON'T CONNECT.

TSOP Top View
Type 1

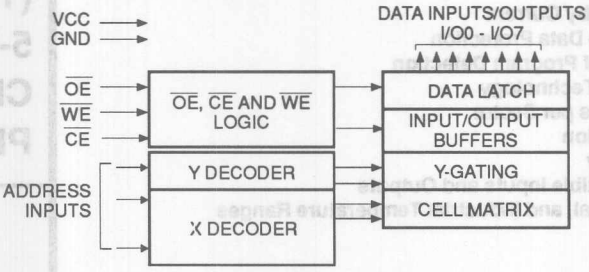


Description (Continued)

To allow for simple in-system reprogrammability, the AT29C010 does not require high input voltages for programming. Five-volt-only commands determine the operation of the device. Reading data out of the device is similar to reading from an EPROM. Reprogramming the AT29C010 is performed on a sector basis; 128 bytes of data are loaded into the device and then simultaneously programmed.

During a reprogram cycle, the address locations and 128 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a program cycle, the device will automatically erase the sector and then program the latched data using an internal control timer. The end of a program cycle can be detected by DATA polling of I/O7. Once the end of a program cycle has been detected, a new access for a read or program can begin.

Block Diagram



Device Operation

READ: The AT29C010 is accessed like an EPROM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

BYTE LOAD: Byte loads are used to enter the 128 bytes of a sector to be programmed or the software codes for data protection. A byte load is performed by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$.

PROGRAM: The device is reprogrammed on a sector basis. If a byte of data within a sector is to be changed, data for the entire sector must be loaded into the device. Any byte that is not loaded during the programming of its sector will be erased to read FFh. Once the bytes of a sector are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data byte has been loaded into the device, successive bytes are entered in the same manner. Each new byte to be programmed must have its high to low transition on $\overline{WE}$ (or $\overline{CE}$) within 150 µs of the low to high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding byte. If a high to low transition is not detected within 150 µs of the last low to high transition, the load period will end and the internal programming period will start. A7 to A16 specify the sector address. The sector address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A6 specify the byte address within the sector. The bytes may be loaded in any order; sequential loading is not required.

SOFTWARE DATA PROTECTION: A software controlled data protection feature is available on the AT29C010. Once the software protection is enabled a software algorithm must be issued to the device before a program may be performed. The software protection feature may be enabled or disabled by the user; when shipped from Atmel, the software data protection feature is disabled. To enable the software data protection, a series of three program commands to specific addresses with specific data must be performed. After the software data protection is enabled the same three program commands must begin each program cycle in order for the programs to occur. All software program commands must obey the sector program timing specifications. Once set, the software data protection feature remains active unless its disable command is issued. Power transitions will not reset the software data protection feature, however the software feature will guard against inadvertent program cycles during power transitions.

Once set, software data protection will remain active unless the disable command sequence is issued.

After setting SDP, any attempt to write to the device without the three-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, a read operation will effectively be a polling operation.

After the software data protection's three-byte command code is given, a byte load is performed by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$.

continued on next page

Device Operation (Continued)

The 128 bytes of data must be loaded into each sector. Any byte that is not loaded during the programming of its sector will be erased to read FFh. Once the bytes of a sector are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data byte has been loaded into the device, successive bytes are entered in the same manner. Each new byte to be programmed must have its high to low transition on $\overline{WE}$ (or $\overline{CE}$) within 150 µs of the low to high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding byte. If a high to low transition is not detected within 150 µs of the last low to high transition, the load period will end and the internal programming period will start. A7 to A15 specify the sector address. The sector address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A6 specify the byte address within the sector. The bytes may be loaded in any order; sequential loading is not required.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT29C010 in the following ways: (a) V_{CC} sense— if V_{CC} is below 3.8 V (typical), the program function is inhibited. (b) V_{CC} power on delay— once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 5 ms (typical) before programming. (c) Program inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (d) Noise filter— pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product. In addition, users may wish to use the software product identification mode to identify the part (i.e. using the device code), and have the system software use the appropriate sector size for program operations. In this manner, the user can have a common board design for 256K to 4-megabit densities and, with each density's sector size in a memory map, have the system software apply the appropriate sector size.

For details, see Operating Modes (for hardware operation) or Software Product Identification. The manufacturer and device code is the same for both modes.

$\overline{DATA}$ POLLING: The AT29C010 features $\overline{DATA}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{DATA}$ polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ polling the AT29C010 provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

OPTIONAL CHIP ERASE MODES: The entire device may be erased by either using a six-byte software code or high voltage. For details, please contact Atmel.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6 V to +6.25 V
All Output Voltages with Respect to Ground	-0.6 V to V_{CC} +0.6 V
Voltage on $\overline{OE}$ with Respect to Ground	-0.6 V to +13.5 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Note: 1. This parameter is characterized and is not 100% tested.

D.C. and A.C. Operating Range

		AT29C010-90	AT29C010-12	AT29C010-15	AT29C010-20
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 10%	5 V ± 10%	5 V ± 10%	5 V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Ai	D_{OUT}
Program[2]	V_{IL}	V_{IH}	V_{IL}	Ai	D_{IN}
5V Chip Erase	V_{IL}	V_{IH}	V_{IL}	Ai	
Standby/Write Inhibit	V_{IH}	X[1]	X	X	High Z
Program Inhibit	X	X	V_{IH}		
Program Inhibit	X	V_{IL}	X		
Output Disable	X	V_{IH}	X		High Z
Product Identification	V_{IL}	V_{IL}	V_{IH}	A1-A16 = V_{IL}, A9 = V_H,[3] A0 = V_{IL}	Manufacturer Code[4]
				A1-A16 = V_{IL}, A9 = V_H,[3] A0 = V_{IH}	Device Code[4]

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.
3. V_H = 12.0 V ± 0.5 V.
4. Manufacturer Code: 1F, Device Code: D5

D.C. Characteristics

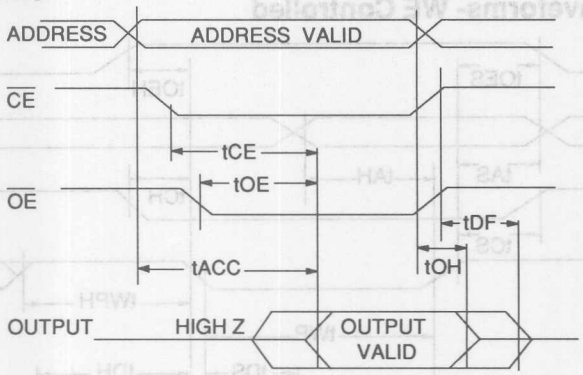
Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0 V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC}	Com.		100	µA
			Ind., Mil.		300	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0 V to V_{CC}			3	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA			50	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA		2.4		V
V_{OH2}	Output High Voltage CMOS	I_{OH} = -100 µA; V_{CC} = 4.5 V		4.2		V

A.C. Read Characteristics

Symbol	Parameter	AT29C010-90		AT29C010-12		AT29C010-15		AT29C010-20		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		90		120		150		200	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		90		120		150		200	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	40	0	50	0	70	0	80	ns
t_{DF} (3,4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	40	0	40	0	50	0	55	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		ns

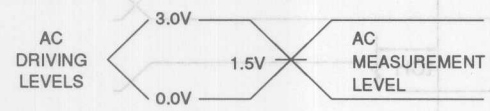
3

A.C. Read Waveforms



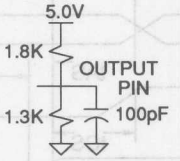
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



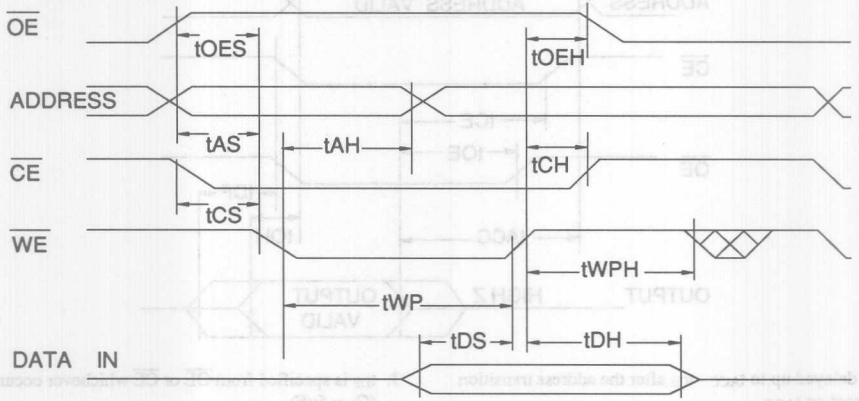
t_R, t_F < 5 ns

Output Test Load

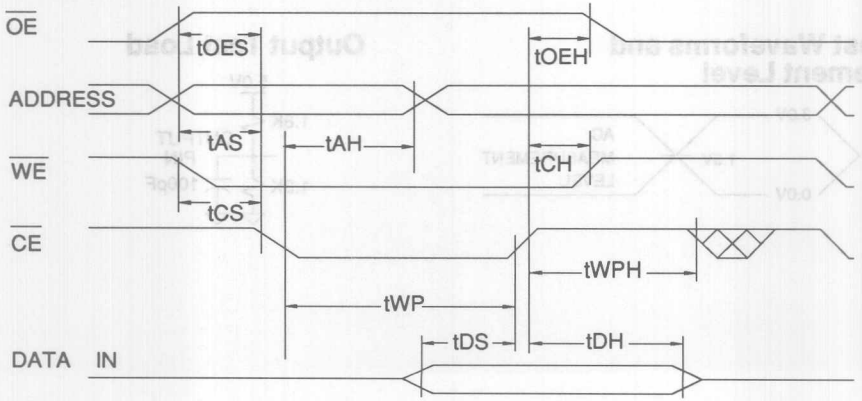


Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	90		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{WC}	Write Cycle Time		10	ms

A.C. Byte Load Waveforms- $\overline{WE}$ Controlled



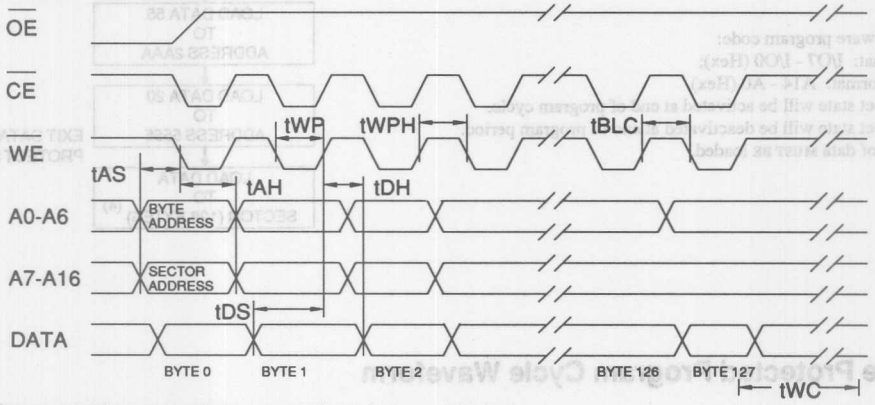
A.C. Byte Load Waveforms- $\overline{CE}$ Controlled



Program Cycle Characteristics

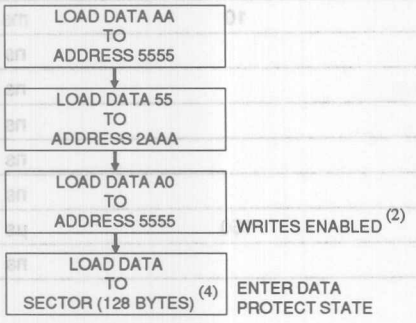
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	90		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	100		ns

Program Cycle Waveforms

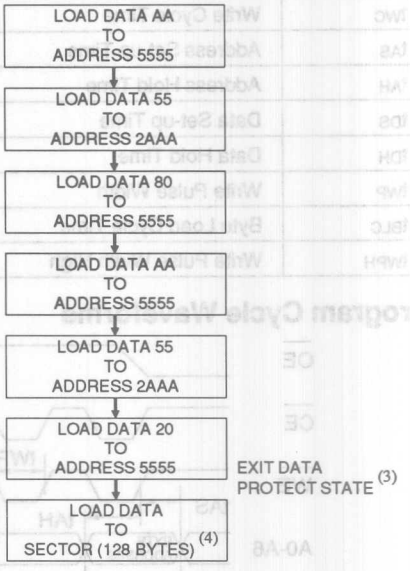


Notes: A7 through A16 must specify the sector address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
All bytes that are not loaded within the sector being programmed will be erased to FF.

Software Data Protection Enable Algorithm [1]

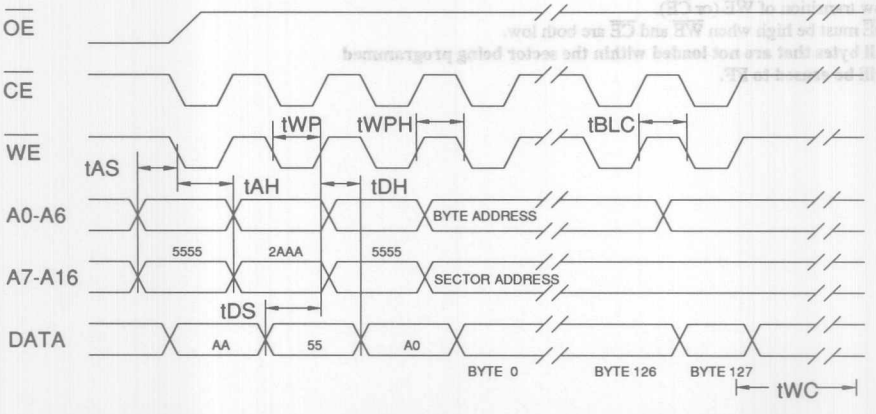


Software Data Protection Disable Algorithm [1]



Notes for software program code:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Data Protect state will be activated at end of program cycle.
3. Data Protect state will be deactivated at end of program period.
4. 128 bytes of data MUST BE loaded.

Software Protected Program Cycle Waveform



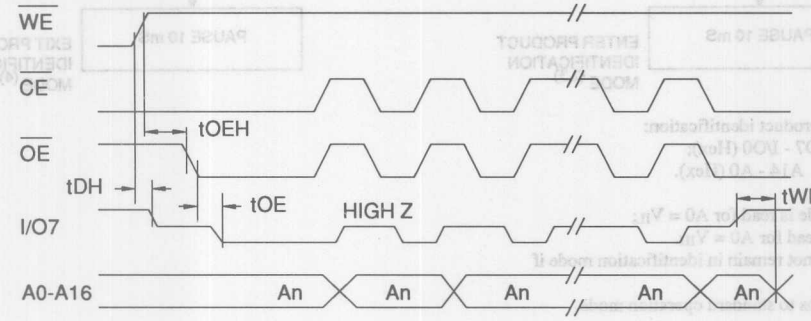
Notes: 1. A7 through A16 must specify the sector address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
2. $\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
3. **All bytes that are not loaded within the sector being programmed *will be erased to FF.***

$\overline{\text{Data}}$ Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{Data}}$ Polling Waveforms

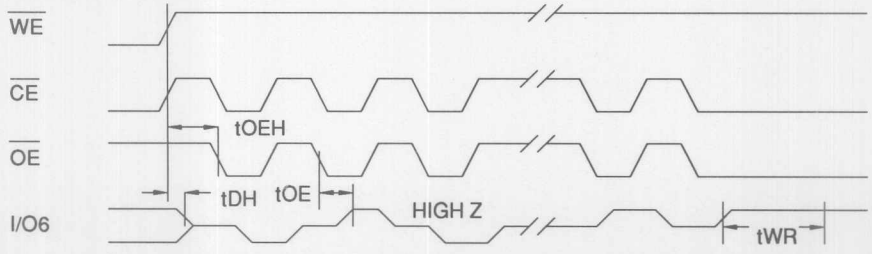


Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

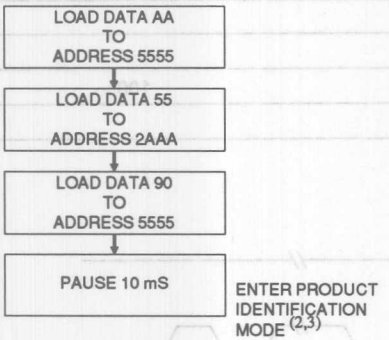
Note: 1. These parameters are characterized and not 100% tested.

Toggle Bit Waveforms

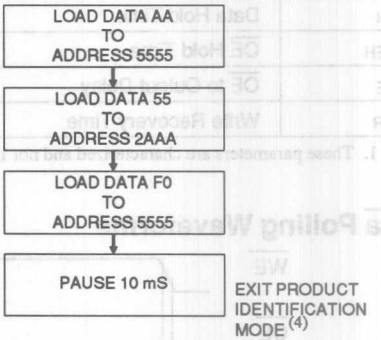


Notes:
1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry [1]

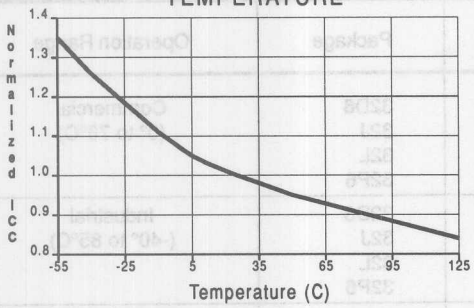


Software Product Identification Exit [1]

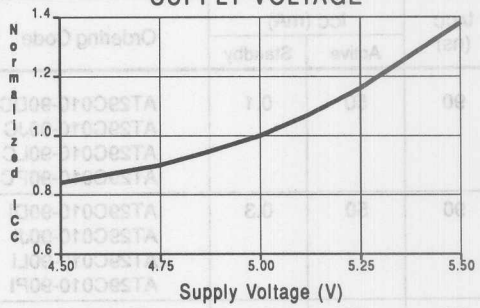


Notes for software product identification:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. A1 - A16 = V_{IL}.
   Manufacture Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.

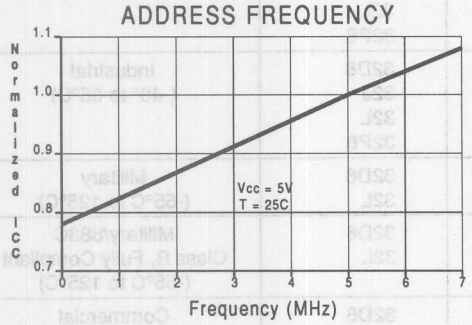
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	50	0.1	AT29C010-90DC AT29C010-90JC AT29C010-90LC AT29C010-90PC	32D6 32J 32L 32P6	Commercial (0° to 70°C)
90	50	0.3	AT29C010-90DI AT29C010-90JI AT29C010-90LI AT29C010-90PI	32D6 32J 32L 32P6	Industrial (-40° to 85°C)
120	50	0.1	AT29C010-12DC AT29C010-12JC AT29C010-12LC AT29C010-12PC	32D6 32J 32L 32P6	Commercial (0° to 70°C)
120	50	0.3	AT29C010-12DI AT29C010-12JI AT29C010-12LI AT29C010-12PI	32D6 32J 32L 32P6	Industrial (-40° to 85°C)
			AT29C010-12DM AT29C010-12LM	32D6 32L	Military (-55°C to 125°C)
			AT29C010-12DM/883 AT29C010-12LM/883	32D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	50	0.1	AT29C010-15DC AT29C010-15JC AT29C010-15LC AT29C010-15PC	32D6 32J 32L 32P6	Commercial (0° to 70°C)
150	50	0.3	AT29C010-15DI AT29C010-15JI AT29C010-15LI AT29C010-15PI	32D6 32J 32L 32P6	Industrial (-40° to 85°C)
			AT29C010-15DM AT29C010-15LM	32D6 32L	Military (-55°C to 125°C)
			AT29C010-15DM/883 AT29C010-15LM/883	32D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	50	0.1	AT29C010-20DC AT29C010-20JC AT29C010-20LC AT29C010-20PC	32D6 32J 32L 32P6	Commercial (0° to 70°C)
200	50	0.3	AT29C010-20DI AT29C010-20JI AT29C010-20LI AT29C010-20PI	32D6 32J 32L 32P6	Industrial (-40° to 85°C)
			AT29C010-20DM AT29C010-20LM	32D6 32L	Military (-55°C to 125°C)
			AT29C010-20DM/883 AT29C010-20LM/883	32D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	50	0.1	AT29C010-12TC	32T	Commercial (0° to 70°C)
150	50	0.1	AT29C010-15TC	32T	Commercial (0° to 70°C)

Package Type	
32D6	32 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
32T	32 Lead, Thin Small Outline Package (TSOP)

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	50	0.1	AT29C010-12TC	32T	Commercial (0° to 70°C)
150	50	0.1	AT29C010-15TC	32T	Commercial (0° to 70°C)

Package Type	
32DM	32 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
32T	32 Lead, Thin Small Outline Package (TSOP)

1 Megabit (128K x 8) 3-Volt Only CMOS PEROM

Preliminary

PRELIMINARY

Features

- **Single 3.3 V ± 10% Supply**
- **Three-Volt-Only Read and Write Operation**
- **Software Protected Programming**
- **Low Power Dissipation**
  - **15 mA Active Current**
  - **20 µA CMOS Standby Current**
- **Fast Read Access Time - 200 ns**
- **Sector Program Operation**
  - **Single Cycle Reprogram (Erase and Program)**
  - **1024 Sectors (128 bytes/sector)**
  - **Internal Address and Data Latches for 128 Bytes**
- **Fast Sector Program Cycle Time - 20 ms Max.**
- **Internal Program Control and Timer**
- **DATA Polling for End of Program Detection**
- **High Reliability CMOS Technology**
  - **1000 Program Cycles per Sector**
  - **10-Year Data Retention**
- **CMOS and TTL Compatible Inputs and Outputs**
- **Commercial and Industrial Temperature Ranges**

Description

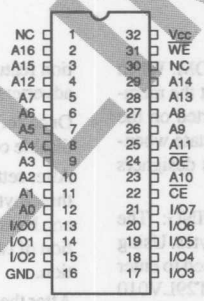
The AT29LV010 is a three-volt-only in-system Programmable Erasable Read Only Memory (PEROM). Its one-megabit of memory is organized as 131,072 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 200 ns with power dissipation of just 54 mW over the commercial temperature range. When the device is deselected, the CMOS standby current is less than 20 µA.

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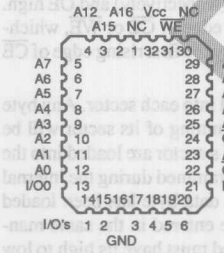
Pin Configurations

Pin Name	Function
A0 - A16	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

DIP Top View

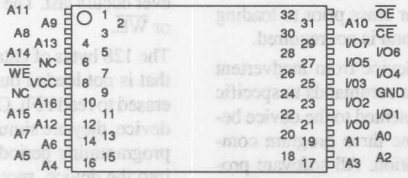


PLCC, LCC Top View



Note: PLCC package pin 30 is a DON'T CONNECT.

TSOP Top View
Type 1

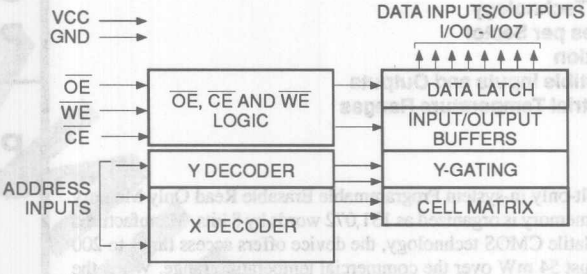


Description (Continued)

To allow for simple in-system reprogrammability, the AT29LV010 does not require high input voltages for programming. Three-volt-only commands determine the operation of the device. Reading data out of the device is similar to reading from an EPROM. Reprogramming the AT29LV010 is performed on a sector basis; 128 bytes of data are loaded into the device and then simultaneously programmed.

During a reprogram cycle, the address locations and 128 bytes of data are captured at microprocessor speed and internally latched, freeing the address and data bus for other operations. Following the initiation of a program cycle, the device will automatically erase the sector and then program the latched data using an internal control timer. The end of a program cycle can be detected by $\overline{\text{DATA}}$ polling of I/O7. Once the end of a program cycle has been detected, a new access for a read or program can begin.

Block Diagram



Device Operation

READ: The AT29LV010 is accessed like an EPROM. When $\overline{\text{CE}}$ and $\overline{\text{OE}}$ are low and $\overline{\text{WE}}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{\text{CE}}$ or $\overline{\text{OE}}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

SOFTWARE DATA PROTECTION PROGRAMMING: The AT29LV010 has 1024 individual sectors, each 128 bytes. Using the software data protection feature, byte loads are used to enter the 128 bytes of a sector to be programmed. The AT29LV010 can only be programmed or reprogrammed using the software data protection feature. The device is programmed on a sector basis. If a byte of data within the sector is to be changed, data for the entire 128-byte sector must be loaded into the device. The AT29LV010 automatically does a sector erase prior to loading the data into the sector. An erase command is not required.

Software data protection protects the device from inadvertent programming. A series of three program commands to specific addresses with specific data must be presented to the device before programming may occur. The same three program commands must begin each program operation. All software program commands must obey the sector program timing specifications. Power transitions will not reset the software data protection feature, however the software feature will guard against inadvertent program cycles during power transitions.

Once set, software data protection will remain active unless the disable command sequence is issued.

After setting SDP, any attempt to write to the device without the three-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, a read operation will effectively be a polling operation.

After the software data protection's three-byte command code is given, a byte load is performed by applying a low pulse on the $\overline{\text{WE}}$ or $\overline{\text{CE}}$ input with $\overline{\text{CE}}$ or $\overline{\text{WE}}$ low (respectively) and $\overline{\text{OE}}$ high. The address is latched on the falling edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$, whichever occurs last. The data is latched by the first rising edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$.

The 128 bytes of data must be loaded into each sector. Any byte that is not loaded during the programming of its sector will be erased to read FFh. Once the bytes of a sector are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data byte has been loaded into the device, successive bytes are entered in the same manner. Each new byte to be programmed must have its high to low transition on $\overline{\text{WE}}$ (or $\overline{\text{CE}}$) within 150 µs of the low to high tran-

continued on next page

Device Operation (Continued)

sition of $\overline{WE}$ (or $\overline{CE}$) of the preceding byte. If a high to low transition is not detected within 150 µs of the last low to high transition, the load period will end and the internal programming period will start. A7 to A16 specify the sector address. The sector address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A6 specify the byte address within the sector. The bytes may be loaded in any order; sequential loading is not required.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT29LV010 in the following ways: (a) V_{CC} sense— if V_{CC} is below 1.8 V (typical), the program function is inhibited. (b) V_{CC} power on delay— once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 10 ms (typical) before programming. (c) Program inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (d) Noise filter— pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle.

INPUT LEVELS: While operating with a 3.3 V ±10% power supply, the address inputs and control inputs ($\overline{OE}$, $\overline{CE}$ and $\overline{WE}$) may be driven from 0 to 5.5 V without adversely affecting the operation of the device. The I/O lines can only be driven from 0 to 3.6 volts.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product. In addition, users may wish to use the software product identification mode to identify the part (i.e. using the device code), and have the system software use the appropriate sector size for program operations. In this manner, the user can have a common board design for 256K to 4-megabit densities and, with each density's sector size in a memory map, have the system software apply the appropriate sector size.

For details, see Operating Modes (for hardware operation) or Software Product Identification. The manufacturer and device code is the same for both modes.

$\overline{DATA}$ POLLING: The AT29LV010 features $\overline{DATA}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{DATA}$ polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ polling the AT29LV010 provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

OPTIONAL CHIP ERASE MODES: The entire device may be erased by either using a six-byte software code or high voltage. For details, please contact Atmel.

3

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6 V to +6.25 V
All Output Voltages with Respect to Ground	-0.6 V to V_{CC} +0.6 V
Voltage on A9 (including N.C. Pins) with Respect to Ground	-0.6 V to +13.5 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Note: 1. These parameters are characterized and not 100% tested.

D.C. and A.C. Operating Range

		AT29LV010-20	AT29LV010-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		3.3 V ± 0.3 V	3.3 V ± 0.3 V

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	AI	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Ai	D_{OUT}
Program[2]	V_{IL}	V_{IH}	V_{IL}	Ai	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	X	High Z
Program Inhibit	X	X	V_{IH}		
Program Inhibit	X	V_{IL}	X		
Output Disable	X	V_{IH}	X		High Z
Product Identification	V_{IL}	V_{IL}	V_{IH}	A1-A16 = V_{IL}, A9 = V_H[3], A0 = V_{IL}	Manufacturer Code[4]
				A1-A16 = V_{IL}, A9 = V_H[3], A0 = V_{IH}	Device Code[4]

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.
3. V_H = 12.0 V ± 0.5 V.
4. Manufacturer Code: 1F, Device Code: 35.

D.C. Characteristics

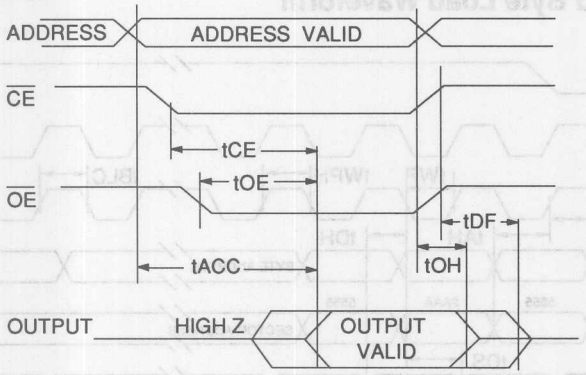
Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}			1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0 V to V_{CC}			1	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3 V to V_{CC}	Com.		20	µA
			Ind.		50	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0 V to V_{CC}			1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6 V			15	mA
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA; V_{CC} = 3.0 V			.45	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA; V_{CC} = 3.0 V		2.4		V

A.C. Read Characteristics

Symbol	Parameter	AT29LV010-20 Min	AT29LV010-20 Max	AT29LV010-25 Min	AT29LV010-25 Max	Units
t_{ACC}	Address to Output Delay		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	100	0	120	ns
t_{DF} (3,4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	55	0	80	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		ns

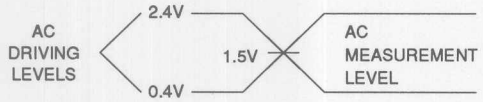
3

A.C. Read Waveforms



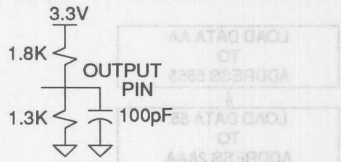
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

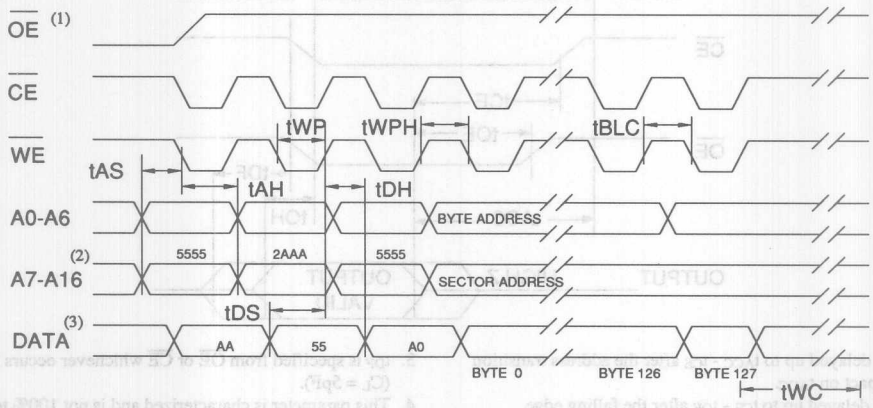
Output Test Load



Program Cycle Characteristics

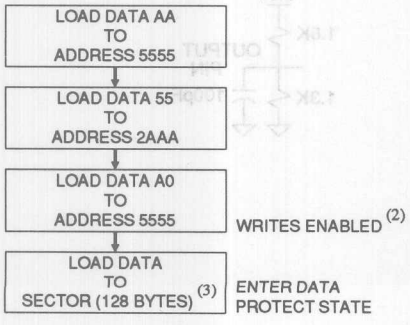
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		20	ms
t_{AS}	Address Set-up Time	10		ns
t_{AH}	Address Hold Time	100		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}	Data Hold Time	10		ns
t_{WP}	Write Pulse Width	200		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	200		ns

Software Protected Byte Load Waveform



Notes:
1. $\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
2. A7 through A16 must specify the sector address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
3. **All bytes that are not loaded within the sector being programmed will be erased to FF.**

Software Data Protection Write Algorithm (1)



Notes for software program code:
1. Data Format: I/O7–I/O0 (Hex);
   Address Format: A14–A0 (Hex).
2. Data Protect state will be re-activated at end of program cycle.
3. 128 bytes of data **MUST BE** loaded.

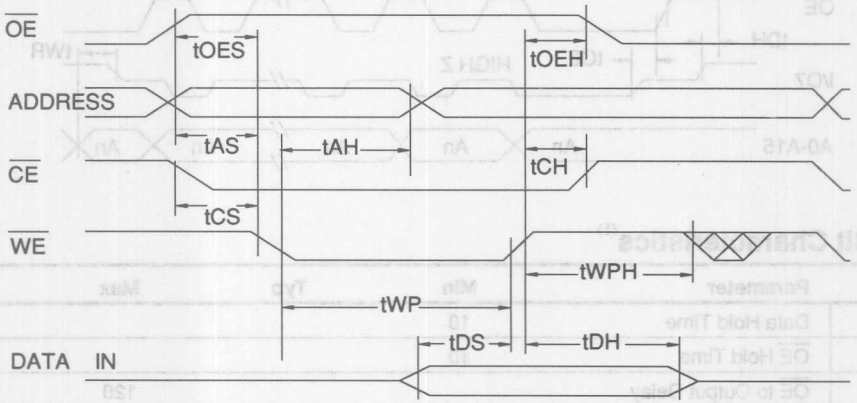
A.C. Byte Load Characteristics

Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	10		ns
t_{AH}	Address Hold Time	100		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	200		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time	10		ns
t_{WC}	Write Cycle Time		20	ms

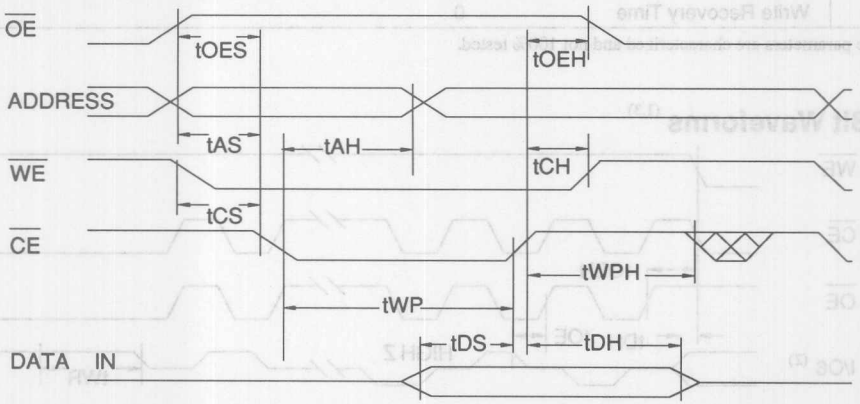
3

A.C. Byte Load Waveforms During Software Protection (1,2)

WE Controlled



CE Controlled



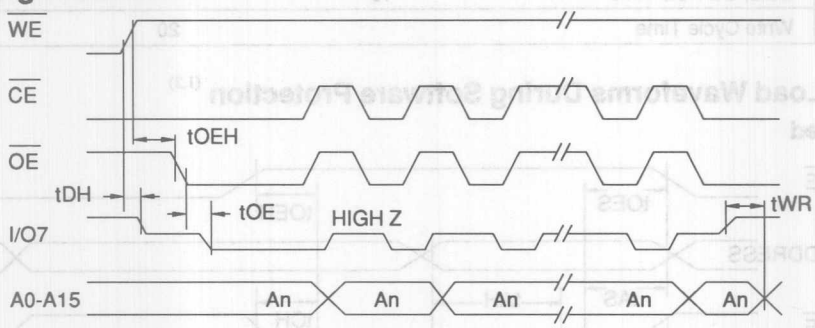
Notes:
1. The software data protection commands must be applied prior to byte loads.
2. A complete sector (128 bytes) should be loaded using these waveforms as shown in the Software Protected Byte Load waveforms (see previous page).

$\overline{\text{Data}}$ Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			120	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{Data}}$ Polling Waveforms

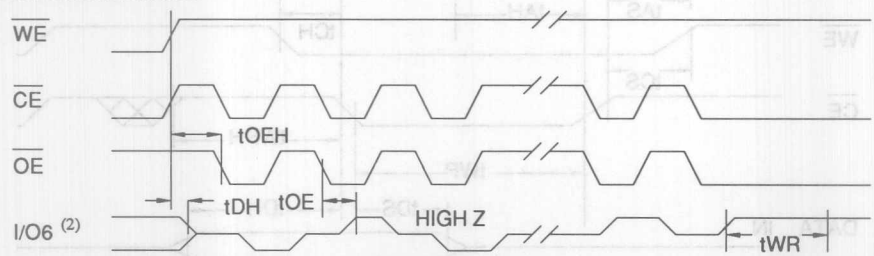


Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			120	ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

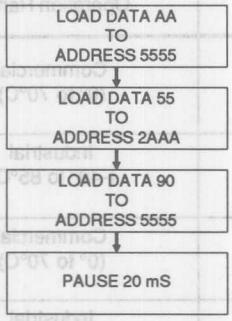
Note: 1. These parameters are characterized and not 100% tested.

Toggle Bit Waveforms [1,3]

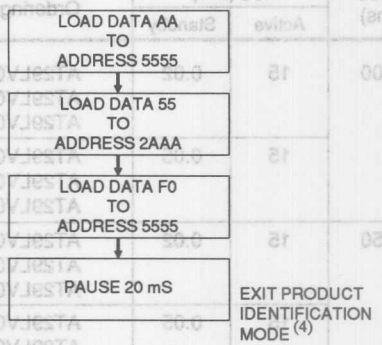


Notes:
1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry [1]



Software Product Identification Exit [1]



Notes for software product identification:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. A1 - A16 = V_{IL}.
   Manufacture Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
200	15	0.02	AT29LV010-20DC AT29LV010-20JC AT29LV010-20PC	32D6 32J 32P6	Commercial (0° to 70°C)
	15	0.05	AT29LV010-20DI AT29LV010-20JI AT29LV010-20PI	32D6 32J 32P6	Industrial (-40° to 85°C)
250	15	0.02	AT29LV010-25DC AT29LV010-25JC AT29LV010-25PI	32D6 32J 32P6	Commercial (0° to 70°C)
	15	0.05	AT29LV010-25DI AT29LV010-25JI AT29LV010-25PI	32D6 32J 32P6	Industrial (-40° to 85°C)

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
200	15	0.02	AT29LV010-20TC	32T	Commercial (0° to 70°C)
250	15	0.02	AT29LV010-25TC	32T	Commercial (0° to 70°C)

Package Type	
32D6	32 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
32T	32 Lead, Thin Small Outline Package (TSOP)

Features

- Fast Read Access Time - 120 ns
- Five-Volt-Only Read and Program Operation
- Software and Hardware Data Protection
- Sector Program Operation
  - Single Cycle Reprogram (Erase and Program)
  - 1024 Sectors (512 bytes/sector)
  - Internal Address and Data Latches for 512 Bytes
- Fast Sector Program Cycle Time - 10 ms
- Internal Program Control and Timer
- Low Power Dissipation
  - 50 mA Active Current
  - 100 µA CMOS Standby Current
- DATA Polling for End of Program Detection
- High Reliability CMOS Technology
  - 1000 Program Cycles
  - 10-Year Data Retention
- Single 5 V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- Full Military, Commercial, and Industrial Temperature Ranges
- DIP is Pin-Compatible with the 256K, 512K, and 1 Megabit

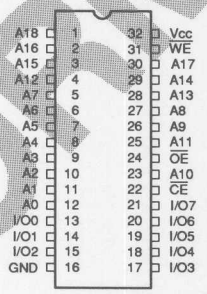
Description

The AT29C040 is a five-volt-only in-system Programmable and Erasable Read Only Memory (PEROM). Its 4 megabit of memory is organized as 524,288 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 120 ns with power dissipation of just 275 mW over the commercial temperature range. When the device is deselected, the CMOS standby current is less than 100 µA. The programming algorithm is identical to Atmel's 256K, 512K, and 1-megabit Flash PEROMs.

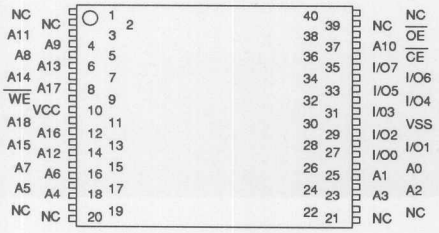
Pin Configurations

Pin Name	Function
A0 - A18	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

DIP Top View



TSOP Top View
Type 1



4 Megabit (512K x 8) 5-Volt Only CMOS PEROM

3

Advance Information

ADVANCE INFORMATION

4 Megabit (512K x 8) 5-Volt Only CMOS EPROM

Advance Information

Features

- Single 3.3 V ± 10% Supply
- Three-Volt-Only Read and Write Operation
- Fast Read Access Time - 250 ns
- Software Protected Programming
- Low Power Dissipation
  - 15 mA Active Current
  - 20 µA CMOS Standby Current
- Sector Program Operation
  - Single Cycle Reprogram (Erase and Program)
  - 1024 Sectors (512 bytes/sector)
  - Internal Address and Data Latches for 512 Bytes
- Fast Sector Program Cycle Time - 20 ms Max.
- Internal Program Control and Timer
- DATA Polling for End of Program Detection
- High Reliability CMOS Technology
  - 1000 Program Cycles per Sector
  - 10-Year Data Retention
- CMOS and TTL Compatible Inputs and Outputs
- Commercial and Industrial Temperature Ranges

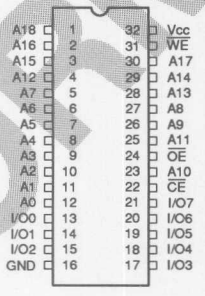
Description

The AT29LV040 is a three-volt-only in-system Programmable and Erasable Read Only Memory (PEROM). Its 4 megabit of memory is organized as 524,288 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 250 ns with power dissipation of just 54 mW over the commercial temperature range. When the device is deselected, the CMOS standby current is less than 20 µA. The programming algorithm is identical to Atmel's 256K, 512K, and 1-megabit Flash PEROMs.

Pin Configurations

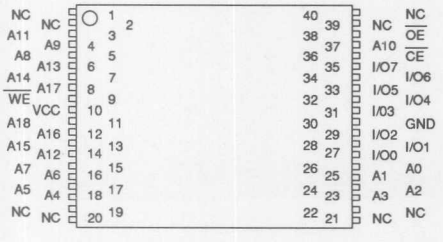
Pin Name	Function
A0 - A18	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

DIP Top View



TSOP Top View

Type 1



3

4 Megabit (512K x 8) 3-Volt Only CMOS PEROM

Advance Information

ADVANCE INFORMATION

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PEROMs (Flash) 3
EPROMs 4
PROMs 5
SRAMs 6
EPLDs 7
Gate Arrays 8
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Microcontroller 12
Packaging Services 13
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Standard Package Outlines 17

Product Information
E²PROMs
PERROMs (Flash)
EPROMs
PROMs
SRAMs
EPLDs
Gate Arrays
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Contents

Section 4

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On-Board, System EPROM Programming with V_{CC} = 5 Volts 4-111
On-Board EPROM Programming 4-113
EPROM Speed Programming 4-117
Programming Socket Adapter 4-125

Features

- Fast Read Access Time - 70 ns
- Low Power CMOS Operation
  - 100 µA max. Standby
  - 20 mA max. Active at 5 MHz
- Wide Selection of JEDEC Standard Packages Including:
  - 28-Lead 600-mil Cerdip, OTP Plastic DIP, SOIC, or TSOP
  - 32-Pad LCC, 32-Lead JLCC and OTP PLCC
- 5V ± 10% Supply
- High Reliability CMOS Technology
  - 2000 V ESD Protection
  - 200 mA Latchup Immunity
- Rapid Programming - 100 µs/byte (typical)
- Two-line Control
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Military, Commercial and Industrial Temperature Ranges

256K (32K x 8) UV Erasable CMOS EPROM

4

Description

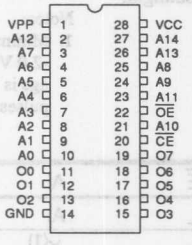
The AT27C256R chip is a low-power, high performance 262,144 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized 32K x 8. It requires only one 5 V power supply in normal read mode operation. Any byte can be accessed in less than 70 ns, eliminating the need for speed reducing WAIT states on high performance microprocessor systems.

Atmel's scaled CMOS technology provides low active power consumption, and fast programming. Power consumption is typically only 8 mA in Active Mode and less than 10 µA in Standby.

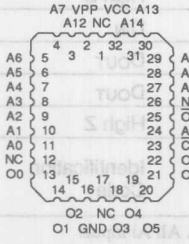
Pin Configurations

Pin Name	Function
A0-A14	Addresses
O0-O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
NC	No Connect

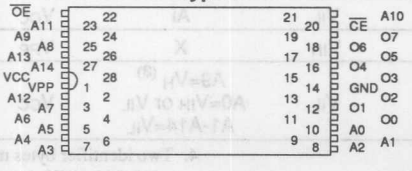
CDIP, PDIP, SOIC Top



LCC, JLCC, PLCC Top



TSOP Top View
Type 1



Note: PLCC Package Pins 1 and 17 are DON'T CONNECT.

Description (Continued)

The AT27C256R comes in a choice of industry standard JEDEC-approved packages including: 28-pin windowed ceramic DIP, 28-pin one time programmable (OTP) plastic DIP, 28-pin OTP gull wing small outline IC (SOIC), 28-pin OTP thin small outline package (TSOP), 32-pad windowed ceramic leadless chip carrier (LCC), 32-lead windowed J-leaded chip carrier (JLCC), and 32-lead OTP plastic J-leaded chip carrier (PLCC). All devices feature two line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

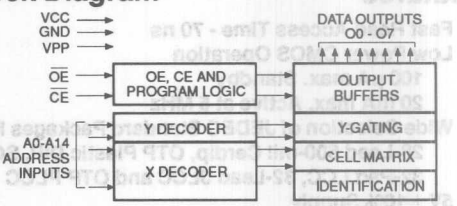
With high density 32K byte storage capability, the AT27C256R allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's 27C256R has additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Erasure Characteristics

The entire memory array of the AT27C256R is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 µW/cm^2 intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 W·sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Voltage on A9 with Respect to Ground	-2.0 V to +14.0 V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0 V to +14.0 V(1)
Integrated UV Erase Dose	7258 W•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC}+0.75 V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	Ai	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	Ai	V_{CC}	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X(1)	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Rapid Program(2)	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC}	D_{IN}
PGM Verify(2)	X	V_{IL}	Ai	V_{PP}	V_{CC}	D_{OUT}
Optional PGM Verify(2)	V_{IL}	V_{IL}	Ai	V_{CC}	V_{CC}	D_{OUT}
PGM Inhibit(2)	V_{IH}	V_{IH}	X	V_{PP}	V_{CC}	High Z
Product Identification(4)	V_{IL}	V_{IL}	A9=V_H (3) A0=V_{IH} or V_{IL} A1-A14=V_{IL}	V_{CC}	V_{CC}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. V_H = 12.0 ± 0.5 V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

D.C. and A.C. Operating Conditions for Read Operation

		AT27C256R					
		-70	-90	-12	-15	-20	-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 10%	5 V ± 10%	5 V ± 10%	5 V ± 10%	5 V ± 10%	5 V ± 10%

4

D.C. and Operating Characteristics for Read Operation

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1 V to V_{CC}+1 V			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1 V to V_{CC}+0.1 V			10	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = 3.8 to V_{CC}+0.3 V			10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS) $\overline{CE}$ = V_{CC}-0.3 to V_{CC}+1.0 V	Com.		100	µA
			Ind.,Mil.		200	µA
		I_{SB2} (TTL) $\overline{CE}$ = 2.0 to V_{CC}+1.0 V	Com.		2	mA
			Ind.,Mil.		3	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = VIL	Com.		20	mA
			Ind.,Mil.		25	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC}+0.75	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			.45	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA		V_{CC}-0.3		V
		I_{OH} = -2.5 mA		3.5		V
		I_{OH} = -400 µA		2.4		V
V_{PP}	V_{PP} Read Voltage	V_{CC} = 5 ± 0.25 V		3.8	V_{CC}+.3	V

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

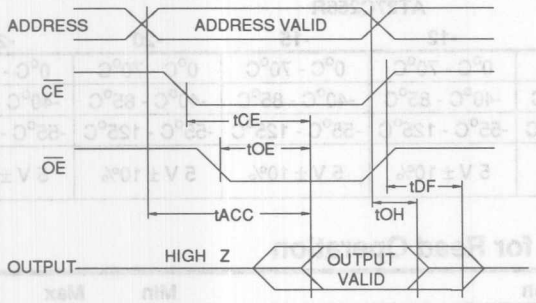
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

A.C. Characteristics for Read Operation

				AT27C256R										
				-70		-90		-12		-15		-20		-25		
Symbol	Parameter	Condition		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{ACC} (4)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Com., Ind.		70		90		120		150		200		250	ns
			Mil.				90		120		150		200		250	ns
t_{CE} (3)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}			70		90		120		150		200		250	ns
t_{OE} (3,4)	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}			30		35		35		60		75		100	ns
t_{DF} (2,5)	$\overline{OE}$ or $\overline{CE}$ High to Output Float	$\overline{CE}$ = V_{IL}			25		30		30		45		55		60	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		0		0		0		0		0		0		ns

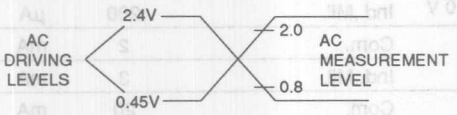
Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

A.C. Waveforms for Read Operation [1]



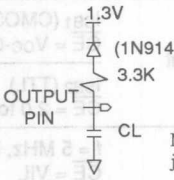
Notes:
1. Timing measurement references are 0.8 V and 2.0 V. Input AC driving levels are 0.45 V and 2.4 V, unless otherwise specified.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first. Output float is defined as the point when data is no longer driven.
3. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
5. This parameter is only sampled and is not 100% tested.

Input Test Waveforms and Measurement Levels



t_R, t_F < 20 ns (10% to 90%)

Output Test Load



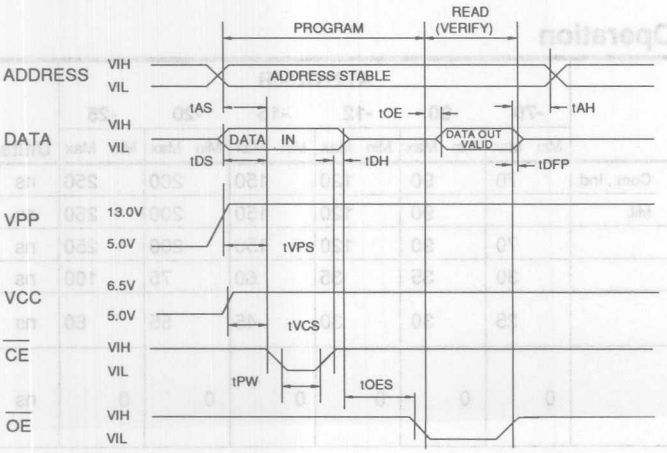
Note: C_L = 100 pF including jig capacitance.

Pin Capacitance (f = 1MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes:
1. The Input Timing Reference is 0.8 V for V_{IL} and 2.0 V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27C256R a 0.1-µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

D.C. Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25$ V, $V_{PP} = 13.0 \pm 0.25$ V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	$V_{CC}+1$	V
V_{OL}	Output Low Volt.	$I_{OL}=2.1$ mA		.45	V
V_{OH}	Output High Volt.	$I_{OH}=-400$ µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			25	mA
I_{PP2}	V_{PP} Current	$\overline{CE}=V_{IL}$		25	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25$ V, $V_{PP} = 13.0 \pm 0.25$ V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Limits Max	Units
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CE}$ Program Pulse Width	(Note 3)	95	105	µs
t_{OE}	Data Valid from $\overline{OE}$	(Note 2)		150	ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) ..... 20 ns
Input Pulse Levels ..... 0.45 V to 2.4 V
Input Timing Reference Level ..... 0.8 V to 2.0 V
Output Timing Reference Level ..... 0.8 V to 2.0 V

Notes:

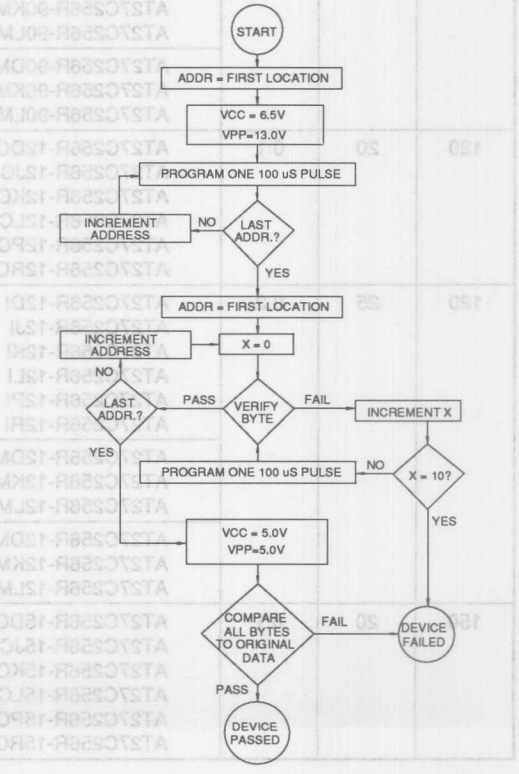
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100 µsec ± 5%.

Atmel's 27C256R Integrated Product Identification Code

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	1	0	0	0	1	1	0	0	8C

Rapid Programming Algorithm

A 100 µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5 V and V_{PP} is raised to 13.0 V. Each address is first programmed with one 100 µs $\overline{CE}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0 V and V_{CC} to 5.0 V. All bytes are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	20	0.1	AT27C256R-70DC AT27C256R-70KC AT27C256R-70LC	28DW6 32KW 32LW	Commercial (0°C to 70°C)
70	25	0.2	AT27C256R-70DI AT27C256R-70KI AT27C256R-70LI	28DW6 32KW 32LW	Industrial (-40°C to 85°C)
90	20	0.1	AT27C256R-90DC AT27C256R-90JC AT27C256R-90KC AT27C256R-90LC AT27C256R-90PC AT27C256R-90RC	28DW6 32J 32KW 32LW 28P6 28R	Commercial (0°C to 70°C)
90	25	0.2	AT27C256R-90DI AT27C256R-90JI AT27C256R-90KI AT27C256R-90LI AT27C256R-90PI AT27C256R-90RI	28DW6 32J 32KW 32LW 28P6 28R	Industrial (-40°C to 85°C)
			AT27C256R-90DM AT27C256R-90KM AT27C256R-90LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C256R-90DM/883 AT27C256R-90KM/883 AT27C256R-90LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	20	0.1	AT27C256R-12DC AT27C256R-12JC AT27C256R-12KC AT27C256R-12LC AT27C256R-12PC AT27C256R-12RC	28DW6 32J 32KW 32LW 28P6 28R	Commercial (0°C to 70°C)
120	25	0.2	AT27C256R-12DI AT27C256R-12JI AT27C256R-12KI AT27C256R-12LI AT27C256R-12PI AT27C256R-12RI	28DW6 32J 32KW 32LW 28P6 28R	Industrial (-40°C to 85°C)
			AT27C256R-12DM AT27C256R-12KM AT27C256R-12LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C256R-12DM/883 AT27C256R-12KM/883 AT27C256R-12LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	20	0.1	AT27C256R-15DC AT27C256R-15JC AT27C256R-15KC AT27C256R-15LC AT27C256R-15PC AT27C256R-15RC	28DW6 32J 32KW 32LW 28P6 28R	Commercial (0°C to 70°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	25	0.2	AT27C256R-15DI AT27C256R-15JI AT27C256R-15KI AT27C256R-15LI AT27C256R-15PI AT27C256R-15RI	28DW6 32J 32KW 32LW 28P6 28R	Industrial (-40°C to 85°C)
			AT27C256R-15DM AT27C256R-15KM AT27C256R-15LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C256R-15DM/883 AT27C256R-15KM/883 AT27C256R-15LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	20	0.1	AT27C256R-20DC AT27C256R-20JC AT27C256R-20KC AT27C256R-20LC AT27C256R-20PC AT27C256R-20RC	28DW6 32J 32KW 32LW 28P6 28R	Commercial (0°C to 70°C)
200	25	0.2	AT27C256R-20DI AT27C256R-20JI AT27C256R-20KI AT27C256R-20LI AT27C256R-20PI AT27C256R-20RI	28DW6 32J 32KW 32LW 28P6 28R	Industrial (-40°C to 85°C)
			AT27C256R-20DM AT27C256R-20KM AT27C256R-20LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C256R-20DM/883 AT27C256R-20KM/883 AT27C256R-20LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	20	0.1	AT27C256R-25DC AT27C256R-25JC AT27C256R-25KC AT27C256R-25LC AT27C256R-25PC AT27C256R-25RC	28DW6 32J 32KW 32LW 28P6 28R	Commercial (0°C to 70°C)
250	25	0.2	AT27C256R-25DI AT27C256R-25JI AT27C256R-25KI AT27C256R-25LI AT27C256R-25PI AT27C256R-25RI	28DW6 32J 32KW 32LW 28P6 28R	Industrial (-40°C to 85°C)
			AT27C256R-25DM AT27C256R-25KM AT27C256R-25LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C256R-25DM/883 AT27C256R-25KM/883 AT27C256R-25LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

4

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	25	0.2	5962-86063 07 XX 5962-86063 07 YX 5962-86063 07 ZX	28DW6 32LW 32KW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	25	0.2	5962-86063 06 XX 5962-86063 06 YX 5962-86063 06 ZX	28DW6 32LW 32KW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	25	0.2	5962-86063 05 XX 5962-86063 05 YX 5962-86063 05 ZX	28DW6 32LW 32KW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
170	25	0.2	5962-86063 04 XX 5962-86063 04 YX 5962-86063 04 ZX	28DW6 32LW 32KW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	25	0.2	5962-86063 01 XX 5962-86063 01 YX 5962-86063 01 ZX	28DW6 32LW 32KW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	25	0.2	5962-86063 02 XX 5962-86063 02 YX 5962-86063 02 ZX	28DW6 32LW 32KW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
300	25	0.2	5962-86063 03 XX 5962-86063 03 YX 5962-86063 03 ZX	28DW6 32LW 32KW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	20	0.1	AT27C256R-90TC	28T	Commercial (0°C to 70°C)
120	20	0.1	AT27C256R-12TC	28T	Commercial (0°C to 70°C)
150	20	0.1	AT27C256R-15TC	28T	Commercial (0°C to 70°C)
200	20	0.1	AT27C256R-20TC	28T	Commercial (0°C to 70°C)
250	20	0.1	AT27C256R-25TC	28T	Commercial (0°C to 70°C)

Ordering Information

Package Type	
28DW6	28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32KW	32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
28R	28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline OTP (SOIC)
28T	28 Lead, Plastic Thin Small Outline Package OTP (TSOP)

	Package Type
28CWB	28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32KW	32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
28R	28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline OTP (SOIC)
28T	28 Lead, Plastic Thin Small Outline Package OTP (TSOP)

256K (32K x 8) Low Voltage UV Erasable CMOS EPROM

Features

- Wide Power Supply Range, 3.0 VDC to 5.5 VDC
- Compatible with JEDEC Standard AT27C256R
- Low Power 3-Volt CMOS Operation
  - 100 µA max. Standby
  - 26 mW max. Active at 1 MHz for V_{CC} = 3.3 VDC
  - 110 mW max. Active at 5 MHz for V_{CC} = 5.5 VDC
- Read Access Time - 200ns
- Wide Selection of JEDEC Standard Packages Including OTP
  - 28-Lead, 600-mil Cerdip and OTP Plastic DIP, SOIC, or TSOP
  - 32-Pad LCC, 32-Lead JLCC, and OTP PLCC
- High Reliability CMOS Technology
  - 2000 V ESD Protection
  - 200 mA Latchup Immunity
- Rapid Programming - 100 µs/byte (typical)
- Two-line Control
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

Description

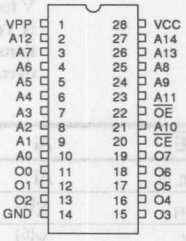
The AT27LV256R chip is a low power, low voltage 262,144 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized as 32K x 8 bits. It requires only one supply in the range of 3.0 to 5.5 VDC in normal read mode operation, making it ideal for battery powered systems.

With a typical power draw of only 18 mW at 1 MHz and V_{CC} at 3.3 VDC, the AT27LV256R will draw less than one-fifth the power of a standard 5-volt EPROM. Standby mode supply current is typically less than 10 µA.

Pin Configurations

Pin Name	Function
A0-A14	Addresses
O0-O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
NC	No Connect

CDIP, PDIP, SOIC Top View

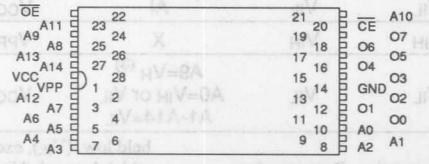


LCC, JLCC, PLCC Top View



Note: PLCC Package Pins 1 and 17 are DON'T CONNECT

TSOP Top View
Type 1



Description (Continued)

The AT27LV256R comes in a choice of industry standard JEDEC-approved through hole and surface mount packages including windowed and one time programmable (OTP) packages, such as the OTP thin small outline package (TSOP). All devices feature two line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

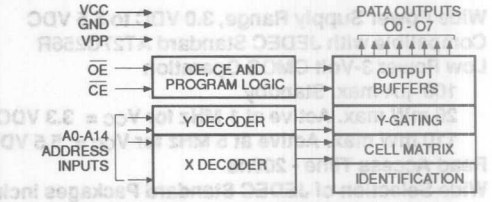
The AT27LV256R operating with V_{CC} at 3.0 VDC produces TTL level outputs that are compatible with standard TTL logic devices operating at V_{CC} = 5.0 VDC.

Atmel's 27LV256R has additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages. The AT27LV256R programs identically as an AT27C256R.

Erasure Characteristics

The entire memory array of the AT27LV256R is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 µW/cm^2 intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 W·sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +125°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Voltage on A9 with Respect to Ground	-2.0 V to +14.0 V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0 V to +14.0 V(1)
Integrated UV Erase Dose	7258 W•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75 V dc which may be exceeded if certain precautions are observed (consult application notes) and which may overshoot to +7.0 V for pulses of less than 20 ns.

Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	Ai	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	Ai	V_{CC}	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X(1)	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X(5)	V_{CC}	V_{CC}	High Z
Rapid Program(2)	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC}	D_{IN}
PGM Verify(2)	X	V_{IL}	Ai	V_{PP}	V_{CC} (2)	D_{OUT}
Optional PGM Verify(2)	V_{IL}	V_{IL}	Ai	V_{CC}	V_{CC} (2)	D_{OUT}
PGM Inhibit(2)	V_{IH}	V_{IH}	X	V_{PP}	V_{CC} (2)	High Z
Product Identification(2),(4)	V_{IL}	V_{IL}	A9=V_H (3) A0=V_{IH} or V_{IL} A1-A14=V_{IL}	V_{CC}	V_{CC} (2)	Identification Code

Notes:
1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics. Programming modes require V_{CC} > 4.5 V.
3. V_H = 12.0 ± 0.5 V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.
5. Standby V_{CC} Current (I_{SB}) is specified with V_{PP}=V_{CC}. V_{CC} > V_{PP} will cause a slight increase in I_{SB}.

D.C. and A.C. Operating Conditions for Read Operation

		AT27LV256R	
		-20	-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		3.0 V to 5.5 V	3.0 V to 5.5 V

4

D.C. and Operating Characteristics for Read Operation

(V_{CC} = 3.0V to 5.5V unless otherwise specified)

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1 V to V_{CC}+1 V			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1 V to V_{CC}+0.1 V			10	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}-0.7 V to V_{CC}+0.3 V			10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC}-0.3 to V_{CC}+1.0 V			100	µA
		I_{SB2} (TTL), $\overline{CE}$=2.0 to V_{CC}+1.0V			1	mA
I_{CC}	V_{CC} Active Current	I_{CC1} f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}, V_{CC} = 5.5 V	Com.		20	mA
			Ind.		25	mA
		I_{CC2} f = 1 MHz, I_{OUT} = 0 mA $\overline{CE}$ = V_{IL}, V_{CC} = 3.3 V	Com.		8	mA
			Ind.		10	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC}+0.75	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			.45	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA		V_{CC}-0.3		V
		I_{OH} = -400 µA		2.4		V

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

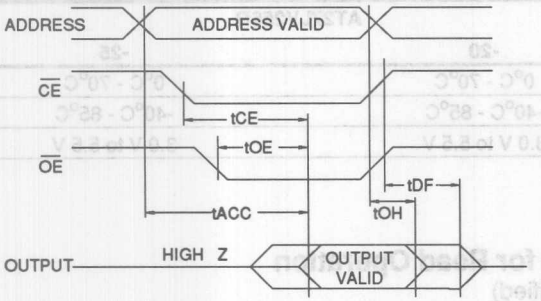
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

A.C. Characteristics for Read Operation (V_{CC} = 3.0 V to 5.5 V)

				AT27LV256R				
				-20		-25		
Symbol	Parameter	Condition		Min	Max	Min	Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Com.		200		250	ns
			Ind.		200		250	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}			200		250	ns
t_{OE} (2,3)	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}			70		100	ns
t_{DF} (4,5)	$\overline{OE}$ High to Output Float	$\overline{CE}$ = V_{IL}			50		50	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		0		0		ns

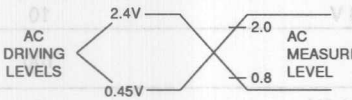
Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

A.C. Waveforms for Read Operation



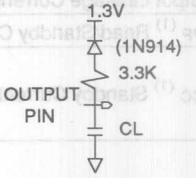
Notes:
1. Timing measurement references are 0.8 V and 2.0 V. Input AC driving levels are 0.45 V and 2.4 V. See Input Test Waveforms and Measurement Levels.
2. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

Input Test Waveforms and Measurement Levels



t_R, t_F < 20 ns (10% to 90%)

Output Test Load



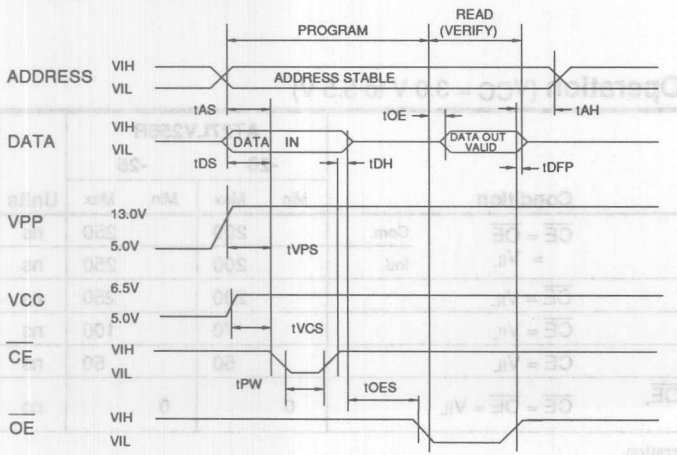
Note: C_L = 100 pF including jig capacitance.

Pin Capacitance (f= 1 MHz, T=25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	8	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Notes: 1. Typical values for 5-V supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms (1)



Notes:
1. The Input Timing Reference is 0.8 V for V_{IL} and 2.0 V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27LV256R a 0.1-µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

D.C. Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25$ V, $V_{PP} = 13.0 \pm 0.25$ V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	$V_{CC}+1$	V
V_{OL}	Output Low Volt.	$I_{OL}=2.1$ mA		.45	V
V_{OH}	Output High Volt.	$I_{OH}=-400$ µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			25	mA
I_{PP2}	V_{PP} Current	$\overline{CE}=V_{IL}$		25	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25$ V, $V_{PP} = 13.0 \pm 0.25$ V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Limits Max	Units
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CE}$ Program Pulse Width	(Note 3)	95	105	µs
t_{OE}	Data Valid from $\overline{OE}$	(Note 2)		150	ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) ..... 20 ns
Input Pulse Levels ..... 0.45 V to 2.4 V
Input Timing Reference Level ..... 0.8 V to 2.0 V
Output Timing Reference Level ..... 0.8 V to 2.0 V

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100 µsec ±5%.

Atmel's 27LV256R Integrated Product Identification Code[1]

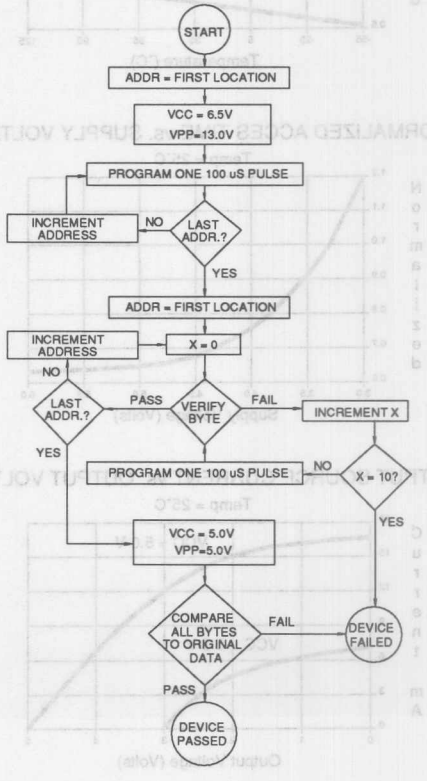
Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	1	0	0	0	1	1	0	0	8C

Note: 1. The AT27LV256R has the same Product Identification Code as the AT27C256R. Both are programming compatible.

4

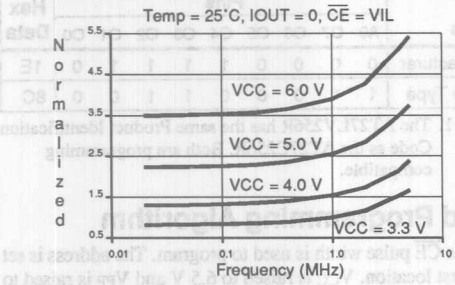
Rapid Programming Algorithm

A 100 µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5 V and V_{PP} is raised to 13.0 V. Each address is first programmed with one 100 µs $\overline{CE}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0 V and V_{CC} to 5.0 V. All bytes are read again and compared with the original data to determine if the device passes or fails.

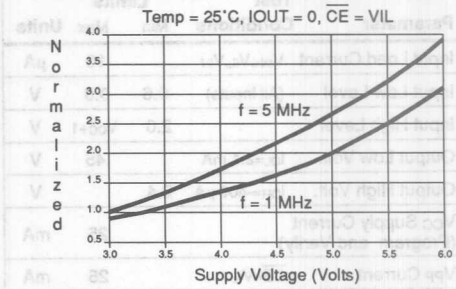


LV EPROM Product Characteristics

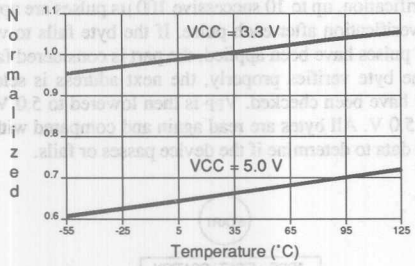
NORMALIZED SUPPLY CURRENT vs. FREQUENCY



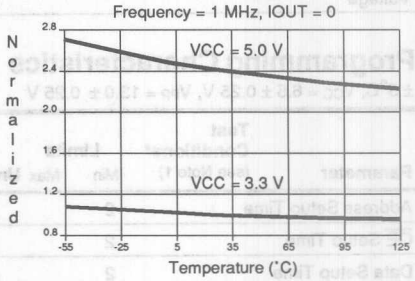
NORMALIZED SUPPLY CURRENT vs. VOLTAGE



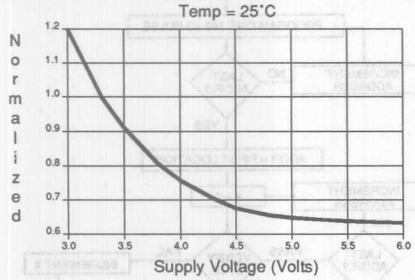
NORMALIZED ACCESS TIME vs. TEMPERATURE



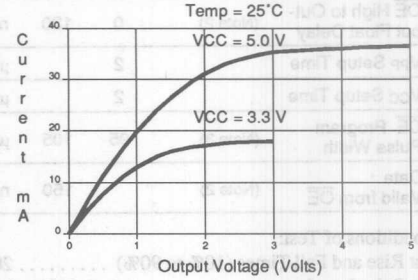
NORMALIZED SUPPLY CURRENT vs. TEMP.



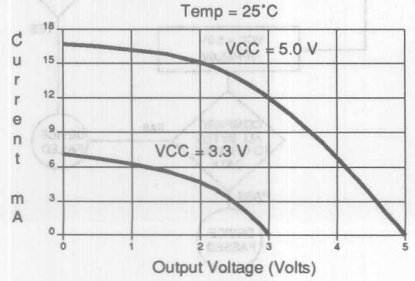
NORMALIZED ACCES TIME vs. SUPPLY VOLTAGE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



Ordering Information

t_{ACC} (ns)	I_{CC} (mA) V_{CC} = 3.3 V		Ordering Code	Package	Operation Range
	Active	Standby			
200	8	0.1	AT27LV256R-20DC AT27LV256R-20JC AT27LV256R-20KC AT27LV256R-20LC AT27LV256R-20PC AT27LV256R-20RC	28DW6 32J 32KW 32LW 28P6 28R	Commercial (0°C to 70°C)
200	10	0.1	AT27LV256R-20DI AT27LV256R-20KI AT27LV256R-20LI	28DW6 32KW 32LW	Industrial (-40°C to 85°C)
250	8	0.1	AT27LV256R-25DC AT27LV256R-25JC AT27LV256R-25KC AT27LV256R-25LC AT27LV256R-25PC AT27LV256R-25RC	28DW6 32J 32KW 32LW 28P6 28R	Commercial (0°C to 70°C)
250	10	0.1	AT27LV256R-25DI AT27LV256R-25KI AT27LV256R-25LI	28DW6 32KW 32LW	Industrial (-40°C to 85°C)

t_{ACC} (ns)	I_{CC} (mA) V_{CC} = 3.3 V		Ordering Code	Package	Operation Range
	Active	Standby			
200	8	0.1	AT27LV256R-20TC	28T	Commercial (0° to 70°C)
250	8	0.1	AT27LV256R-25TC	28T	Commercial (0° to 70°C)

Package Type	
28DW6	28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32KW	32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
28R	28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline OTP (SOIC)
28T	28 Lead, Plastic Thin Small Outline Package OTP (TSOP)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA) V_{CC} = 3.3 V Active	Standby	Ordering Code	Package	Operation Range
200	8	0.1	AT27LV256R-20DC AT27LV256R-20JC AT27LV256R-20KC AT27LV256R-20LC AT27LV256R-20PC AT27LV256R-20RC	28DW6 32J 32KW 32LW 28P6 28R	Commercial (0°C to 70°C)
200	10	0.1	AT27LV256R-20DI AT27LV256R-20KI AT27LV256R-20LI	28DW6 32KW 32LW	Industrial (-40°C to 85°C)
250	8	0.1	AT27LV256R-25DC AT27LV256R-25JC AT27LV256R-25KC AT27LV256R-25LC AT27LV256R-25PC AT27LV256R-25RC	28DW6 32J 32KW 32LW 28P6 28R	Commercial (0°C to 70°C)
250	10	0.1	AT27LV256R-25DI AT27LV256R-25KI AT27LV256R-25LI	28DW6 32KW 32LW	Industrial (-40°C to 85°C)

t_{ACC} (ns)	I_{CC} (mA) V_{CC} = 3.3 V Active	Standby	Ordering Code	Package	Operation Range
200	8	0.1	AT27LV256R-20TC	28T	Commercial (0° to 70°C)
250	8	0.1	AT27LV256R-25TC	28T	Commercial (0° to 70°C)

Package Type	
28DW6	28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32KW	32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
28R	28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline OTP (SOIC)
28T	28 Lead, Plastic Thin Small Outline Package OTP (TSOP)

Features

- **Bipolar Speed in JEDEC Standard EPROM Pinout**
  - **Read Access Time - 55 ns**
  - **28-Lead 600 mil CERDIP and OTP Plastic DIP**
  - **32-Pad LCC and JLCC**
- **Low Power CMOS Operation**
  - **50 mA max. Active at 10 MHz**
- **High Output Drive Capability**
- **High Reliability Latch-Up Resistant CMOS Technology**
- **Rapid Programming - 100 µs/byte (typical)**
- **Two-line Control**
- **CMOS and TTL Compatible Inputs and Outputs**
- **Integrated Product Identification Code**
- **Full Military, Industrial and Commercial Temperature Ranges**

256K (32K x 8) High Speed UV Erasable CMOS EPROM

Description

The AT27HC256R is a high-speed, low-power 262,144 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized as 32K x 8 bits. The AT27HC256R is suited for very high-speed applications, and requires only one 5 V power supply in normal read mode operation. Any byte can be accessed in less than 55 ns on the AT27HC256R, making this part ideal for high-performance systems. Power consumption is typically only 35 mA in Active Mode, and less than 15 mA in Standby Mode.

Atmel's high-speed CMOS technology provides optimum speed, lower power and high noise immunity. The high-speed CMOS process is an extension of Atmel's high quality and highly manufacturable floating poly EPROM technology.

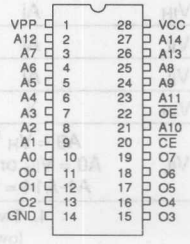
Pin Configurations

Pin Name	Function
A0-A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
NC	No Connect
O0-O7	Outputs

LCC, JLCC
Top View



DIP
Top View



Description (Continued)

The AT27HC256R comes in a choice of industry standard JEDEC-approved packages including: 28-pin DIP ceramic, 32-pad ceramic leadless chip carrier (LCC), and 32-lead ceramic (JLCC). The device features two-line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

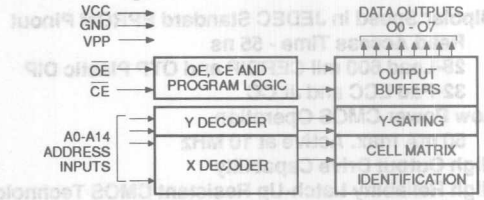
With a storage capacity of 32K bytes, Atmel's 27HC256R allows firmware to be stored reliably and to be accessed at very high speeds. The AT27HC256R has exceptional output drive capability — source 4 mA and sink 16 mA per output.

The AT27HC256R has additional features to ensure high-quality and efficient production use. The Rapid programming algorithm reduces the time required to program the chip and guarantees reliable programming. The Integrated Product Identification Code electronically identifies the device and manufacturing origin. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Erasure Characteristics

The entire memory array of the AT27HC256R is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 $W \cdot sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Voltage on A9 with Respect to Ground	-2.0 V to +14.0 V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0 V to +14.0 V(1)
Integrated UV Erase Dose	7258 W•sec/cm²

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} +0.75 V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	Ai	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	Ai	V_{CC}	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X(1)	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Rapid Program(2)	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC}	D_{IN}
PGM Verify(2)	X	V_{IL}	Ai	V_{PP}	V_{CC}	D_{OUT}
Optional PGM Verify(2)	V_{IL}	V_{IL}	Ai	V_{CC}	V_{CC}	D_{OUT}
PGM Inhibit(2)	V_{IH}	V_{IH}	X	V_{PP}	V_{CC}	High Z
Product Identification(4)	V_{IL}	V_{IL}	A9 = V_H (3) A0 = V_{IH} or V_{IL} A1-A14 = V_{IL}	V_{CC}	V_{CC}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. $V_H = 12.0 \pm 0.5$ V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

D.C. and A.C. Operating Conditions for Read Operation

		AT27HC256R	
		-55	-70
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%

D.C. and Operating Characteristics for Read Operation

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1 V to V_{CC} + 1 V			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1 V to V_{CC} + 0.1 V			10	µA
I_{PP} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = 3.8 to V_{CC}+0.3 V			20	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS) $\overline{CE}$ = V_{CC}-0.3 to V_{CC}+1.0 V			30	mA
		I_{SB2} (TTL) $\overline{CE}$ = 2.0 to V_{CC}+1.0 V			35	mA
I_{CC}	V_{CC} Active Current	f = 10 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}	Com.		50	mA
			Ind.,Mil.		55	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC}+0.75	V
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			.45	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA		V_{CC}-0.3		V
		I_{OH} = -2.5 mA		3.5		V
		I_{OH} = -4.0 mA		2.4		V
V_{PP}	V_{PP} Read Voltage	V_{CC} = 5 ± 0.5 V		3.8	V_{CC}+0.3	V

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

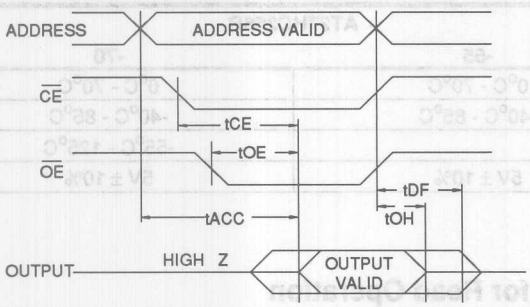
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

A.C. Characteristics for Read Operation

				AT27HC256R				
				-55		-70		
Symbol	Parameter	Condition		Min	Max	Min	Max	Units
t_{ACC} (4)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Com.,Ind.		55		70	ns
			Mil.				70	ns
t_{CE} (3)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}			55		70	ns
t_{OE} (3,4)	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}			25		30	ns
t_{DF} (2,5)	$\overline{OE}$ or $\overline{CE}$ High to Output Float	$\overline{CE}$ = V_{IL}			25		30	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		0		0		ns

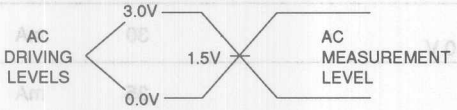
Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation

A.C. Waveforms for Read Operation [1]



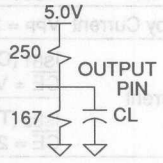
Notes:
1. Timing measurement reference is 1.5 V. Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified. C_L = 30 pF, add 10 ns for C_L = 100 pF.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first. t_{DF} is measured at V_{OH}-0.5 V or V_{OL}+0.5 V with C_L = 5 pF.
3. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
5. This parameter is only sampled and is not 100% tested.

Input Test Waveforms and Measurement Levels



t_R, t_F < 5 ns (10% to 90%)

Output Test Load



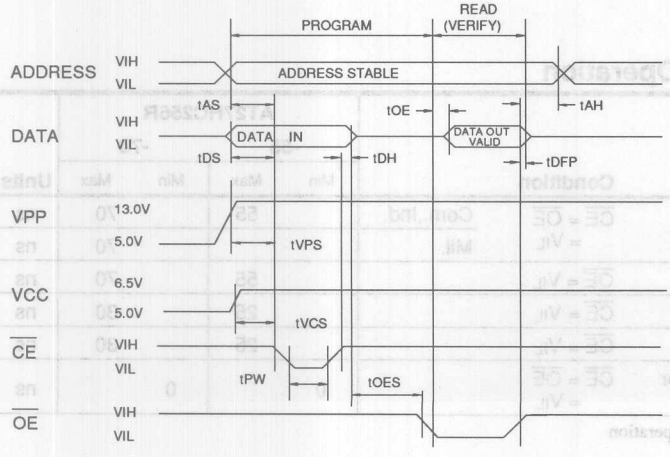
Note: C_L = 30 pF including jig capacitance.

Pin Capacitance (f = 1MHz, T= 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes:
1. Timing measurement reference is 1.5 V. Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27HC256R a 0.1-µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

D.C. Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25$ V, $V_{PP} = 13.0 \pm 0.25$ V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	$V_{CC}+1$	V
V_{OL}	Output Low Volt.	I_{OL} = 16 mA		.45	V
V_{OH}	Output High Volt.	I_{OH} =-4.0 mA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			60	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE} = V_{IL}$		30	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25$ V, $V_{PP} = 13.0 \pm 0.25$ V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Limits Max	Units
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CE}$ Program Pulse Width	(Note 3)	95	105	µs
t_{OE}	Data Valid from $\overline{OE}$			150	ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) ..... 5 ns
Input Pulse Levels ..... 0.0 V to 3.0 V
Input Timing Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V

Notes:

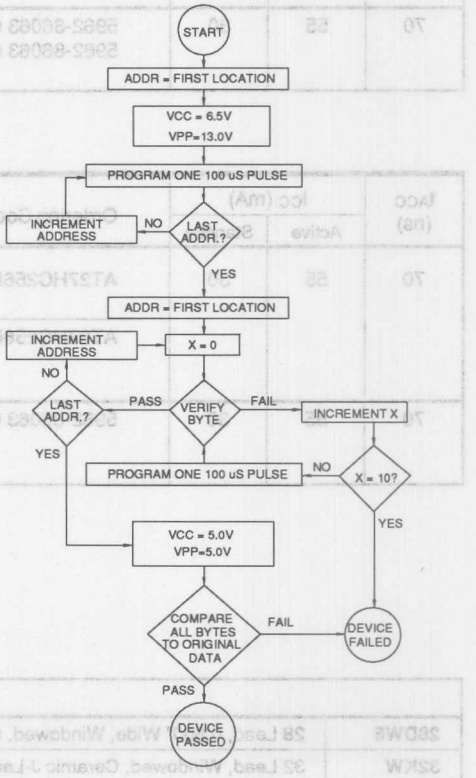
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100 µsec ±5%.

Atmel's 27HC256R Integrated Product Identification Code

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	1	0	0	1	0	1	0	0	94

Rapid Programming Algorithm

A 100 µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5 V and V_{PP} is raised to 13.0 V. Each address is first programmed with one 100 µs $\overline{CE}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0 V and V_{CC} to 5.0 V. All bytes are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
55	50	30	AT27HC256R-55DC AT27HC256R-55KC AT27HC256R-55LC	28DW6 32KW 32LW	Commercial (0°C to 70°C)
55	55	30	AT27HC256R-55DI AT27HC256R-55KI AT27HC256R-55LI	28DW6 32KW 32LW	Industrial (-40°C to 85°C)
70	50	30	AT27HC256R-70DC AT27HC256R-70KC AT27HC256R-70LC	28DW6 32KW 32LW	Commercial (0°C to 70°C)
70	55	30	AT27HC256R-70DI AT27HC256R-70KI AT27HC256R-70LI	28DW6 32KW 32LW	Industrial (-40°C to 85°C)
			AT27HC256R-70DM AT27HC256R-70LM	28DW6 32LW	Military (-55°C to 125°C)
			AT27HC256R-70DM/883 AT27HC256R-70LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
70	55	30	5962-86063 08 XX 5962-86063 08 YX	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	55	30	AT27HC256R-70KM	32KW	Military (-55°C to 125°C)
			AT27HC256R-70KM	32KW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
70	55	30	5962-86063 08 ZX	32KW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
28DW6	28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32KW	32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)

512K (64K x 8) UV Erasable CMOS EPROM

Features

- Fast Read Access Time - 90 ns
- Low Power CMOS Operation
  - 100 µA max. Standby
  - 20 mA max. Active at 5 MHz
- Wide Selection of JEDEC Standard Packages
  - 28-Lead 600-mil Cerdip and OTP Plastic DIP, SOIC, or TSOP
  - 32-Pad LCC, 32-Lead JLCC and OTP PLCC
- 5 V ± 10% Supply
- High Reliability CMOS Technology
  - 2000 V ESD Protection
  - 200 mA Latchup Immunity
- Rapid Programming - 100 µs/byte (typical)
- Two-line Control
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Military, Commercial and Industrial Temperature Ranges

Description

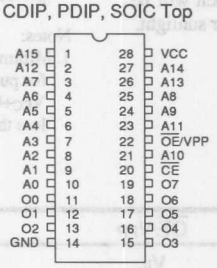
The AT27C512R chip is a low-power, high performance 524,288 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized 64K x 8. It requires only one 5 V power supply in normal read mode operation. Any byte can be accessed in less than 90 ns, eliminating the need for speed reducing WAIT states on high performance microprocessor systems.

Atmel's scaled CMOS technology provides high speed, lower active power consumption, and significantly faster programming. Power consumption is typically only 8 mA in Active Mode and less than 10 µA in Standby.

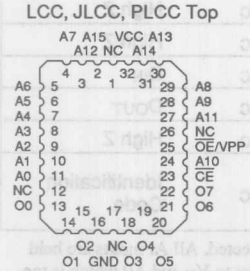
Pin Configurations

Pin Name	Function
A0-A15	Addresses
O0-O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$ /V_{PP}	Output Enable
NC	No Connect

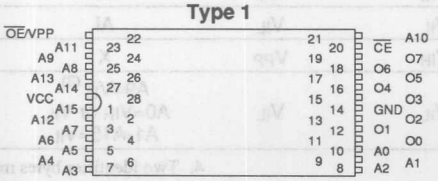
CDIP, PDIP, SOIC Top



LCC, JLCC, PLCC Top



TSOP Top View
Type 1



Note: PLCC Package Pins 1 and 17 are DON'T CONNECT.

Description (Continued)

The AT27C512R comes in a choice of industry standard JEDEC-approved packages including; 28-pin windowed ceramic DIP, 28-pin one time programmable (OTP) plastic DIP, 28-pin OTP gull-wing small outline IC (SOIC), 28-pin OTP thin small outline package (TSOP), 32-pad windowed ceramic leadless chip carrier (LCC), 32-lead windowed J-leaded chip carrier (JLCC), and 32-lead OTP plastic J-leaded chip carrier (PLCC). All devices feature two line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

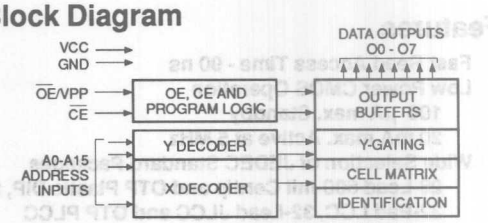
With high density 64K byte storage capability, the AT27C512R allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's 27C512R has additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Erasure Characteristics

The entire memory array of the AT27C512R is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 µW/cm^2 intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 W·sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Voltage on A9 with Respect to Ground	-2.0 V to +14.0 V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0 V to +14.0 V(1)
Integrated UV Erase Dose	7258 W•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC}+0.75 V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}/V_{PP}$	Ai	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	Ai	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X(1)	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	High Z
Rapid Program(2)	V_{IL}	V_{PP}	Ai	V_{CC}	D_{IN}
PGM Verify	V_{IL}	V_{IL}	Ai	V_{CC}	D_{OUT}
PGM Inhibit	V_{IH}	V_{PP}	X	V_{CC}	High Z
Product Identification(4)	V_{IL}	V_{IL}	A9=V_H (3) A0=V_{IH} or V_{IL} A1-A15=V_{IL}	V_{CC}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. V_H = 12.0 ± 0.5 V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

D.C. and A.C. Operating Conditions for Read Operation

		AT27C512R				
		-90	-12	-15	-20	-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 10%	5 V ± 10%	5 V ± 10%	5 V ± 10%	5 V ± 10%

4

D.C. and Operating Characteristics for Read Operation

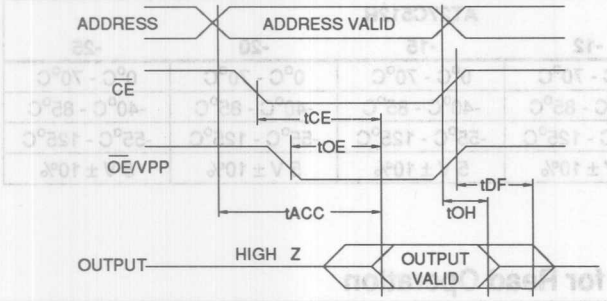
Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1 V to V_{CC}+1 V			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1 V to V_{CC}+0.1 V			10	µA
I_{SB}	V_{CC} [1] Standby Current	I_{SB1} (CMOS) $\overline{CE}$ = V_{CC}-0.3 to V_{CC}+1.0 V	Com.		100	µA
			Ind.,Mil.		200	µA
		I_{SB2} (TTL) $\overline{CE}$ = 2.0 to V_{CC}+1.0 V	Com.		1	mA
			Ind.,Mil.		2	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}	Com.		20	mA
			Ind.,Mil.		25	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC}+0.75	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			.45	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA		V_{CC}-0.3		V
		I_{OH} = -2.5 mA		3.5		V
		I_{OH} = -400 µA		2.4		V

Notes: 1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$, and removed simultaneously or after $\overline{OE}/V_{PP}$.

A.C. Characteristics for Read Operation

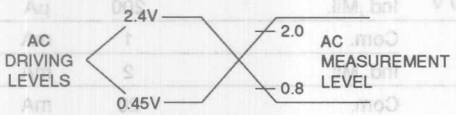
			AT27C512R									
			-90		-12		-15		-20		-25	
Symbol	Parameter	Condition	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{ACC} [4]	Address to Output Delay	$\overline{CE}$ = $\overline{OE}/V_{PP}$ = VIL		90		120		150		200		250	ns
t_{CE} [3]	$\overline{CE}$ to Output Delay	$\overline{OE}/V_{PP}$ = V_{IL}		90		120		150		200		250	ns
t_{OE} [3,4]	$\overline{OE}/V_{PP}$ to Output Delay	$\overline{CE}$ = V_{IL}		40		50		60		75		100	ns
t_{DF} [2,5]	$\overline{OE}/V_{PP}$ or $\overline{CE}$ High to Output Float	$\overline{CE}$ = V_{IL}		30		30		50		55		60	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}/V_{PP}$, whichever occurred first	$\overline{CE}$ = $\overline{OE}/V_{PP}$ = V_{IL}	0		0		0		0		0		ns

Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.



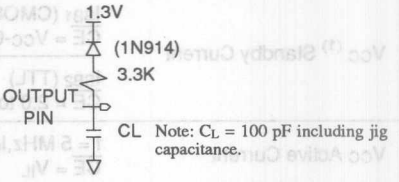
Notes:
1. Timing measurement references are 0.8 V and 2.0 V. Input AC driving levels are 0.45 V and 2.4 V, unless otherwise specified.
2. t_{DF} is specified from $\overline{OE}$ /V_{PP} or $\overline{CE}$, whichever occurs first. Output float is defined as the point when data is no longer driven.
3. $\overline{OE}$/V_{PP} may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. $\overline{OE}$ /V_{PP} may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
5. This parameter is only sampled and is not 100% tested.

Input Test Waveforms and Measurement Levels



t_R, t_F < 20ns (10% to 90%)

Output Test Load



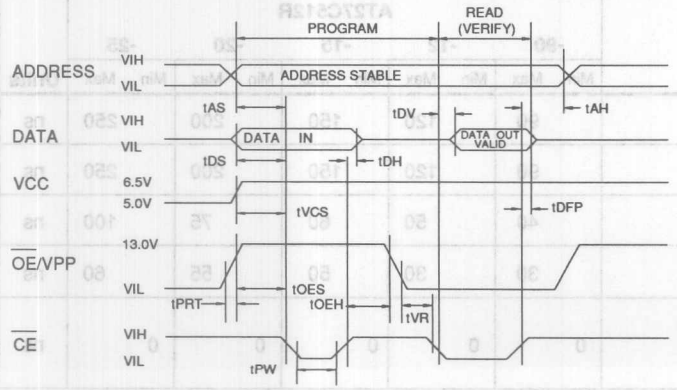
Note: C_L = 100 pF including jig capacitance.

Pin Capacitance (f = 1 MHz T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes:
1. The Input Timing Reference is 0.8 V for V_{IL} and 2.0 V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

D.C. Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25V$, $\overline{OE}/V_{PP} = 13.0 \pm 0.25V$

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	$V_{CC}+1$	V
V_{OL}	Output Low Volt.	$I_{OL}=2.1$ mA		.45	V
V_{OH}	Output High Volt.	$I_{OH}=-400$ µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			25	mA
I_{PP2}	$\overline{OE}/V_{PP}$ Current	$\overline{CE}=V_{IL}$		25	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25V$, $\overline{OE}/V_{PP} = 13.0 \pm 0.25V$

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Limits Max	Units
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time		2		µs
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{CE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CE}$ Program Pulse Width	(Note 3)	95	105	µs
t_{DV}	Data Valid from $\overline{CE}$	(Note 2)		1	µs
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time		2		µs
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time During Programming		50		ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) ..... 20 ns
Input Pulse Levels ..... 0.45 V to 2.4 V
Input Timing Reference Level ..... 0.8 V to 2.0 V
Output Timing Reference Level ..... 0.8 V to 2.0 V

Notes:

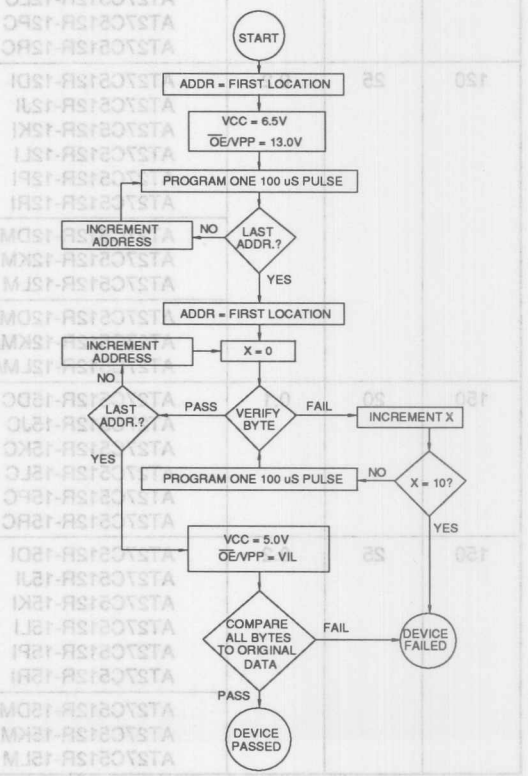
1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100 µsec ± 5%.

Atmel's 27C512R Integrated Product Identification Code

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	0	0	0	0	1	1	0	1	0D

Rapid Programming Algorithm

A 100 µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and $\overline{OE}/V_{PP}$ is raised to 13.0 V. Each address is first programmed with one 100 µs $\overline{CE}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. $\overline{OE}/V_{PP}$ is then lowered to V_{IL} and V_{CC} to 5.0 V. All bytes are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	20	0.1	AT27C512R-90DC	28DW6	Commercial (0°C to 70°C)
			AT27C512R-90JC	32J	
			AT27C512R-90KC	32KW	
			AT27C512R-90LC	32LW	
			AT27C512R-90PC	28P6	
			AT27C512R-90RC	28R	
90	25	0.2	AT27C512R-90DI	28DW6	Industrial (-40°C to 85°C)
			AT27C512R-90JI	32J	
			AT27C512R-90KI	32KW	
			AT27C512R-90LI	32LW	
			AT27C512R-90PI	28P6	
			AT27C512R-90RI	28R	
			AT27C512R-90DM	28DW6	Military (-55°C to 125°C)
			AT27C512R-90KM	32KW	
			AT27C512R-90LM	32LW	
120	20	0.1	AT27C512R-12DC	28DW6	Commercial (0°C to 70°C)
			AT27C512R-12JC	32J	
			AT27C512R-12KC	32KW	
			AT27C512R-12LC	32LW	
			AT27C512R-12PC	28P6	
			AT27C512R-12RC	28R	
120	25	0.2	AT27C512R-12DI	28DW6	Industrial (-40°C to 85°C)
			AT27C512R-12JI	32J	
			AT27C512R-12KI	32KW	
			AT27C512R-12LI	32LW	
			AT27C512R-12PI	28P6	
			AT27C512R-12RI	28R	
			AT27C512R-12DM	28DW6	Military (-55°C to 125°C)
			AT27C512R-12KM	32KW	
			AT27C512R-12LM	32LW	
			AT27C512R-12DM/883	28DW6	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			AT27C512R-12KM/883	32KW	
			AT27C512R-12LM/883	32LW	
150	20	0.1	AT27C512R-15DC	28DW6	Commercial (0°C to 70°C)
			AT27C512R-15JC	32J	
			AT27C512R-15KC	32KW	
			AT27C512R-15LC	32LW	
			AT27C512R-15PC	28P6	
			AT27C512R-15RC	28R	
150	25	0.2	AT27C512R-15DI	28DW6	Industrial (-40°C to 85°C)
			AT27C512R-15JI	32J	
			AT27C512R-15KI	32KW	
			AT27C512R-15LI	32LW	
			AT27C512R-15PI	28P6	
			AT27C512R-15RI	28R	
			AT27C512R-15DM	28DW6	Military (-55°C to 125°C)
			AT27C512R-15KM	32KW	
			AT27C512R-15LM	32LW	

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	25	0.2	AT27C512R-15DM/883 AT27C512R-15KM/883 AT27C512R-15LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	20	0.1	AT27C512R-20DC AT27C512R-20JC AT27C512R-20KC AT27C512R-20LC AT27C512R-20PC AT27C512R-20RC	28DW6 32J 32KW 32LW 28P6 28R	Commercial (0°C to 70°C)
200	25	0.2	AT27C512R-20DI AT27C512R-20JI AT27C512R-20KI AT27C512R-20LI AT27C512R-20PI AT27C512R-20RI	28DW6 32J 32KW 32LW 28P6 28R	Industrial (-40°C to 85°C)
			AT27C512R-20DM AT27C512R-20KM AT27C512R-20LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C512R-20DM/883 AT27C512R-20KM/883 AT27C512R-20LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	20	0.1	AT27C512R-25DC AT27C512R-25JC AT27C512R-25KC AT27C512R-25LC AT27C512R-25PC AT27C512R-25RC	28DW6 32J 32KW 32LW 28P6 28R	Commercial (0°C to 70°C)
250	25	0.2	AT27C512R-25DI AT27C512R-25JI AT27C512R-25KI AT27C512R-25LI AT27C512R-25PI AT27C512R-25RI	28DW6 32J 32KW 32LW 28P6 28R	Industrial (-40°C to 85°C)
			AT27C512R-25DM AT27C512R-25KM AT27C512R-25LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C512R-25DM/883 AT27C512R-25KM/883 AT27C512R-25LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	25	0.2	5962-87648 04 XX 5962-87648 04 YX 5962-87648 04 ZX	28DW6 32LW 32KW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	25	0.2	5962-87648 01 XX 5962-87648 01 YX 5962-87648 01 ZX	28DW6 32LW 32KW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	25	0.2	5962-87648 02 XX 5962-87648 02 YX 5962-87648 02 ZX	28DW6 32LW 32KW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

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t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
250	25	0.2	5962-87648 03 XX 5962-87648 03 YX 5962-87648 03 ZX	28DW6 32LW 32KW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	20	0.1	AT27C512R-90TC	28T	Commercial (0° to 70°C)
120	20	0.1	AT27C512R-120TC	28T	Commercial (0° to 70°C)
150	20	0.1	AT27C512R-150TC	28T	Commercial (0° to 70°C)

Package Type	
28DW6	28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32KW	32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
28R	28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline OTP (SOIC)
28T	28 Lead, Thin Small Outline Package OTP (TSOP)

512K (64K x 8) Low Voltage UV Erasable CMOS EPROM

Features

- Wide Power Supply Range, 3.0 VDC to 5.5 VDC
- Compatible with JEDEC Standard AT27C512R
- Low Power 3-Volt CMOS Operation
  - 100 µA max. Standby
  - 26 mW max. Active at 1 MHz for V_{CC} = 3.3 VDC
  - 110 mW max. Active at 5 MHz for V_{CC} = 5.5 VDC
- Read Access Time - 200 ns
- Wide Selection of JEDEC Standard Packages Including OTP
  - 28-Lead, 600-mil Cerdip and OTP Plastic DIP, SOIC or TSOP
  - 32-Pad LCC, 32-Lead JLCC and OTP PLCC
- High Reliability CMOS Technology
  - 2000 V ESD Protection
  - 200 mA Latchup Immunity
- Rapid Programming - 100 µs/byte (typical)
- Two-line Control
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

Description

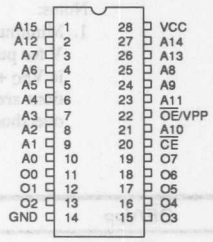
The AT27LV512R chip is a low power, low voltage 524,288 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized as 64K x 8 bits. It requires only one supply in the range of 3.0 to 5.5 VDC in normal read mode operation, making it ideal for battery powered systems.

With a typical power draw of only 18 mW at 1 MHz and V_{CC} at 3.3 VDC, the AT27LV512R will draw less than one fifth the power of a standard 5-volt EPROM. Standby mode supply current is typically less than 10 µA.

Pin Configurations

Pin Name	Function
A0-A15	Addresses
O0-O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$ /V_{PP}	Output Enable
NC	No Connect

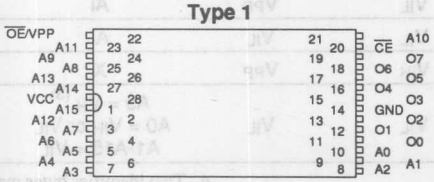
CDIP, PDIP, SOIC Top View



LCC, JLCC, PLCC Top View



TSOP Top View
Type 1



Note: PLCC Package Pins 1 and 17 are DON'T CONNECT.

Description (Continued)

The AT27LV512R comes in a choice of industry standard JEDEC-approved through hole and surface mount packages including windowed and one time programmable (OTP) packages, such as the OTP thin small outline package (TSOP). All devices feature two line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

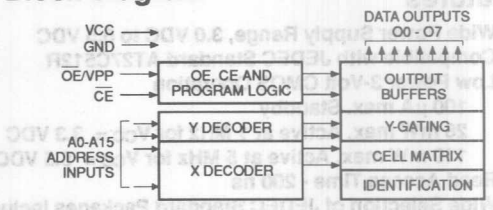
The AT27LV512R operating with V_{CC} at 3.0 VDC produces TTL level outputs that are compatible with standard TTL logic devices operating at V_{CC} = 5.0 VDC.

Atmel's 27LV512R has additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages. The AT27LV512R programs identically as an AT27C512R.

Erasure Characteristics

The entire memory array of the AT27LV512R is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 µW/cm^2 intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 W·sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +125°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Voltage on A9 with Respect to Ground	-2.0 V to +14.0 V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0 V to +14.0 V(1)
Integrated UV Erase Dose	7258 W•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75 V dc which may be exceeded if certain precautions are observed (consult application notes) and which may overshoot to +7.0 V for pulses of less than 20 ns.

Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}$/V_{PP}	Ai	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	Ai	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X(1)	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	High Z
Rapid Program(2)	V_{IL}	V_{PP}	Ai	V_{CC} (2)	D_{IN}
PGM Verify (2)	V_{IL}	V_{IL}	Ai	V_{CC} (2)	D_{OUT}
PGM Inhibit (2)	V_{IH}	V_{PP}	X	V_{CC} (2)	High Z
Product Identification(2),(4)	V_{IL}	V_{IL}	A9 = V_H (3) A0 = V_{IH} or V_{IL} A1-A15 = V_{IL}	V_{CC} (2)	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics. Programming modes require V_{CC} > 4.5 V.
3. V_H = 12.0 ± 0.5 V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

D.C. and A.C. Operating Conditions for Read Operation

		AT27LV512R	
		-20	-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		3.0 V to 5.5 V	3.0 V to 5.5 V

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D.C. and Operating Characteristics for Read Operation

(V_{CC} = 3.0 V to 5.5 V unless otherwise specified)

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1 V to V_{CC}+1 V			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1 V to V_{CC}+0.1 V			10	µA
I_{SB}	V_{CC} [1] Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC}-0.3 to V_{CC}+1.0 V			100	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC}+1.0 V			1	mA
I_{CC}	V_{CC} Active Current	I_{CC1} f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}, V_{CC} = 5.5 V	Com.		20	mA
			Ind.		25	mA
		I_{CC2} f = 1 MHz, I_{OUT} = 0 mA $\overline{CE}$ = V_{IL}, V_{CC} = 3.3 V	Com.		8	mA
			Ind.		10	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC}+0.75	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			.45	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA		V_{CC}-0.3		V
		I_{OH} = -400 µA		2.4		V

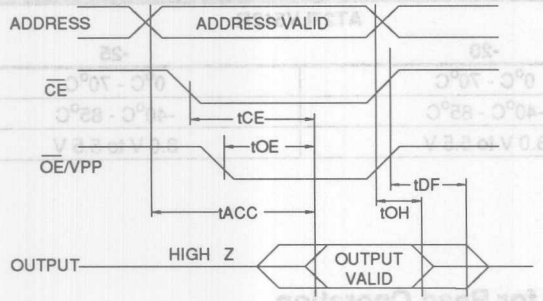
Notes: 1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$, and removed simultaneously or after $\overline{OE}/V_{PP}$.

A.C. Characteristics for Read Operation (V_{CC} = 3.0 V to 5.5 V)

				AT27LV512R				
				-20		-25		
Symbol	Parameter	Condition		Min	Max	Min	Max	Units
t_{ACC} [3]	Address to Output Delay	$\overline{CE}$ = $\overline{OE}/V_{PP}$ = V_{IL}	Com.		200		250	ns
			Ind.		200		250	ns
t_{CE} [2]	$\overline{CE}$ to Output Delay	$\overline{OE}/V_{PP}$ = V_{IL}			200		250	ns
t_{OE} [2,3]	$\overline{OE}/V_{PP}$ to Output Delay	$\overline{CE}$ = V_{IL}			70		100	ns
t_{DF} [4,5]	$\overline{OE}/V_{PP}$ High to Output Float	$\overline{CE}$ = V_{IL}			50		50	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}/V_{PP}$, whichever occurred first	$\overline{CE}$ = $\overline{OE}/V_{PP}$ = V_{IL}		0		0		ns

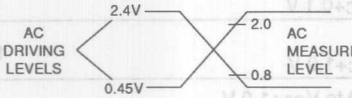
Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

A.C. Waveforms for Read Operation [1]



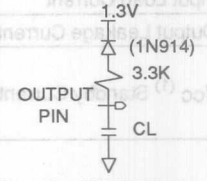
Notes:
1. Timing measurement references are 0.8 V and 2.0 V. Input AC driving levels are 0.45 V and 2.4 V. See Input Test Waveforms and Measurement Levels.
2. $\overline{OE}/V_{PP}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}/V_{PP}$ may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

Input Test Waveforms and Measurement Levels



t_R, t_F < 20 ns (10% to 90%)

Output Test Load



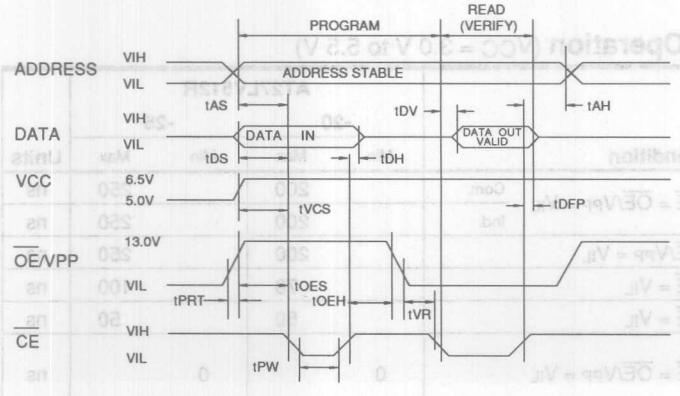
Note: C_L = 100 pF including jig capacitance.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	8	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Notes: 1. Typical values for 5-V supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes:
1. The Input Timing Reference is 0.8 V for V_{IL} and 2.0 V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

D.C. Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25$ V, $\overline{OE}/V_{PP} = 13.0 \pm 0.25$ V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	$V_{CC}+1$	V
V_{OL}	Output Low Volt.	I_{OL} = 2.1 mA		.45	V
V_{OH}	Output High Volt.	I_{OH} = -400 µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			25	mA
I_{PP2}	$\overline{OE}/V_{PP}$ Current	$\overline{CE} = V_{IL}$		25	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25$ V, $\overline{OE}/V_{PP} = 13.0 \pm 0.25$ V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Limits Max	Units
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time		2		µs
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{CE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CE}$ Program Pulse Width	(Note 3)	95	105	µs
t_{DV}	Data Valid from $\overline{CE}$	(Note 2)		1	µs
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time		2		µs
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time During Programming		50		ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) ..... 20 ns
Input Pulse Levels ..... 0.45 V to 2.4 V
Input Timing Reference Level ..... 0.8 V to 2.0 V
Output Timing Reference Level ..... 0.8 V to 2.0 V

Notes:

1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100 µsec±5%.

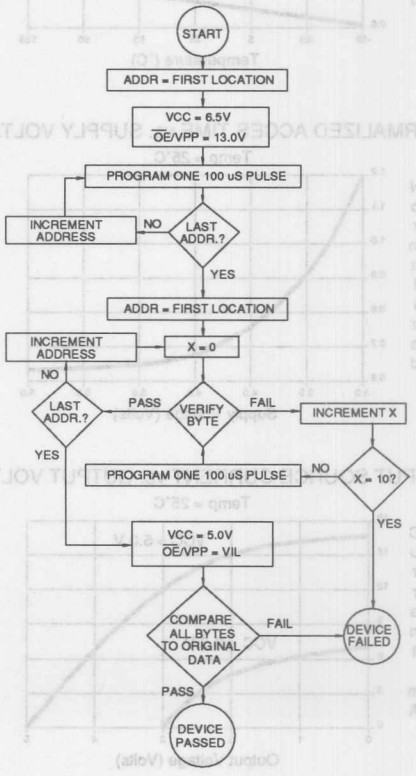
Atmel's 27LV512R Integrated Product Identification Code[1]

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	0	0	0	0	1	1	0	1	0D

Note: 1. The AT27LV512R has the same Product Identification Code as the AT27C512R. Both are programming compatible.

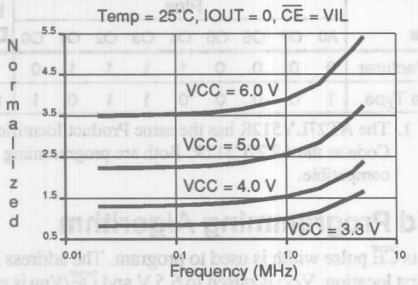
Rapid Programming Algorithm

A 100 µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5 V and $\overline{OE}/V_{PP}$ is raised to 13.0 V. Each address is first programmed with one 100 µs $\overline{CE}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. $\overline{OE}/V_{PP}$ is then lowered to V_{IL} and V_{CC} to 5.0 V. All bytes are read again and compared with the original data to determine if the device passes or fails.

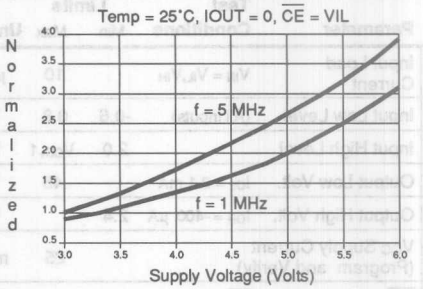


LV EPROM Product Characteristics

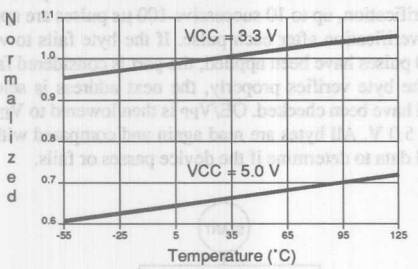
NORMALIZED SUPPLY CURRENT vs. FREQUENCY



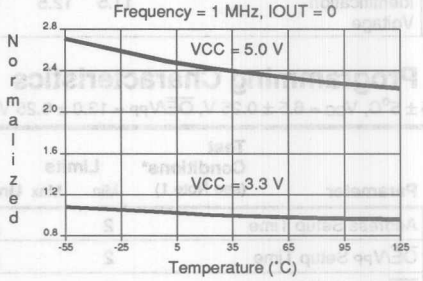
NORMALIZED SUPPLY CURRENT vs. VOLTAGE



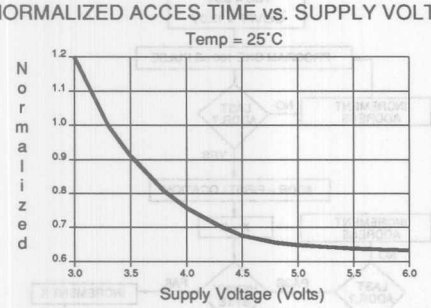
NORMALIZED ACCESS TIME vs. TEMPERATURE



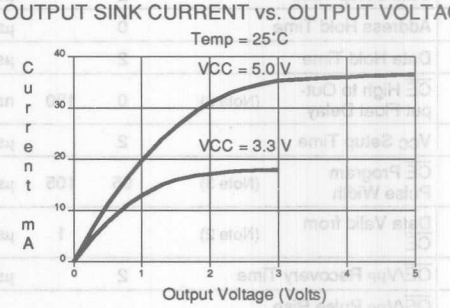
NORMALIZED SUPPLY CURRENT vs. TEMP.



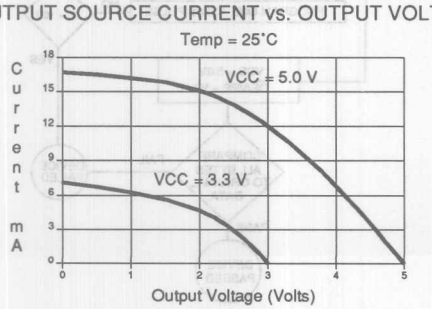
NORMALIZED ACCES TIME vs. SUPPLY VOLTAGE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



Ordering Information

t_{ACC} (ns)	I_{CC} (mA) V_{CC} = 3.3 V		Ordering Code	Package	Operation Range
	Active	Standby			
200	8	0.1	AT27LV512R-20DC AT27LV512R-20JC AT27LV512R-20KC AT27LV512R-20LC AT27LV512R-20PC AT27LV512R-20RC	28DW6 32J 32KW 32LW 28P6 28R	Commercial (0°C to 70°C)
200	10	0.1	AT27LV512R-20DI AT27LV512R-20KI AT27LV512R-20LI	28DW6 32KW 32LW	Industrial (-40°C to 85°C)
250	8	0.1	AT27LV512R-25DC AT27LV512R-25JC AT27LV512R-25KC AT27LV512R-25LC AT27LV512R-25PC AT27LV512R-25RC	28DW6 32J 32KW 32LW 28P6 28R	Commercial (0°C to 70°C)
250	10	0.1	AT27LV512R-25DI AT27LV512R-25KI AT27LV512R-25LI	28DW6 32KW 32LW	Industrial (-40°C to 85°C)

t_{ACC} (ns)	I_{CC} (mA) V_{CC} = 3.3 V		Ordering Code	Package	Operation Range
	Active	Standby			
200	8	0.1	AT27LV512R-20TC	28T	Commercial (0° to 70°C)
250	8	0.1	AT27LV512R-25TC	28T	Commercial (0° to 70°C)

Package Type	
28DW6	28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32KW	32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
28R	28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline OTP (SOIC)
28T	28 Lead, Plastic Thin Small Outline Package OTP (TSOP)

Ordering Code	Package	Operation Range
AT27LV512R-20DC	28DW6	Commercial (0°C to 70°C)
AT27LV512R-20JC	32J	
AT27LV512R-20KC	32KW	
AT27LV512R-20LC	32LW	
AT27LV512R-20PC	28P6	
AT27LV512R-20RC	28R	
AT27LV512R-20DI	28DW6	Industrial (-40°C to 85°C)
AT27LV512R-20KI	32KW	
AT27LV512R-20LI	32LW	
AT27LV512R-25DC	28DW6	Commercial (0°C to 70°C)
AT27LV512R-25JC	32J	
AT27LV512R-25KC	32KW	
AT27LV512R-25LC	32LW	
AT27LV512R-25PC	28P6	
AT27LV512R-25RC	28R	
AT27LV512R-25DI	28DW6	Industrial (-40°C to 85°C)
AT27LV512R-25KI	32KW	
AT27LV512R-25LI	32LW	

Ordering Code	Package	Operation Range
AT27LV512R-20TC	28T	Commercial (0° to 70°C)
AT27LV512R-25TC	28T	Commercial (0° to 70°C)

Package Type	
28DW6	28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32KW	32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
28R	28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline OTP (SOIC)
28T	28 Lead, Plastic Thin Small Outline Package OTP (TSOP)

1 Megabit (128K x 8) UV Erasable CMOS EPROM

Features

- Fast Read Access Time - 100 ns
- Low Power CMOS Operation
  - 100 µA max. Standby
  - 25 mA max. Active at 5 MHz (AT27C010L)
  - 40 mA max. Active at 5 MHz (AT27C010)
- Wide Selection of JEDEC Standard Packages Including OTP
  - 32-Lead 600-mil Cerdip and OTP Plastic DIP, SOIC or TSOP
  - 32-Pad LCC, 32-Lead JLCC and OTP PLCC
- 5 V ± 10% Supply
- High Reliability CMOS Technology
  - 2000 V ESD Protection
  - 200 mA Latchup Immunity
- Rapid Programming - 100 µs/byte (typical)
- Two-line Control
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Full Military, Commercial and Industrial Temperature Ranges

Description

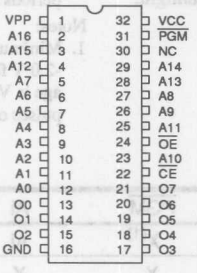
The AT27C010/L chip family is a low-power, high performance 1,048,576 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized as 128K x 8 bits. They require only one 5 V power supply in normal read mode operation. Any byte can be accessed in less than 100 ns, eliminating the need for speed reducing WAIT states on high performance microprocessor systems.

Two power versions are offered. In read mode, the AT27C010 typically consumes 25 mA while the AT27C010L takes only 8 mA. Standby mode supply current for both parts is typically less than 10 µA.

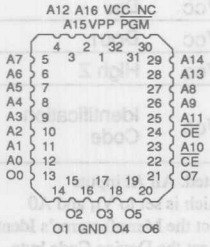
Pin Configurations

Pin Name	Function
A0-A16	Addresses
O0-O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Strobe
NC	No Connect

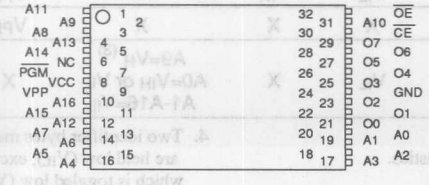
CDIP, PDIP, SOIC Top



LCC, JLCC, PLCC Top



TSOP Top View
Type 1



Description (Continued)

The AT27C010/L comes in a choice of industry standard JEDEC-approved packages including; 32-pin ceramic DIP; 32-pad ceramic leadless chip carrier (LCC); 32-lead ceramic J-leaded chip carrier (JLCC); 32-lead one time programmable (OTP) plastic J-leaded chip carrier (PLCC); 32-pin OTP plastic gull wing small outline IC (SOIC); and 32-pin OTP thin small outline package (TSOP). All devices feature two line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

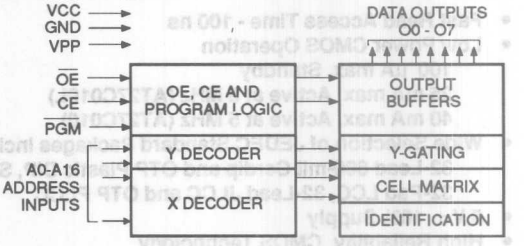
With high density 128K byte storage capability, the AT27C010/L allow firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's 27C010/L have additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Erasure Characteristics

The entire memory array of the AT27C010/L is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 $W \cdot sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Voltage on A9 with Respect to Ground	-2.0 V to +14.0 V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0 V to +14.0 V(1)
Integrated UV Erase Dose	7258 W•sec/cm²

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75 V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	Ai	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X(1)	Ai	X	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	X	X	X	V_{CC}	High Z
Standby	V_{IH}	X	X	X	X	V_{CC}	High Z
Fast Program(2)	V_{IL}	V_{IH}	V_{IL}	Ai	V_{PP}	V_{CC}	D_{IN}
PGM Verify	V_{IL}	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC}	D_{OUT}
PGM Inhibit	V_{IH}	X	X	X	V_{PP}	V_{CC}	High Z
Product Identification(4)	V_{IL}	V_{IL}	X	A9=V_H (3) A0=V_{IH} or V_{IL} A1-A16=V_{IL}	X	V_{CC}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. $V_H = 12.0 \pm 0.5$ V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

D.C. and A.C. Operating Conditions for Read Operation

		AT27C010 / AT27C010L				
		-10	-12	-15	-20	-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.		-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 5%	5 V ± 10%	5 V ± 10%	5 V ± 10%	5 V ± 10%

D.C. and Operating Characteristics for Read Operation

Symbol	Parameter	Condition			Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1 V to V_{CC}+1 V				5	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1 V to V_{CC}+0.1 V				10	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = 3.8 to V_{CC}+0.3 V				10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC}-0.3 to V_{CC}+1.0 V				100	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC}+1.0 V				1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}	AT27C010L	Com.		25	mA
				Ind.,Mil.		30	mA
			AT27C010	Com.		40	mA
				Ind.,Mil.		50	mA
V_{IL}	Input Low Voltage				-0.6	0.8	V
V_{IH}	Input High Voltage				2.0	V_{CC}+0.75	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA				.45	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA			V_{CC}-0.3		V
		I_{OH} = -2.5 mA			3.5		V
		I_{OH} = -400 µA			2.4		V

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

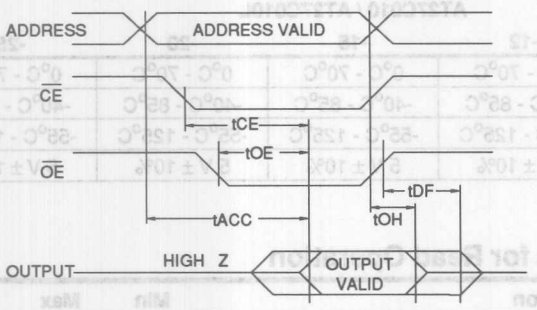
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

A.C. Characteristics for Read Operation

				AT27C010 / AT27C010L										
				-10		-12		-15		-20		-25		
Symbol	Parameter	Condition		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Com.		100		120		150		200		250	ns
			Ind.,Mil.				120		150		200		250	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}			100		120		150		200		250	ns
t_{OE} (2,3)	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}			35		40		40		70		100	ns
t_{DF} (4,5)	$\overline{OE}$ High to Output Float	$\overline{CE}$ = V_{IL}			30		35		40		55		60	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		0		0		0		0		0		ns

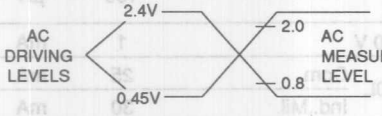
Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

A.C. Waveforms for Read Operation [1]



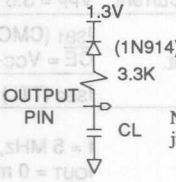
Notes:
1. Timing measurement references are 0.8 V and 2.0 V. Input AC driving levels are 0.45 V and 2.4 V, unless otherwise specified.
2. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

Input Test Waveforms and Measurement Levels



t_R, t_F < 20 ns (10% to 90%)

Output Test Load



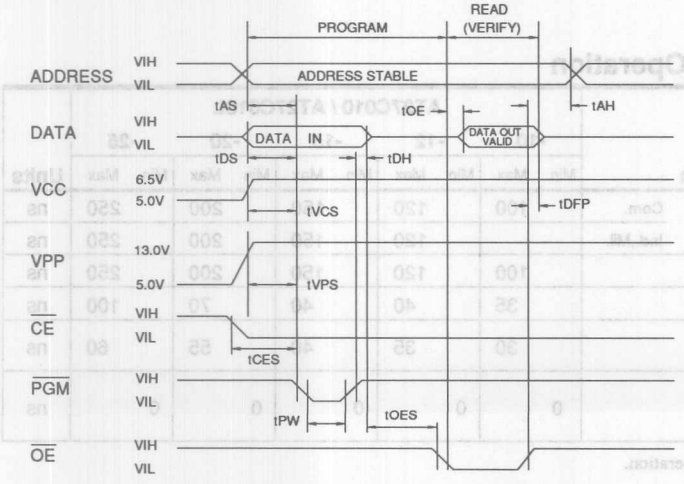
Note: C_L= 100 pF including jig capacitance.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	8	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes:
1. The Input Timing Reference is 0.8 V for V_{IL} and 2.0 V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27C010/L a 0.1-µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

D.C. Programming Characteristics

$T_A = 25 \pm 5^oC$, $V_{CC} = 6.5 \pm 0.25$ V, $V_{PP} = 13.0 \pm 0.25$ V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	$V_{CC}+1$	V
V_{OL}	Output Low Volt.	I_{OL}=2.1 mA		.45	V
V_{OH}	Output High Volt.	I_{OH}=-400 µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			40	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE}=\overline{PGM}=V_{IL}$		20	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

$T_A = 25 \pm 5^oC$, $V_{CC} = 6.5 \pm 0.25$ V, $V_{PP} = 13.0 \pm 0.25$ V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Limits Max	Units
t_{AS}	Address Setup Time		2		µs
t_{CES}	$\overline{CE}$ Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{PGM}$ Program Pulse Width	(Note 3)	95	105	µs
t_{OE}	Data Valid from $\overline{OE}$			150	ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) ..... 20 ns
Input Pulse Levels ..... 0.45 V to 2.4 V
Input Timing Reference Level ..... 0.8 V to 2.0 V
Output Timing Reference Level ..... 0.8 V to 2.0 V

Notes:

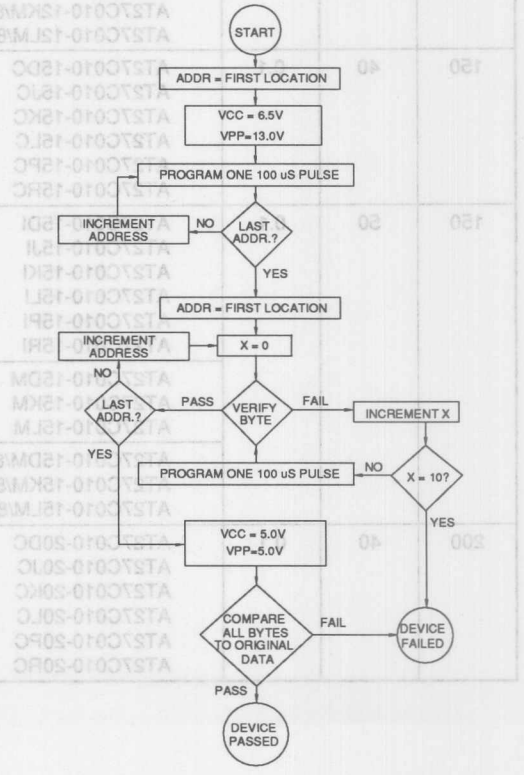
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100 µsec ± 5%.

Atmel's 27C010/L Integrated Product Identification Code

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	0	0	0	0	0	1	0	1	O5

Rapid Programming Algorithm

A 100 µs $\overline{PGM}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5 V and V_{PP} is raised to 13.0 V. Each address is first programmed with one 100 µs $\overline{PGM}$ pulse without verification. Then a verification / reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0 V and V_{CC} to 5.0 V. All bytes are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

tACC (ns)	ICC (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
100	40	0.1	AT27C010-10DC AT27C010-10KC AT27C010-10LC	32DW6 32KW 32LW	Commercial (0°C to 70°C)
120	40	0.1	AT27C010-12DC AT27C010-12JC AT27C010-12KC AT27C010-12LC AT27C010-12PC AT27C010-12RC	32DW6 32J 32KW 32LW 32P6 32R	Commercial (0°C to 70°C)
120	50	0.1	AT27C010-12DI AT27C010-12JI AT27C010-12KI AT27C010-12LI AT27C010-12PI AT27C010-12RI	32DW6 32J 32KW 32LW 32P6 32R	Industrial (-40°C to 85°C)
			AT27C010-12DM AT27C010-12KM AT27C010-12LM	32DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C010-12DM/883 AT27C010-12KM/883 AT27C010-12LM/883	32DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	40	0.1	AT27C010-15DC AT27C010-15JC AT27C010-15KC AT27C010-15LC AT27C010-15PC AT27C010-15RC	32DW6 32J 32KW 32LW 32P6 32R	Commercial (0°C to 70°C)
150	50	0.1	AT27C010-15DI AT27C010-15JI AT27C010-15KI AT27C010-15LI AT27C010-15PI AT27C010-15RI	32DW6 32J 32KW 32LW 32P6 32R	Industrial (-40°C to 85°C)
			AT27C010-15DM AT27C010-15KM AT27C010-15LM	32DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C010-15DM/883 AT27C010-15KM/883 AT27C010-15LM/883	32DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	40	0.1	AT27C010-20DC AT27C010-20JC AT27C010-20KC AT27C010-20LC AT27C010-20PC AT27C010-20RC	32DW6 32J 32KW 32LW 32P6 32R	Commercial (0°C to 70°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
200	50	0.1	AT27C010-20DI AT27C010-20JI AT27C010-20KI AT27C010-20LI AT27C010-20PI AT27C010-20RI	32DW6 32J 32KW 32LW 32P6 32R	Industrial (-40°C to 85°C)
			AT27C010-20DM AT27C010-20KM AT27C010-20LM	32DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C010-20DM/883 AT27C010-20KM/883 AT27C010-20LM/883	32DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	40	0.1	AT27C010-25DC AT27C010-25JC AT27C010-25KC AT27C010-25LC AT27C010-25PC	32DW6 32J 32KW 32LW 32P6	Commercial (0°C to 70°C)
250	50	0.1	AT27C010-25DI AT27C010-25JI AT27C010-25KI AT27C010-25LI AT27C010-25PI	32DW6 32J 32KW 32LW 32P6	Industrial (-40°C to 85°C)
			AT27C010-25DM AT27C010-25KM AT27C010-25LM	32DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C010-25DM/883 AT27C010-25KM/883 AT27C010-25LM/883	32DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	50	0.1	5962-89614 06 M XX 5962-89614 06 M YX	32DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	50	0.1	5962-89614 05 M XX 5962-89614 05 M YX	32DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
170	50	0.1	5962-89614 04 M XX 5962-89614 04 M YX	32DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	50	0.1	5962-89614 03 M XX 5962-89614 03 M YX	32DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	50	0.1	5962-89614 02 M XX 5962-89614 02 M YX	32DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
300	50	0.1	5962-89614 01 M XX 5962-89614 01 M YX	32DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

tACC (ns)	Icc (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	40	0.1	AT27C010-12TC	32T	Commercial (0° to 70°C)
150	40	0.1	AT27C010-15TC	32T	Commercial (0° to 70°C)

Package Type	
32DW6	32 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32KW	32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
32R	32 Lead, 0.450" Wide, Plastic Gull Wing Small Outline OTP (SOIC)
32T	32 Lead, Plastic Thin Small Outline Package OTP (TSOP)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
100	40	0.1	AT27C010L-10DC AT27C010L-10KC AT27C010L-10LC	32DW6 32KW 32LW	Commercial (0°C to 70°C)
120	25	0.1	AT27C010L-12DC AT27C010L-12JC AT27C010L-12KC AT27C010L-12LC AT27C010L-12PC AT27C010L-12RC	32DW6 32J 32KW 32LW 32P6 32R	Commercial (0°C to 70°C)
120	30	0.1	AT27C010L-12DI AT27C010L-12JI AT27C010L-12KI AT27C010L-12LI AT27C010L-12PI AT27C010L-12RI	32DW6 32J 32KW 32LW 32P6 32R	Industrial (-40°C to 85°C)
			AT27C010L-12DM AT27C010L-12KM AT27C010L-12LM	32DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C010L-12DM/883 AT27C010L-12KM/883 AT27C010L-12LM/883	32DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	25	0.1	AT27C010L-15DC AT27C010L-15JC AT27C010L-15LC AT27C010L-15KC AT27C010L-15PC AT27C010L-15RC	32DW6 32J 32LW 32KW 32P6 32R	Commercial (0°C to 70°C)
150	30	0.1	AT27C010L-15DI AT27C010L-15JI AT27C010L-15KI AT27C010L-15LI AT27C010L-15PI AT27C010L-15RI	32DW6 32J 32KW 32LW 32P6 32R	Industrial (-40°C to 85°C)
			AT27C010L-15DM AT27C010L-15KM AT27C010L-15LM	32DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C010L-15DM/883 AT27C010L-15KM/883 AT27C010L-15LM/883 AT27C010L-17LI AT27C010L-17PI AT27C010L-17SI	32DW6 32KW 32LW 32LW 32P6 32S	Military/883C Class B, Fully Compliant (-55°C to 125)
200	25	0.1	AT27C010L-20DC AT27C010L-20JC AT27C010L-20KC AT27C010L-20LC AT27C010L-20PC AT27C010L-20RC	32DW6 32J 32KW 32LW 32P6 32R	Commercial (0°C to 70°C)

4

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
200	30	0.1	AT27C010L-20DI AT27C010L-20JI AT27C010L-20KI	32DW6 32J 32KW	Industrial (-40°C to 85°C)
			AT27C010L-20LI AT27C010L-20PI AT27C010L-20RI	32LW 32P6 32R	
			AT27C010L-20DM AT27C010L-20KM AT27C010L-20LM	32DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C010L-20DM/883 AT27C010L-20KM/883 AT27C010L-20LM/883	32DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	25	0.1	AT27C010L-25DC AT27C010L-25JC AT27C010L-25KC AT27C010L-25LC AT27C010L-25PC	32DW6 32J 32KW 32LW 32P6	Commercial (0°C to 70°C)
250	30	0.1	AT27C010L-25DI AT27C010L-25JI AT27C010L-25KI AT27C010L-25LI AT27C010L-25PI	32DW6 32J 32KW 32LW 32P6	Industrial (-40°C to 85°C)
			AT27C010L-25DM AT27C010L-25KM AT27C010L-25LM	32DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C010L-25DM/883 AT27C010L-25KM/883 AT27C010L-25LM/883	32DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	25	0.1	AT27C010L-12TC	32T	Commercial (0° to 70°C)
150	25	0.1	AT27C010L-15TC	32T	Commercial (0° to 70°C)

Package Type	
32DW6	32 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32KW	32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
32R	32 Lead, 0.450" Wide, Plastic Gull Wing Small Outline OTP (SOIC)
32T	32 Lead, Plastic Thin Small Outline Package OTP (TSOP)

32DW6	32 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32KW	32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
32R	32 Lead, 0.450" Wide, Plastic Gull Wing Small Outline OTP (SOIC)
32T	32 Lead, Plastic Thin Small Outline Package OTP (TSOP)

1 Megabit (128K x 8) Low Voltage UV Erasable CMOS EPROM

Features

- **Wide Power Supply Range, 3.0 VDC to 5.5 VDC**
- **Compatible with JEDEC Standard AT27C010**
- **Low Power 3-Volt CMOS Operation**
  - **100 µA max. Standby**
  - **26 mW max. Active at 1 MHz for V_{CC} = 3.3 VDC**
  - **138 mW max. Active at 5 MHz for V_{CC} = 5.5 VDC**
- **Read Access Time - 250 ns**
- **Wide Selection of JEDEC Standard Packages Including OTP**
  - **32-Lead 600-mil Cerdip and OTP Plastic DIP and SOIC**
  - **32-Pad LCC, 32-Lead JLCC, OTP PLCC and TSOP**
- **High Reliability CMOS Technology**
  - **2000 V ESD Protection**
  - **200 mA Latchup Immunity**
- **Rapid Programming - 100 µs/byte (typical)**
- **Two-line Control**
- **CMOS and TTL Compatible Inputs and Outputs**
- **Integrated Product Identification Code**
- **Commercial and Industrial Temperature Ranges**

Description

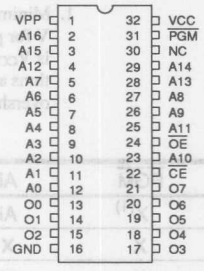
The AT27LV010 chip is a low power, low voltage 1,048,576 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized as 128K x 8 bits. It requires only one supply in the range of 3.0 to 5.5 VDC in normal read mode operation, making it ideal for battery powered systems.

With a typical power draw of only 18mW at 1 MHz and V_{CC} at 3.3 VDC, the AT27LV010 will draw less than one-fifth the power of a standard 5-volt EPROM. Standby mode supply current is typically less than 10 µA.

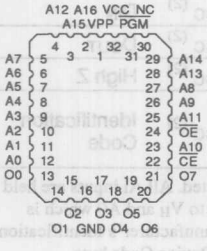
Pin Configurations

Pin Name	Function
A0-A16	Addresses
O0-O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Strobe
NC	No Connect

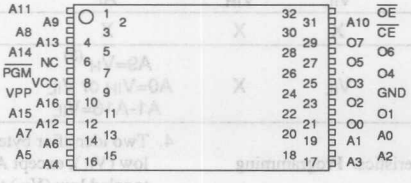
CDIP, PDIP, SOIC Top View



LCC, JLCC, PLCC Top View



TSOP Top View
Type 1



Description (Continued)

The AT27LV010 comes in a choice of industry standard JEDEC-approved through hole and surface mount packages including windowed and one time programmable (OTP) packages, such as the OTP thin small outline package (TSOP). All devices feature two line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

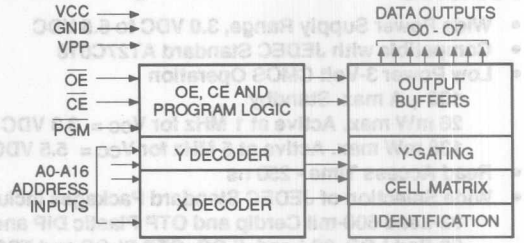
The AT27LV010 operating with V_{CC} at 3.0 VDC produces TTL level outputs that are compatible with standard TTL logic devices operating at V_{CC} = 5.0 VDC.

Atmel's 27LV010 has additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages. The AT27LV010 programs identically as an AT27C010.

Erasure Characteristics

The entire memory array of the AT27LV010 is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 µW/cm^2 intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 W·sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +125°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Voltage on A9 with Respect to Ground	-2.0 V to +14.0 V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0 V to +14.0 V(1)
Integrated UV Erase Dose	7258 W•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75 V dc which may be exceeded if certain precautions are observed (consult application notes) and which may overshoot to +7.0 V for pulses of less than 20 ns.

Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	Ai	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X(1)	Ai	X	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	X	X	X	V_{CC}	High Z
Standby	V_{IH}	X	X	X	X	V_{CC}	High Z
Fast Program(2)	V_{IL}	V_{IH}	V_{IL}	Ai	V_{PP}	V_{CC} (2)	D_{IN}
PGM Verify(2)	V_{IL}	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC} (2)	D_{OUT}
PGM Inhibit(2)	V_{IH}	X	X	X	V_{PP}	V_{CC} (2)	High Z
Product Identification(2),(4)	V_{IL}	V_{IL}	X	A9=V_H (3) A0=V_{IH} or V_{IL} A1-A16=V_{IL}	X	V_{CC} (2)	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics. Programming modes require V_{CC} > 4.5 V.
3. V_H = 12.0 ± 0.5 V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

D.C. and A.C. Operating Conditions for Read Operation

		AT27LV010	
		-25	-30
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		3.0 V to 5.5 V	3.0 V to 5.5 V

D.C. and Operating Characteristics for Read Operation

(V_{CC} = 3.0 V to 5.5 V unless otherwise specified)

Symbol	Parameter	Condition			Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1 V to V_{CC}+1 V				5	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1 V to V_{CC}+0.1 V				10	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}-0.7 V to V_{CC}+0.3 V				10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC}-0.3 to V_{CC}+1.0 V				100	µA
		I_{SB2} (TTL), $\overline{CE}$=2.0 to V_{CC}+1.0 V				1	mA
I_{CC}	V_{CC} Active Current	I_{CC1}	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}, V_{CC} = 5.5 V	Com.		25	mA
				Ind.		30	mA
		I_{CC2}	f = 1 MHz, I_{OUT} = 0 mA $\overline{CE}$ = V_{IL}, V_{CC} = 3.3 V	Com.		8	mA
				Ind.		10	mA
V_{IL}	Input Low Voltage				-0.6	0.8	V
V_{IH}	Input High Voltage				2.0	V_{CC}+0.75	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA				.45	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA			V_{CC}-0.3		V
		I_{OH} = -400 µA			2.4		V

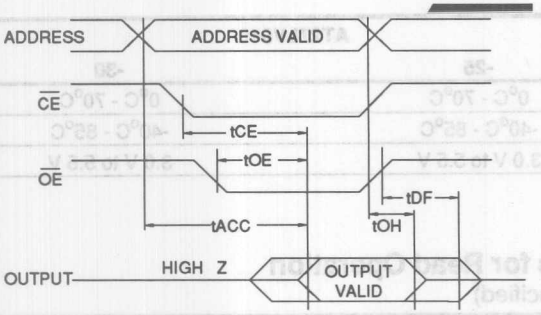
Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

A.C. Characteristics for Read Operation (V_{CC} = 3.0V to 5.5V)

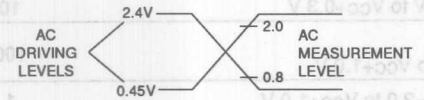
				AT27LV010				
				-25		-30		
Symbol	Parameter	Condition		Min	Max	Min	Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Com.		250		270	ns
			Ind.		250		270	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}			250		300	ns
t_{OE} (2,3)	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}			100		150	ns
t_{DF} (4,5)	$\overline{OE}$ High to Output Float	$\overline{CE}$ = V_{IL}			50		50	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		0		0		ns

Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.



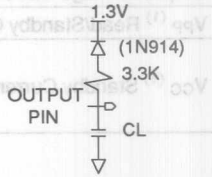
Notes:
1. Timing measurement references are 0.8 V and 2.0 V. Input AC driving levels are 0.45 V and 2.4 V. See Input Test Waveforms and Measurement Levels.
2. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

Input Test Waveform and Measurement Level



t_R, t_F < 20 ns (10% to 90%)

Output Test Load



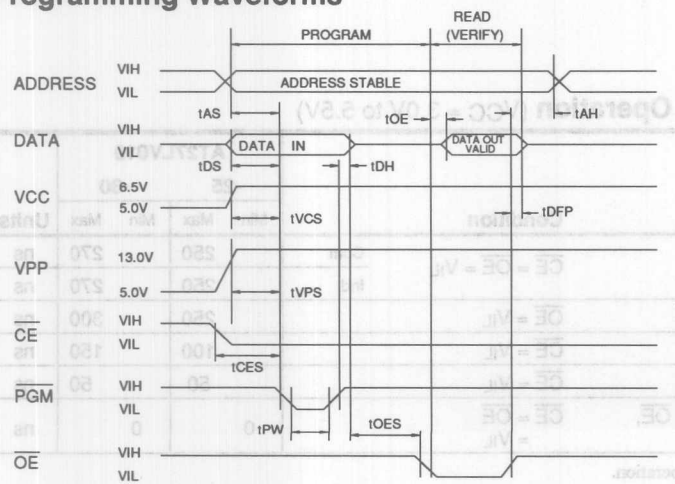
Note: C_L = 100 pF including jig capacitance.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	8	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Notes: 1. Typical values for 5-V supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes:
1. The Input Timing Reference is 0.8 V for V_{IL} and 2.0 V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27LV010 a 0.1-µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

D.C. Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25$ V, $V_{PP} = 13.0 \pm 0.25$ V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	$V_{CC}+1$	V
V_{OL}	Output Low Volt.	$I_{OL}=2.1$ mA		.45	V
V_{OH}	Output High Volt.	$I_{OH}=-400$ µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			40	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE}=\overline{PGM}=V_{IL}$		20	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25$ V, $V_{PP} = 13.0 \pm 0.25$ V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Limits Max	Units
t_{AS}	Address Setup Time		2		µs
t_{CES}	$\overline{CE}$ Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{PGM}$ Program Pulse Width	(Note 3)	95	105	µs
t_{OE}	Data Valid from $\overline{OE}$			150	ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) ..... 20 ns
Input Pulse Levels ..... 0.45 V to 2.4 V
Input Timing Reference Level ..... 0.8 V to 2.0 V
Output Timing Reference Level ..... 0.8 V to 2.0 V

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100 µsec ± 5%.

Atmel's 27LV010 Integrated Product Identification Code[1]

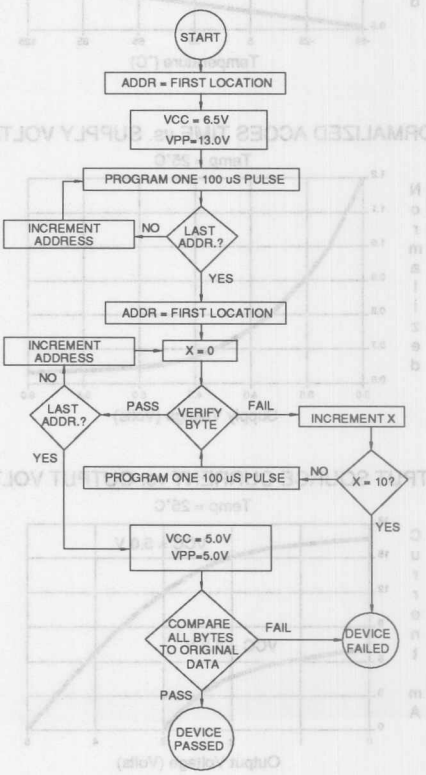
Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	0	0	0	0	0	1	0	1	O5

Note: 1. The AT27LV010 has the same Product Identification Code as the AT27C010/L. Both are programming compatible.

4

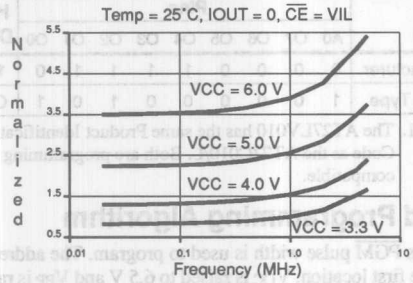
Rapid Programming Algorithm

A 100 µs $\overline{PGM}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5 V and V_{PP} is raised to 13.0 V. Each address is first programmed with one 100 µs $\overline{PGM}$ pulse without verification. Then a verification/ reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0 V and V_{CC} to 5.0 V. All bytes are read again and compared with the original data to determine if the device passes or fails.

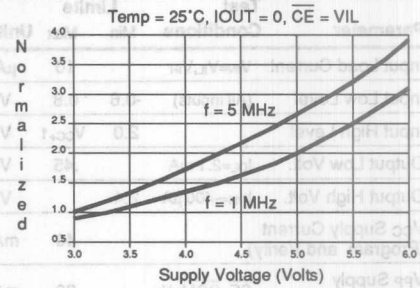


LV EPROM Product Characteristics

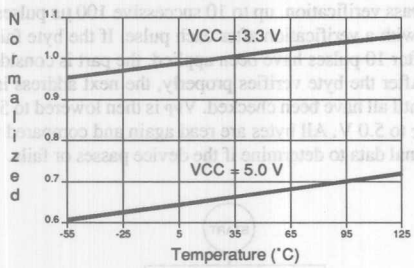
NORMALIZED SUPPLY CURRENT vs. FREQUENCY



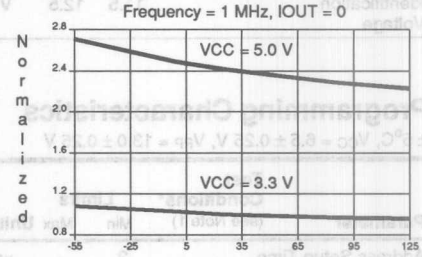
NORMALIZED SUPPLY CURRENT vs. VOLTAGE



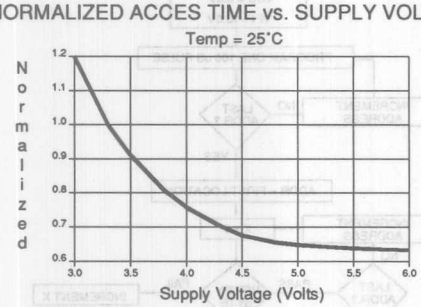
NORMALIZED ACCESS TIME vs. TEMPERATURE



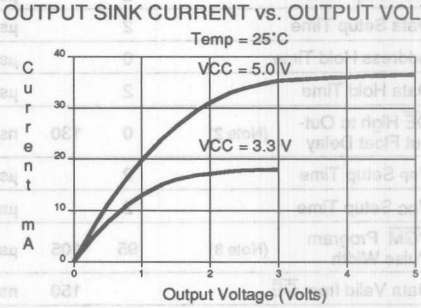
NORMALIZED SUPPLY CURRENT vs. TEMP.



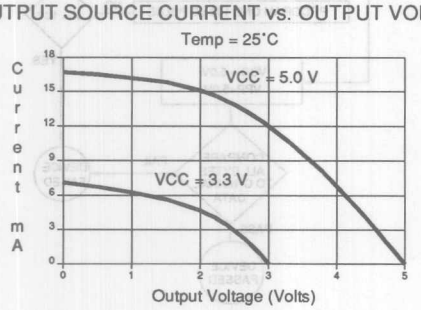
NORMALIZED ACCES TIME vs. SUPPLY VOLTAGE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



Ordering Information

t_{ACC} (ns)	I_{CC} (mA) V_{CC} = 3.3 V Active	I_{CC} (mA) V_{CC} = 3.3 V Standby	Ordering Code	Package	Operation Range
250	8	0.1	AT27LV010-25DC AT27LV010-25KC AT27LV010-25LC	32DW6 32KW 32LW	Commercial (0°C to 70°C)
250	10	0.1	AT27LV010-25DI AT27LV010-25LI	32DW6 32LW	Industrial (-40°C to 85°C)
300	8	0.1	AT27LV010-30DC AT27LV010-30JC AT27LV010-30KC AT27LV010-30LC AT27LV010-30PC AT27LV010-30RC	32DW6 32J 32KW 32LW 32P6 32R	Commercial (0°C to 70°C)
300	10	0.1	AT27LV010-30DI AT27LV010-30LI	32DW6 32LW	Industrial (-40°C to 85°C)

t_{ACC} (ns)	I_{CC} (mA) V_{CC} = 3.3 V Active	I_{CC} (mA) V_{CC} = 3.3 V Standby	Ordering Code	Package	Operation Range
250	8	0.1	AT27LV010-25TC	32T	Commercial (0°C to 70°C)
300	8	0.1	AT27LV010-30TC	32T	Commercial (0°C to 70°C)

Package Type	
32DW6	32 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32KW	32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
32R	32 Lead, 0.450" Wide, Plastic Gull Wing Small Outline OTP (SOIC)
32T	32 Lead, Plastic Thin Small Outline Package OTP (TSOP)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA) V_{CC} = 3.3 V Active	Standby	Ordering Code	Package	Operation Range
250	8	0.1	AT27LV010-25DC AT27LV010-25KC AT27LV010-25JC	32DW6 32KW 32JW	Commercial (0°C to 70°C)
250	10	0.1	AT27LV010-25DI AT27LV010-25JI	32DW6 32JW	Industrial (-40°C to 85°C)
300	8	0.1	AT27LV010-30DC AT27LV010-30JC AT27LV010-30KC AT27LV010-30JC AT27LV010-30PC AT27LV010-30RC	32DW6 32J 32KW 32JW 32P6 32R	Commercial (0°C to 70°C)
300	10	0.1	AT27LV010-30DI AT27LV010-30JI	32DW6 32JW	Industrial (-40°C to 85°C)

t_{ACC} (ns)	I_{CC} (mA) V_{CC} = 3.3 V Active	Standby	Ordering Code	Package	Operation Range
250	8	0.1	AT27LV010-25TC	32T	Commercial (0°C to 70°C)
300	8	0.1	AT27LV010-30TC	32T	Commercial (0°C to 70°C)

Package Type	
32DW6	32 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32KW	32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
32R	32 Lead, 0.450" Wide, Plastic Gull Wing Small Outline OTP (SOIC)
32T	32 Lead, Plastic Thin Small Outline Package OTP (TSOP)

1 Megabit (64K x 16) UV Erasable CMOS EPROM

Features

- Low Power CMOS Operation
  - 100 µA max. Standby
  - 30 mA max. Active at 5 MHz
- Fast Read Access Time - 100 ns
- Wide Selection of JEDEC Standard Packages Including OTP
  - 40-Lead 600-mil Cerdip and OTP Plastic DIP
  - 44-Pad LCC and OTP PLCC
- 5 V ± 10% Power Supply
- High Reliability CMOS Technology
  - 2000 V ESD Protection
  - 200 mA Latchup Immunity
- Rapid Programming - 100 µs/word (typical)
- Two-line Control
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Full Military, Commercial and Industrial Temperature Ranges

Description

The AT27C1024 is a low-power, high performance 1,048,576 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized 64K x 16. It requires only one 5-V power supply in normal read mode operation. Any word can be accessed in less than 100 ns, eliminating the need for speed reducing WAIT states. The by-16 organization make this part ideal for high-performance 16 and 32 bit microprocessor systems.

In read mode, the AT27C1024 typically consumes 15 mA. Standby mode supply current is typically less than 10 µA.

The AT27C1024 come in a choice of industry standard JEDEC-approved packages including; 40-pin DIP in ceramic or one time programmable (OTP) plastic, and 44-pad ceramic leadless chip carrier (LCC), or OTP plastic J-leaded chip carrier (PLCC). All devices feature two line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

With high density 64K word storage capability, the AT27C1024 allow firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

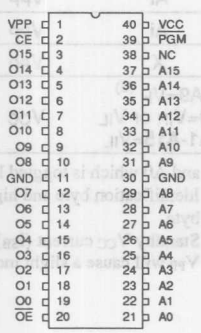
Atmel's 27C1024 have additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/word. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Pin Configurations

Pin Name	Function
A0-A15	Addresses
O0-O15	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Strobe
NC	No Connect

Note: Both GND pins must be connected.

CDIP, PDIP Top View



LCC, JLCC, PLCC Top View

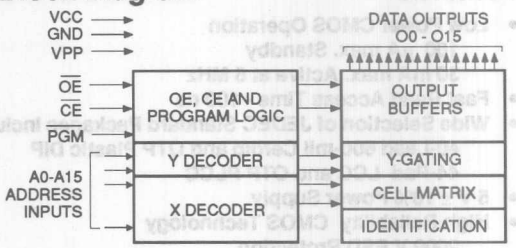


Note: PLCC Package Pins 1 and 23 are DON'T CONNECT.

Erasure Characteristics

The entire memory array of the AT27C1024 is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 W·sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Voltage on A9 with Respect to Ground	-2.0 V to +14.0 V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0 V to +14.0 V(1)
Integrated UV Erase Dose	7258 W•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC}+0.75 V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	Ai	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X(1)	Ai	X	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	X	X	X	V_{CC}	High Z
Standby	V_{IH}	X	X	X	X(5)	V_{CC}	High Z
Rapid Program(2)	V_{IL}	V_{IH}	V_{IL}	Ai	V_{PP}	V_{CC}	D_{IN}
PGM Verify	V_{IL}	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC}	D_{OUT}
PGM Inhibit	V_{IH}	X	X	X	V_{PP}	V_{CC}	High Z
Product Identification(4)	V_{IL}	V_{IL}	X	A9=V_H (3) A0=V_{IH} or V_{IL} A1-A15=V_{IL}	V_{CC}	V_{CC}	Identification Code

Notes:
1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. $V_H = 12.0 \pm 0.5$ V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.
5. Standby V_{CC} current (I_{SB}) is specified with V_{PP}=V_{CC}. V_{CC} > V_{PP} will cause a slight increase in I_{SB}.

D.C. and A.C. Operating Conditions for Read Operation

		AT27C1024			
		-10	-12	-15	-20
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.		-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 5%	5 V ± 10%	5 V ± 10%	5 V ± 10%

4

D.C. and Operating Characteristics for Read Operation

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1 V to V_{CC}+1 V			5	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1 V to V_{CC}+0.1 V			10	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = 3.8 to V_{CC}+0.3 V			10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS) $\overline{CE}$ = V_{CC}-0.3 to V_{CC}+1.0 V			100	µA
		I_{SB2} (TTL) $\overline{CE}$ = 2.0 to V_{CC}+1.0 V			1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}	Com.		30	mA
			Ind.,Mil.		40	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC}+ 0.75	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			.45	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA		V_{CC}-0.3		V
		I_{OH} = -2.5 mA		3.5		V
		I_{OH} = -400 µA		2.4		V

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

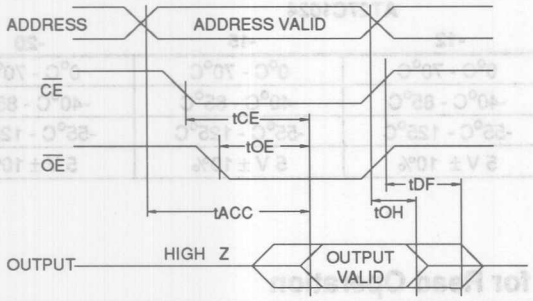
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

A.C. Characteristics for Read Operation

				AT27C1024								
				-10		-12		-15		-20		
Symbol	Parameter	Condition		Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Com.		100		120		150		200	ns
			Ind.,Mil.				120		150		200	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}			100		120		150		200	ns
t_{OE} (2,3)	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}			30		35		65		75	ns
t_{DF} (4,5)	$\overline{OE}$ High to Output Float	$\overline{CE}$ = V_{IL}			30		30		40		55	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		0		0		0		0		ns

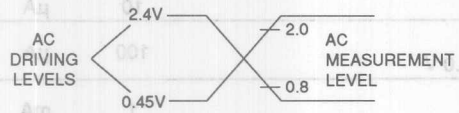
Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

A.C. Waveforms for Read Operation [1]



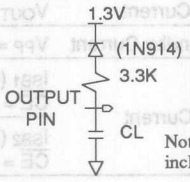
Notes:
1. Timing measurement references are 0.8 V and 2.0 V. Input AC driving levels are 0.45 V and 2.4 V, unless otherwise specified.
2. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

Input Test Waveforms and Measurement Levels



t_R, t_F < 20 ns (10% to 90%)

Output Test Load



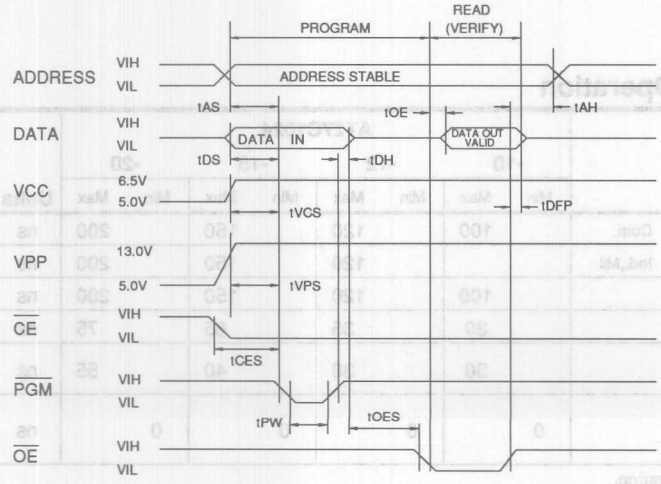
Note: C_L = 100 pF including jig capacitance.

Pin Capacitance (f = 1 MHz T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	8	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes:
1. The Input Timing Reference is 0.8 V for V_{IL} and 2.0 V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27C1024 a 0.1-µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

D.C. Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25$ V, $V_{PP} = 13.0 \pm 0.25$ V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	$V_{CC}+0.3$	V
V_{OL}	Output Low Volt.	I_{OL}=2.1 mA		.45	V
V_{OH}	Output High Volt.	I_{OH}=-400 µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			50	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE}=\overline{PGM}=V_{IL}$		30	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25$ V, $V_{PP} = 13.0 \pm 0.25$ V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Limits Max	Units
t_{AS}	Address Setup Time		2		µs
t_{CES}	$\overline{CE}$ Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{PGM}$ Program Pulse Width	(Note 3)	95	105	µs
t_{OE}	Data Valid from $\overline{OE}$			150	ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) ..... 20 ns
Input Pulse Levels ..... 0.45 V to 2.4 V
Input Timing Reference Level ..... 0.8 V to 2.0 V
Output Timing Reference Level ..... 0.8 V to 2.0 V

Notes:

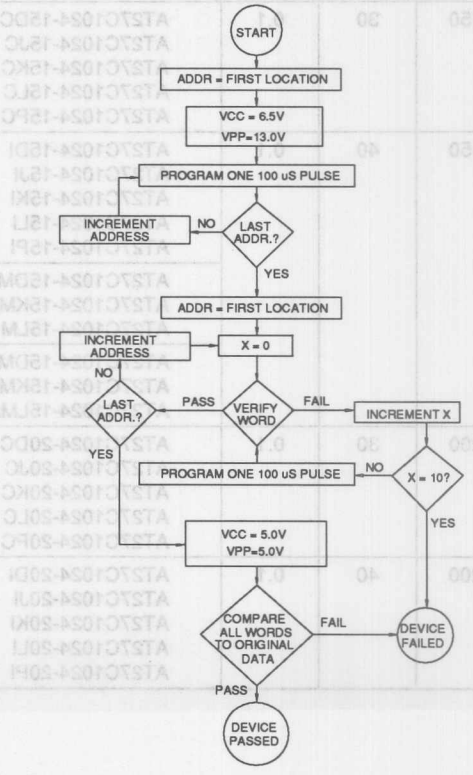
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100 µsec ± 5%.

Atmel's 27C1024 Integrated Product Identification Code

Codes	Pins A0	015-08	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	0	1	1	1	1	0	001E
Device Type	1	0	1	1	1	1	0	0	0	1	00F1

Rapid Programming Algorithm

A 100 µs $\overline{PGM}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5 V and V_{PP} is raised to 13.0 V. Each address is first programmed with one 100 µs $\overline{PGM}$ pulse without verification. Then a verification / reprogramming loop is executed for each address. In the event a word fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the word fails to verify after 10 pulses have been applied, the part is considered failed. After the word verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0 V and V_{CC} to 5.0 V. All words are read again and compared with the original data to determine if the device passes or fails.



t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
100	30	0.1	AT27C1024-10DC AT27C1024-10KC AT27C1024-10LC	40DW6 44KW 44LW	Commercial (0°C to 70°C)
120	30	0.1	AT27C1024-12DC AT27C1024-12JC AT27C1024-12KC AT27C1024-12LC AT27C1024-12PC	40DW6 44J 44KW 44LW 44P6	Commercial (0°C to 70°C)
120	40	0.1	AT27C1024-12DI AT27C1024-12JI AT27C1024-12KI AT27C1024-12LI AT27C1024-12PI	40DW6 44J 44KW 44LW 44P6	Industrial (-40°C to 85°C)
			AT27C1024-12DM AT27C1024-12KM AT27C1024-12LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			AT27C1024-12DM/883 AT27C1024-12KM/883 AT27C1024-12LM/883	40DW6 44KW 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	30	0.1	AT27C1024-15DC AT27C1024-15JC AT27C1024-15KC AT27C1024-15LC AT27C1024-15PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
150	40	0.1	AT27C1024-15DI AT27C1024-15JI AT27C1024-15KI AT27C1024-15LI AT27C1024-15PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
			AT27C1024-15DM AT27C1024-15KM AT27C1024-15LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			AT27C1024-15DM/883 AT27C1024-15KM/883 AT27C1024-15LM/883	40DW6 44KW 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	30	0.1	AT27C1024-20DC AT27C1024-20JC AT27C1024-20KC AT27C1024-20LC AT27C1024-20PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
200	40	0.1	AT27C1024-20DI AT27C1024-20JI AT27C1024-20KI AT27C1024-20LI AT27C1024-20PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
200	40	0.1	AT27C1024-20DM AT27C1024-20KM AT27C1024-20LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			AT27C1024-20DM/883 AT27C1024-20KM/883 AT27C1024-20LM/883	40DW6 44KW 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	60	0.1	5962-86805 06 QX 5962-86805 06 XX	40DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	60	0.1	5962-86805 05 QX 5962-86805 05 XX	40DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
170	60	0.1	5962-86805 04 QX 5962-86805 04 XX	40DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	60	0.1	5962-86805 03 QX 5962-86805 03 XX	40DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	60	0.1	5962-86805 02 QX 5962-86805 02 XX	40DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
300	60	0.1	5962-86805 01 QX 5962-86805 01 XX	40DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

4

Package Type	
40DW6	40 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
44J	44 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
44KW	44 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
44LW	44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
40P6	40 Lead, 0.600" Wide, Plastic Dual Inline package OTP (PDIP)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
200	40	0.1	AT27C1024-20DM AT27C1024-20KM AT27C1024-20LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			AT27C1024-20DM/883 AT27C1024-20KM/883 AT27C1024-20LM/883	40DW6 44KW 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	60	0.1	5962-88805 08 CX 5962-88805 08 XX	40DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	60	0.1	5962-88805 05 CX 5962-88805 05 XX	40DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
170	60	0.1	5962-88805 04 CX 5962-88805 04 XX	40DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	60	0.1	5962-88805 03 CX 5962-88805 03 XX	40DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	60	0.1	5962-88805 02 CX 5962-88805 02 XX	40DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
300	60	0.1	5962-88805 01 CX 5962-88805 01 XX	40DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
40DW6	40 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
44J	44 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
44KW	44 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
44LW	44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
40P6	40 Lead, 0.600" Wide, Plastic Dual Inline package OTP (PDIP)

Features

- Very Fast Read Access Time - 55ns
- Low Power CMOS Operation
  - 8 mA max. Standby
  - 80 mA max. Active at 10 MHz
- Wide Selection of JEDEC Standard Packages Including OTP
  - 40-Lead 600-mil Cerdip and OTP Plastic
  - 44-Pad LCC and OTP PLCC
- High Output Drive Capability
- High Reliability CMOS Technology
  - 2000 V ESD Protection
  - 200 mA Latchup Immunity
- Rapid Programming - 100 µs/word (typical)
- Two-line Control
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Full Military, Industrial and Commercial Temperature Ranges

Description

The AT27HC1024 chip is a high-speed, low-power 1,048,576 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized as 64K x 16 bits. It requires only one 5-V power supply in normal read mode operation. Any word can be accessed in less than 55 ns, eliminating the need for speed reducing WAIT states. The by-16 organization makes these parts ideal for high-performance 16 and 32 bit microprocessor and digital signal processor systems.

In read mode, the AT27HC1024 typically consumes 50 mA, while in standby mode supply current is typically less than 1 mA.

The AT27HC1024 come in a choice of industry standard JEDEC-approved packages including; 40-pin DIP in ceramic or one time programmable (OTP) plastic, and 44-pad ceramic leadless chip carrier (LCC), or OTP plastic J-leaded chip carrier (PLCC). All devices feature two line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

With high density 64K word storage capability, the AT27HC1024 allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media. The AT27HC1024 has exceptional CMOS output device capability— source 4 mA and sink 16mA per output.

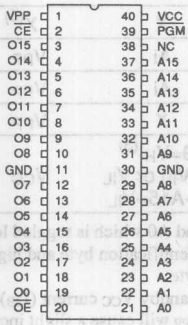
continued on next page

Pin Configurations

Pin Name	Function
A0-A15	Addresses
O0-O15	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Strobe
NC	No Connect

Note: Both GND pins must be connected.

CDIP, PDIP Top View



LCC, JLCC, PLCC Top View



Note: PLCC Package Pins 1 and 23 are DON'T CONNECT.

1 Megabit (64K x 16) High Speed UV Erasable CMOS EPROM

4

Preliminary

PRELIMINARY

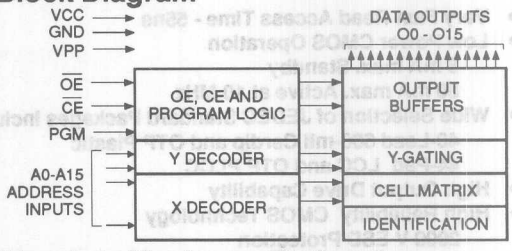
Description (Continued)

Atmel's 27HC1024 has additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/word. Atmel's high speed single transistor floating poly EPROM cell technology also speeds up programming by eliminating the second program "Os" operation required for two transistor per cell designs. The AT27HC1024 uses the same widely accepted programming algorithm as the AT27C1024. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Erasure Characteristics

The entire memory array of the AT27HC1024 is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 µW/cm^2 intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 W·sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Voltage on A9 with Respect to Ground	-2.0 V to +14.0 V(1)
VPP Supply Voltage with Respect to Ground	-2.0 V to +14.0 V(1)
Integrated UV Erase Dose	7258 W•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC}+0.75 V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	Ai	VPP	VCC	Outputs
Read	V_{IL}	V_{IL}	X(1)	Ai	X	VCC	DOUT
Output Disable	X	V_{IH}	X	X	X	VCC	High Z
Standby	V_{IH}	X	X	X	X(5)	VCC	High Z
Rapid Program(2)	V_{IL}	V_{IH}	V_{IL}	Ai	VPP	VCC	DIN
PGM Verify	V_{IL}	V_{IL}	V_{IH}	Ai	VPP	VCC	DOUT
PGM Inhibit	V_{IH}	X	X	X	VPP	VCC	High Z
Product Identification(4)	V_{IL}	V_{IL}	X	A9=V_H (3) A0=V_{IH} or V_{IL} A1-A15=V_{IL}	VCC	VCC	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. V_H = 12.0 ± 0.5 V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.
5. Standby V_{CC} current (I_{SB}) is specified with V_{PP}=V_{CC}. V_{CC} > V_{PP} will cause a slight increase in I_{SB}.

D.C. and A.C. Operating Conditions for Read Operation

		AT27HC1024		
		-55	-70	-90
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.		-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 5%	5 V ± 10%	5 V ± 10%

D.C. and Operating Characteristics for Read Operation

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1 V to V_{CC}+1 V			5	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1 V to V_{CC}+0.1 V			10	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = 3.8 to V_{CC}+0.3 V			10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS) $\overline{CE}$ = V_{CC}-0.3 to V_{CC}+1.0 V	Com.		8	mA
			Ind., Mil.		10	mA
		I_{SB2} (TTL) $\overline{CE}$ = 2.0 to V_{CC}+1.0 V	Com.		17	mA
			Ind., Mil.		20	mA
I_{CC}	V_{CC} Active Current	f = 10 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}	Com.		80	mA
			Ind.,Mil.		90	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			.45	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA		V_{CC}-0.3		V
		I_{OH} = -4.0 mA		2.4		V

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

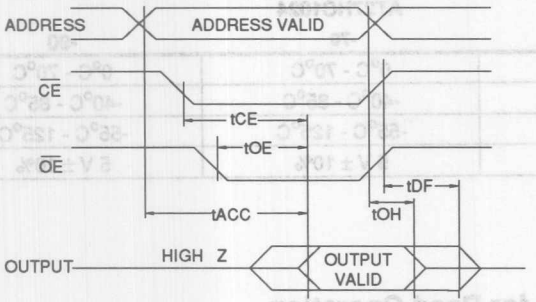
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

A.C. Characteristics for Read Operation

				AT27HC1024						
				-55		-70		-90		
Symbol	Parameter	Condition		Min	Max	Min	Max	Min	Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Com.		55		70		90	ns
			Ind.,Mil.				70		90	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}			55		70		90	ns
t_{OE} (2,3)	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}			30		30		30	ns
t_{DF} (4,5)	$\overline{OE}$ High to Output Float	$\overline{CE}$ = V_{IL}			10		15		20	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		0		0		0		ns

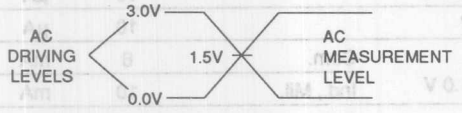
Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

A.C. Waveforms for Read Operation [1]



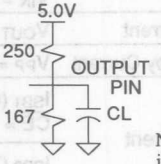
Notes:
1. Timing measurement references is 1.5 V. Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified. C_L = 30 pF, add 6 ns for C_L = 100 pF.
2. t_{DF} is specified from $\overline{OE}$. t_{DF} is measured at V_{OH}-0.5 V or V_{OL}+0.5 V with C_L = 5 pF.
3. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
5. This parameter is only sampled and is not 100% tested.

Input Test Waveforms and Measurement Levels



t_R, t_F < 5 ns (10% to 90%)

Output Test Load



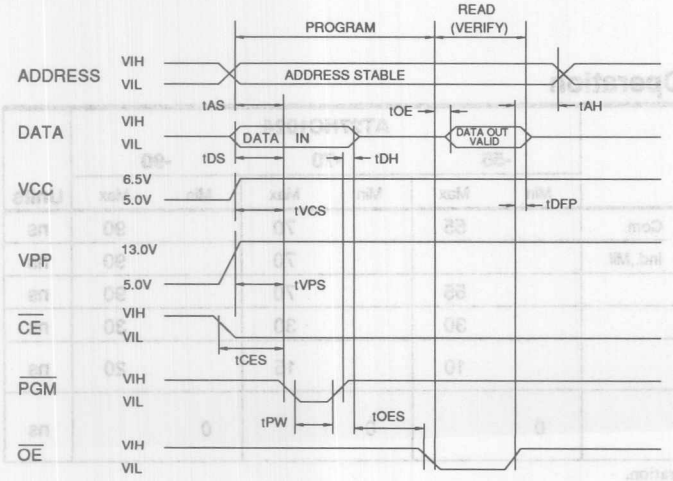
Note: C_L = 30 pF including jig capacitance.

Pin Capacitance (f = 1 MHz T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	10	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes:
1. The Input Timing Reference is 0.0 V for V_{IL} and 3.0 V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27HC1024 a 0.1-µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

D.C. Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25$ V, $V_{PP} = 13.0 \pm 0.25$ V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	$V_{CC}+1$	V
V_{OL}	Output Low Volt.	I_{OL}=16mA		.45	V
V_{OH}	Output High Volt.	I_{OH}=-4mA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			60	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE}=\overline{PGM}=V_{IL}$		40	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25$ V, $V_{PP} = 13.0 \pm 0.25$ V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Limits Max	Units
t_{AS}	Address Setup Time		2		µs
t_{CES}	$\overline{CE}$ Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{PGM}$ Program Pulse Width	(Note 3)	95	105	µs
t_{OE}	Data Valid from $\overline{OE}$			150	ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) ..... 5 ns
Input Pulse Levels ..... 0.0 V to 3.0 V
Input Timing Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V

Notes:

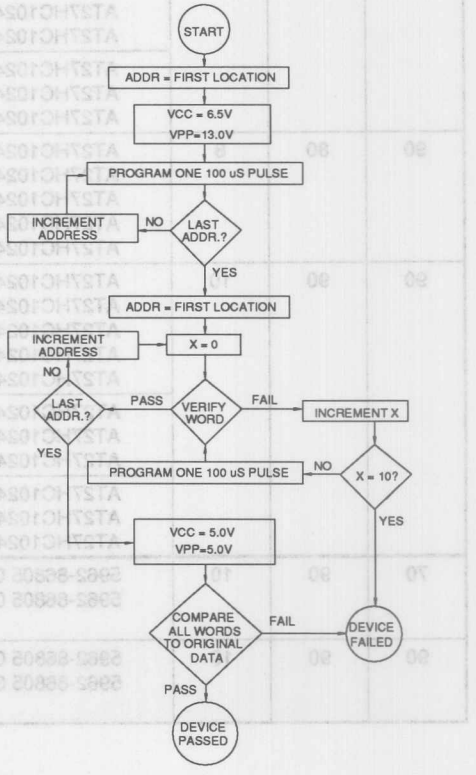
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100 µsec ± 5%.

Atmel's 27HC1024 Integrated Product Identification Code

Codes	Pins A0	015-08	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	0	1	1	1	1	0	001E
Device Type	1	0	0	1	1	0	0	0	0	1	0061

Rapid Programming Algorithm

A 100 µs $\overline{PGM}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5 V and V_{PP} is raised to 13.0 V. Each address is first programmed with one 100 µs $\overline{PGM}$ pulse without verification. Then a verification / reprogramming loop is executed for each address. In the event a word fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the word fails to verify after 10 pulses have been applied, the part is considered failed. After the word verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0 V and V_{CC} to 5.0 V. All words are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
55	80	8	AT27HC1024-55DC AT27HC1024-55JC AT27HC1024-55KC AT27HC1024-55LC AT27HC1024-55PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
55	90	8	AT27HC1024-55DI AT27HC1024-55JI AT27HC1024-55LI	40DW6 44J 44LW	Industrial (-40°C to 85°C)
70	80	8	AT27HC1024-70DC AT27HC1024-70JC AT27HC1024-70KC AT27HC1024-70LC AT27HC1024-70PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
70	90	10	AT27HC1024-70DI AT27HC1024-70JI AT27HC1024-70KI AT27HC1024-70LI AT27HC1024-70PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
			AT27HC1024-70DM AT27HC1024-70KM AT27HC1024-70LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			AT27HC1024-70DM/883 AT27HC1024-70KM/883 AT27HC1024-70LM/883	40DW6 44KW 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	80	8	AT27HC1024-90DC AT27HC1024-90JC AT27HC1024-90KC AT27HC1024-90LC AT27HC1024-90PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
90	90	10	AT27HC1024-90DI AT27HC1024-90JI AT27HC1024-90KI AT27HC1024-90LI AT27HC1024-90PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
			AT27HC1024-90DM AT27HC1024-90KM AT27HC1024-90LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			AT27HC1024-90DM/883 AT27HC1024-90KM/883 AT27HC1024-90LM/883	40DW6 44KW 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
70	90	10	5962-86805 08 QX 5962-86805 08 XX	40DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	90	10	5962-86805 07 QX 5962-86805 07 XX	40DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

Package Type	
40DW6	40 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
44J	44 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
44KW	44 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
44LW	44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
40P6	40 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)

	Package Type
40DWE	40 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
44J	44 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
44KW	44 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
44LW	44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
40P6	40 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)

1 Megabit (64K x 16) Low Voltage UV Erasable CMOS EPROM

Features

- Wide Power Supply Range, 3.0 VDC to 5.5 VDC
- Compatible with JEDEC Standard AT27C1024
- Low Power CMOS Operation
  - 100 µA max. Standby
  - 33 mW max. Active at 1 MHz for V_{CC} = 3.3 VDC
  - 165 mW max. Active at 5 MHz for V_{CC} = 5.5 VDC
- Read Access Time - 250 ns
- Wide Selection of JEDEC Standard Packages Including OTP
  - 40-Lead, 600-mil Cerdip and OTP Plastic DIP
  - 44-Pad LCC and OTP PLCC
- High Reliability CMOS Technology
  - 2000 V ESD Protection
  - 200 mA Latchup Immunity
- Rapid Programming - 100 µs/word (typical)
- Two-line Control
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

Description

The AT27LV1024 chip is a low-power, low voltage 1,048,576-bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized 64K x 16. It requires only one power supply in the range of 3.0 to 5.5 VDC in normal read mode operation. Any word can be accessed in less than 250 ns, eliminating the need for speed reducing WAIT states. The by-16 organization makes these parts ideal for high-performance 16- and 32-bit microprocessor systems.

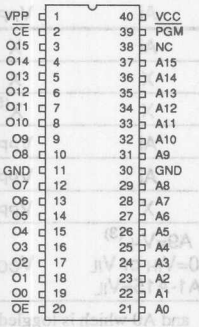
With a typical power draw of only 20 mW at 1 MHz and VCC at 3.3 VDC, the AT27LV1024 will draw less than one-fifth the power of a standard 5-V EPROM. Standby mode supply current is typically less than 10 µA.

Pin Configurations

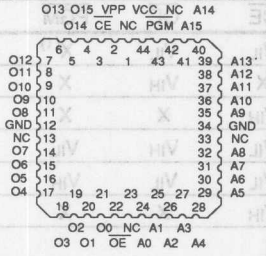
Pin Name	Function
A0-A15	Addresses
O0-O15	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Strobe
NC	No Connect

Note: Both GND pins must be connected.

CDIP, PDIP Top View



PLCC, LCC, JLCC Top View



Note: PLCC Package Pins 1 and 23 are DON'T CONNECT.

Description (Continued)

The AT27LV1024 comes in a choice of industry standard JEDEC-approved packages including; 40-pin DIP in ceramic or one time programmable (OTP) plastic, and 44-pad ceramic leadless chip carrier (LCC), or OTP plastic J-leaded chip carrier (PLCC). All devices feature two line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

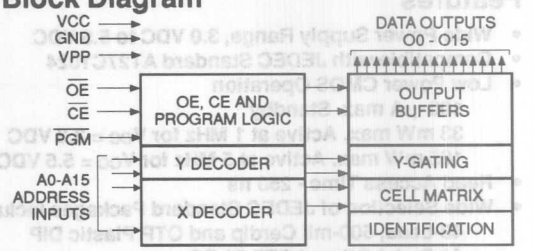
With high density 64K word storage capability, the AT27LV1024 allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's 27LV1024 has additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/word. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Erasure Characteristics

The entire memory array of the AT27LV1024 is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 µW/cm^2 intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 W·sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Voltage on A9 with Respect to Ground	-2.0 V to +14.0 V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0 V to +14.0 V(1)
Integrated UV Erase Dose	7258 W•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC}+0.75 V dc which may be exceeded if certain precautions are observed (consult application notes) and which may overshoot to +7.0 V for pulses of less than 20 ns.

Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	Ai	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X(1)	Ai	X	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	X	X	X	V_{CC}	High Z
Standby	V_{IH}	X	X	X	X(5)	V_{CC}	High Z
Rapid Program(2)	V_{IL}	V_{IH}	V_{IL}	Ai	V_{PP}	V_{CC}	D_{IN}
PGM Verify	V_{IL}	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC}	D_{OUT}
PGM Inhibit	V_{IH}	X	X	X	V_{PP}	V_{CC}	High Z
Product Identification(4)	V_{IL}	V_{IL}	X	A9=V_H (3) A0=V_{IH} or V_{IL} A1-A15=V_{IL}	V_{CC}	V_{CC}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. V_H = 12.0 ± 0.5 V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.
5. Standby V_{CC} current (I_{SB}) is specified with V_{PP}=V_{CC}. V_{CC} > V_{PP} will cause a slight increase in I_{SB}.

D.C. and A.C. Operating Conditions for Read Operation

		AT27LV1024 -25	AT27LV1024 -30
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5 V ± 10%	5 V ± 10%

D.C. and Operating Characteristics for Read Operation

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1 V to V_{CC}+1 V			5	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1 V to V_{CC}+0.1 V			10	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = 3.8 to V_{CC}+0.3 V			10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS) $\overline{CE}$ = V_{CC}-0.3 to V_{CC}+1.0 V			100	µA
		I_{SB2} (TTL) $\overline{CE}$ = 2.0 to V_{CC}+1.0 V			1	mA
I_{CC}	V_{CC} Active Current	I_{CC1} f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}, V_{CC} = 5.5 V	Com.		30	mA
			Ind.		40	mA
		I_{CC2} f = 1 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}, V_{CC} = 3.3 V	Com.		10	mA
			Ind.		12	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC}+.75 V	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			.45	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA		V_{CC}-0.3		V
		I_{OH} = -2.5 mA		3.5		V
		I_{OH} = -400 µA		2.4		V

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

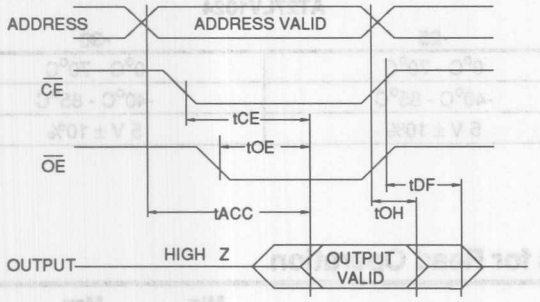
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

A.C. Characteristics for Read Operation

Symbol	Parameter	Condition	AT27LV1024 -25 Min	AT27LV1024 -25 Max	AT27LV1024 -30 Min	AT27LV1024 -30 Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		250		300	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		250		300	ns
t_{OE} (2,3)	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}		100		150	ns
t_{DF} (4,5)	$\overline{OE}$ High to Output Float	$\overline{CE}$ = V_{IL}		50		50	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0		0		ns

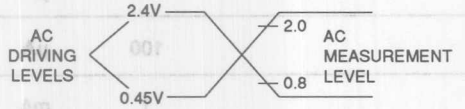
Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

A.C. Waveforms for Read Operation [1,2,3,4,5]



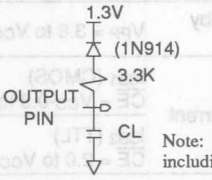
Notes:
1. Timing measurement references are 0.8 V and 2.0 V. Input AC driving levels are 0.45 V and 2.4 V, unless otherwise specified.
2. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

Input Test Waveforms and Measurement Levels



t_R, t_F < 20 ns (10% to 90%)

Output Test Load



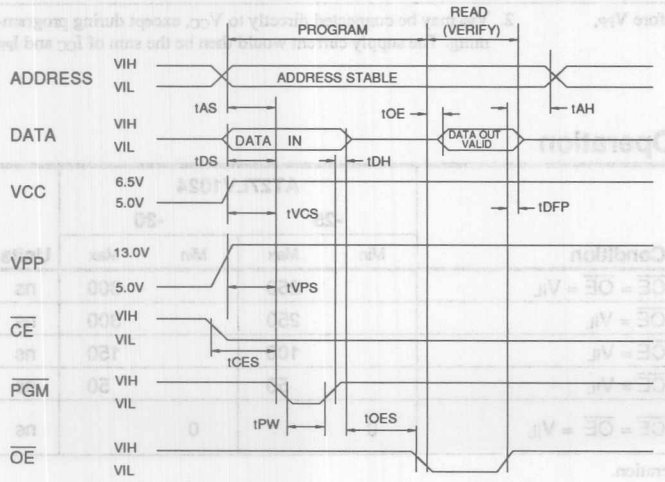
Note: C_L = 100 pF including jig capacitance.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	8	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes:
1. The Input Timing Reference is 0.8 V for V_{IL} and 2.0 V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27LV1024 a 0.1-µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

D.C. Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25$ V, $V_{PP} = 13.0 \pm 0.25$ V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	$V_{CC}+1$	V
V_{OL}	Output Low Volt.	I_{OL}=2.1 mA		.45	V
V_{OH}	Output High Volt.	I_{OH}=-400 µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			50	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE}=\overline{PGM}=V_{IL}$		30	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25$ V, $V_{PP} = 13.0 \pm 0.25$ V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Limits Max	Units
t_{AS}	Address Setup Time		2		µs
t_{CES}	$\overline{CE}$ Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{PGM}$ Program Pulse Width	(Note 3)	95	105	µs
t_{OE}	Data Valid from $\overline{OE}$			150	ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) ..... 20 ns
Input Pulse Levels ..... 0.45 V to 2.4 V
Input Timing Reference Level ..... 0.8 V to 2.0 V
Output Timing Reference Level ..... 0.8 V to 2.0 V

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100 µsec ± 5%.

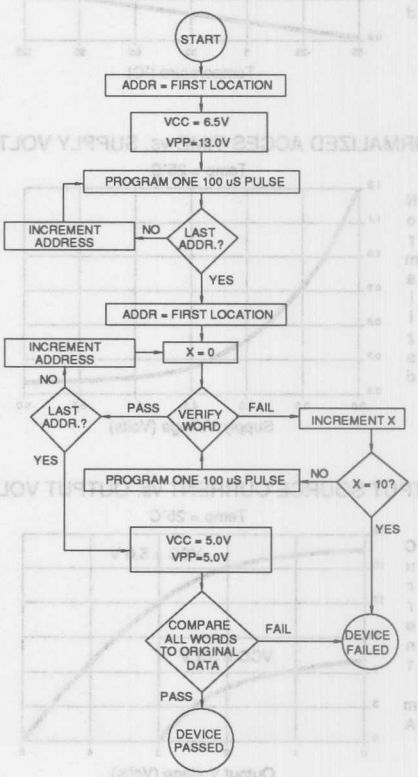
Atmel's 27LV1024 Integrated Product Identification Code[1]

Codes	Pins A0	015-08	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	0	1	1	1	1	0	001E
Device Type	1	0	1	1	1	1	0	0	0	1	00F1

Note: 1. The AT27LV1024 has the same Product Identification Code as the AT27C1024. Both are programming compatible.

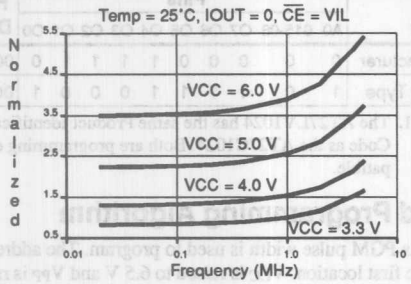
Rapid Programming Algorithm

A 100 µs $\overline{PGM}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5 V and V_{PP} is raised to 13.0 V. Each address is first programmed with one 100 µs $\overline{PGM}$ pulse without verification. Then a verification / reprogramming loop is executed for each address. In the event a word fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the word fails to verify after 10 pulses have been applied, the part is considered failed. After the word verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0 V and V_{CC} to 5.0 V. All words are read again and compared with the original data to determine if the device passes or fails.

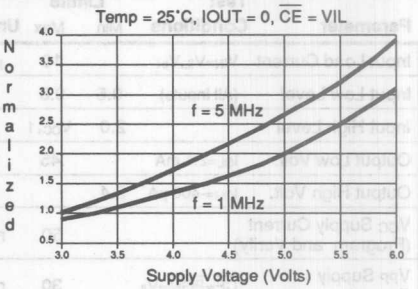


LV EPROM Product Characteristics

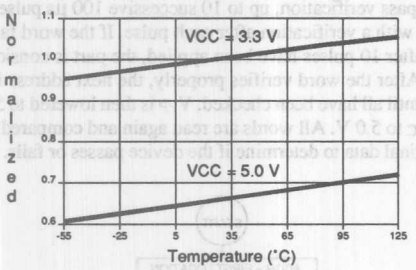
NORMALIZED SUPPLY CURRENT vs. FREQUENCY



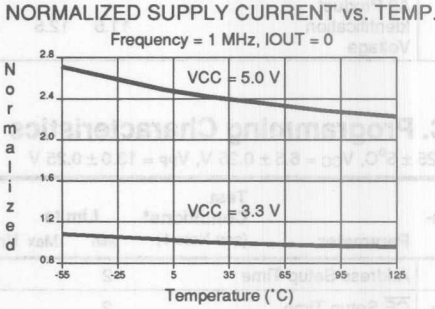
NORMALIZED SUPPLY CURRENT vs. VOLTAGE



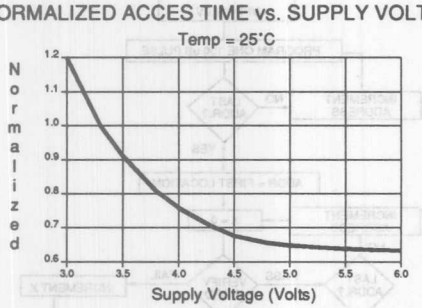
NORMALIZED ACCESS TIME vs. TEMPERATURE



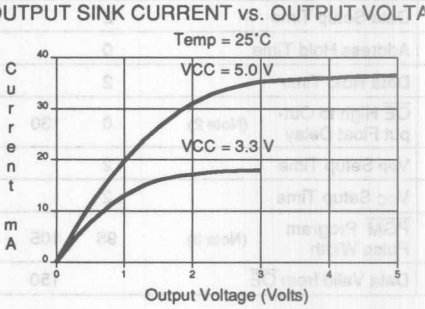
NORMALIZED SUPPLY CURRENT vs. TEMP.



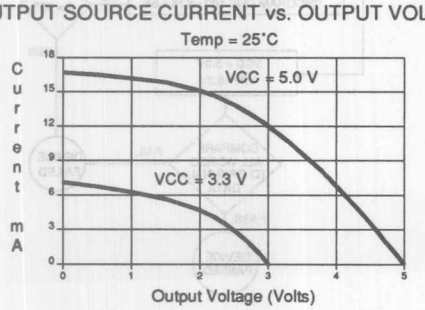
NORMALIZED ACCES TIME vs. SUPPLY VOLTAGE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
250	8	0.1	AT27LV1024-25DC AT27LV1024-25JC AT27LV1024-25KC AT27LV1024-25LC AT27LV1024-25PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
250	10	0.1	AT27LV1024-25DI AT27LV1024-25KI AT27LV1024-25LI	40DW6 44KW 44LW	Industrial (-40°C to 85°C)
300	8	0.1	AT27LV1024-30DC AT27LV1024-30JC AT27LV1024-30KC AT27LV1024-30LC AT27LV1024-30PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
300	10	0.1	AT27LV1024-30DI AT27LV1024-30KI AT27LV1024-30LI	40DW6 44KW 44LW	Industrial (-40°C to 85°C)

4

Package Type	
40DW6	40 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
44J	44 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
44KW	44 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
44LW	44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
40P6	40 Lead, 0.600" Wide, Plastic Dual Inline package OTP (PDIP)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
250	8	0.1	AT27LV1024-25DC AT27LV1024-25JC AT27LV1024-25KC AT27LV1024-25LC AT27LV1024-25PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
250	10	0.1	AT27LV1024-25DI AT27LV1024-25KI AT27LV1024-25LI	40DW6 44KW 44LW	Industrial (-40°C to 85°C)
300	8	0.1	AT27LV1024-30DC AT27LV1024-30JC AT27LV1024-30KC AT27LV1024-30LC AT27LV1024-30PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
300	10	0.1	AT27LV1024-30DI AT27LV1024-30KI AT27LV1024-30LI	40DW6 44KW 44LW	Industrial (-40°C to 85°C)

Package Type	
40DW6	40 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
44J	44 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
44KW	44 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
44LW	44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
40P6	40 Lead, 0.600" Wide, Plastic Dual Inline package OTP (PDIP)

Features

- **Fast Read Access Time - 100 ns**
- **Low Power CMOS Operation**
  - **100 µA max. Standby**
  - **25 mA max. Active at 5 MHz**
- **Wide Selection of JEDEC Standard Packages Including OTP**
  - **32-Lead 600-mil Cerdip and OTP Plastic DIP, or TSOP**
  - **32-Pad LCC and OTP PLCC**
- **5 V ± 10% Supply**
- **High Reliability CMOS Technology**
  - **2000 V ESD Protection**
  - **200 mA Latchup Immunity**
- **Rapid Programming - 100 µs/byte (typical)**
- **Two-line Control**
- **CMOS and TTL Compatible Inputs and Outputs**
- **Integrated Product Identification Code**
- **Full Military, Industrial and Commercial Temperature Ranges**

4 Megabit (512K x 8) UV Erasable CMOS EPROM

4

Description

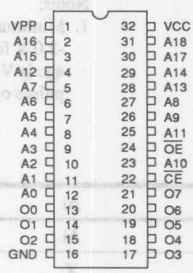
The AT27C040 chip family is a low-power, high-performance 4,194,304 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized as 512K x 8 bits. The AT27C040 requires only one 5-V power supply in normal read mode operation. Any byte can be accessed in less than 100 ns, eliminating the need for speed reducing WAIT states on high-performance microprocessor systems.

Atmel's 1.0-micron scaled CMOS technology provides for significantly lower active power consumption than competing designs. Power consumption is typically 8 mA in active mode and less than 10 µA in standby mode.

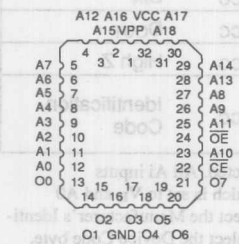
Pin Configurations

Pin Name	Function
A0-A18	Addresses
O0-O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable

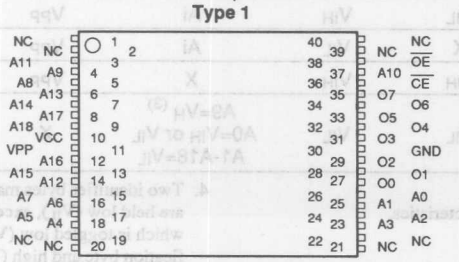
CDIP, PDIP, Top View



LCC, PLCC Top View



TSOP Top View
Type 1



Description (Continued)

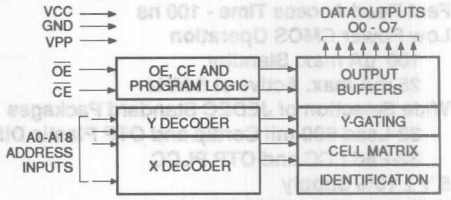
The AT27C040 comes in a choice of industry standard JEDEC-approved through hole and surface mount packages including windowed and one-time programmable (OTP) packages, such as the OTP thin snall outline package (TSOP). All devices feature two line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to avoid bus contention.

Atmel's AT27C040 has additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Erasure Characteristics

The entire memory array of the AT27C040 is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 $W \cdot sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Voltage on A9 with Respect to Ground	-2.0 V to +14.0 V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0 V to +14.0 V(1)
Integrated UV Erase Dose	7258 W•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75 V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	Ai	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	Ai	X(1)	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	X	X	V_{CC}	High Z
Standby	V_{IH}	X	X	X	V_{CC}	High Z
Fast Program(2)	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC}	D_{IN}
PGM Verify	X	V_{IL}	Ai	V_{PP}	V_{CC}	D_{OUT}
PGM Inhibit	V_{IH}	V_{IH}	X	V_{PP}	V_{CC}	High Z
Product Identification(4)	V_{IL}	V_{IL}	A9=V_H (3) A0=V_{IH} or V_{IL} A1-A18=V_{IL}	X	V_{CC}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. $V_H = 12.0 \pm 0.5$ V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

D.C. and A.C. Operating Conditions for Read Operation

		AT27C040			
		-10	-12	-15	-20
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.		-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 5%	5 V ± 10%	5 V ± 10%	5 V ± 10%

4

D.C. and Operating Characteristics for Read Operation

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1 V to V_{CC}+1 V			5	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1 V to V_{CC}+0.1 V			10	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = 3.8 to V_{CC}+0.3 V			10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC}-0.3 to V_{CC}+1.0 V			100	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC}+1.0 V			1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}	Com.		25	mA
			Ind.,Mil.		30	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC}+0.75	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			.45	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA		V_{CC}-0.3		V
		I_{OH} = -2.5 mA		3.5		V
		I_{OH} = -400 µA		2.4		V

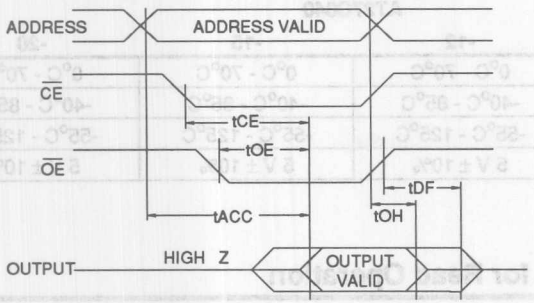
Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

A.C. Characteristics for Read Operation

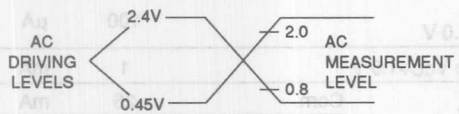
				AT27C040								
				-10		-12		-15		-20		
Symbol	Parameter	Condition		Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Com.		100		120		150		200	ns
			Ind.,Mil.				120		150		200	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}			100		120		150		200	ns
t_{OE} (2,3)	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}			35		35		40		70	ns
t_{DF} (4,5)	$\overline{OE}$ High to Output Float	$\overline{CE}$ = V_{IL}			35		35		40		55	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		0		0		0		0		ns

Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.



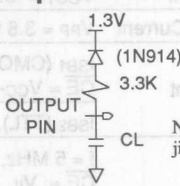
Notes:
1. Timing measurement references are 0.8 V and 2.0 V. Input AC driving levels are 0.45 V and 2.4 V, unless otherwise specified.
2. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

Input Test Waveforms and Measurement Levels



t_R, t_F < 20 ns (10% to 90%)

Output Test Load



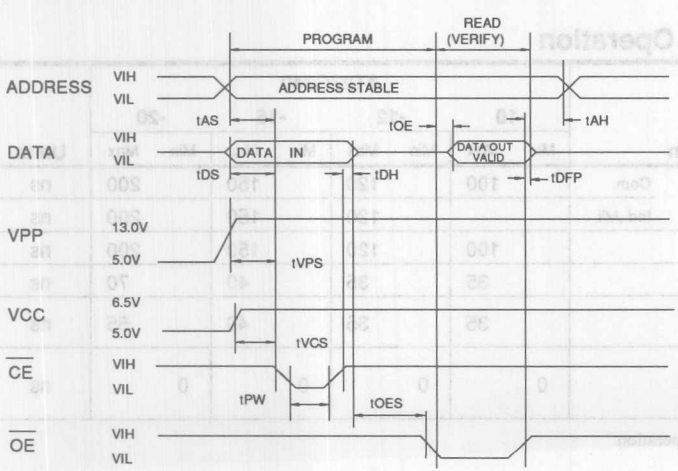
Note: C_L = 100 pF including jig capacitance.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	8	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes:
1. The Input Timing Reference is 0.8 V for V_{IL} and 2.0 V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27C040 a 0.1-µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

D.C. Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25$ V, $V_{PP} = 13.0 \pm 0.25$ V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	$V_{CC}+.7$	V
V_{OL}	Output Low Volt.	$I_{OL}=2.1$ mA		.45	V
V_{OH}	Output High Volt.	$I_{OH}=-400$ µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			40	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE}=V_{IL}$		20	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25$ V, $V_{PP} = 13.0 \pm 0.25$ V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Limits Max	Units
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CE}$ Program Pulse Width	(Note 3)	95	105	µs
t_{OE}	Data Valid from $\overline{OE}$	(Note 2)		150	ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) ..... 20 ns
Input Pulse Levels ..... 0.45 V to 2.4 V
Input Timing Reference Level ..... 0.8 V to 2.0 V
Output Timing Reference Level ..... 0.8 V to 2.0 V

Notes:

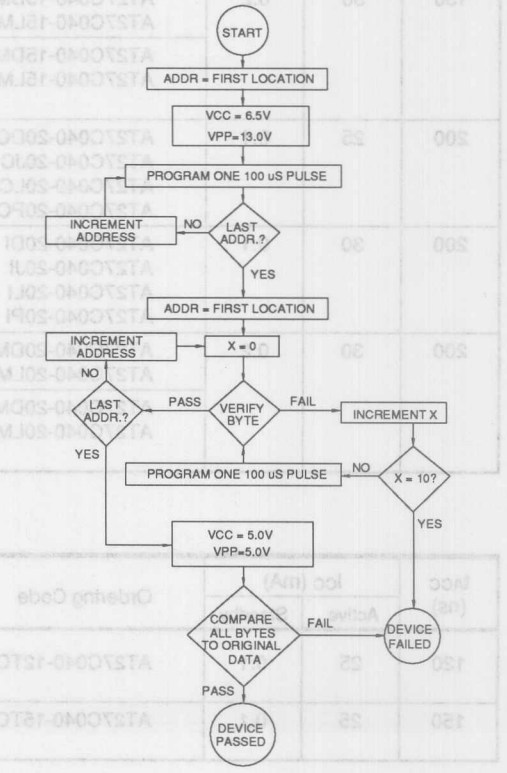
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100 µsec ± 5%.

Atmel's 27C040 Integrated Product Identification Code

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	0	0	0	0	1	0	1	1	0B

Rapid Programming Algorithm

A 100 µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5 V and V_{PP} is raised to 13.0 V. Each address is first programmed with one 100 µs $\overline{CE}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0 V and V_{CC} to 5.0 V. All bytes are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
100	25	0.1	AT27C040-10DC AT27C040-10LC	32DW6 32LW	Commercial (0°C to 70°C)
120	25	0.1	AT27C040-12DC AT27C040-12JC AT27C040-12LC AT27C040-12PC	32DW6 32J 32LW 32P6	Commercial (0°C to 70°C)
120	30	0.1	AT27C040-12DI AT27C040-12JI AT27C040-12LI AT27C040-12PI	32DW6 32J 32LW 32P6	Industrial (-40°C to 85°C)
150	25	0.1	AT27C040-15DC AT27C040-15JC AT27C040-15LC AT27C040-15PC	32DW6 32J 32LW 32P6	Commercial (0°C to 70°C)
150	30	0.1	AT27C040-15DI AT27C040-15JI AT27C040-15LI AT27C040-15PI	32DW6 32J 32LW 32P6	Industrial (-40°C to 85°C)
150	30	0.2	AT27C040-15DM AT27C040-15LM	32DW6 32LW	Military (-55°C to 125°C)
			AT27C040-15DM/883 AT27C040-15LM/883	32DW6 32LW	Military/883D Class B, Fully Compliant (-55°C to 125°C)
200	25	0.1	AT27C040-20DC AT27C040-20JC AT27C040-20LC AT27C040-20PC	32DW6 32J 32LW 32P6	Commercial (0°C to 70°C)
200	30	0.1	AT27C040-20DI AT27C040-20JI AT27C040-20LI AT27C040-20PI	32DW6 32J 32LW 32P6	Industrial (-40°C to 85°C)
200	30	0.2	AT27C040-20DM AT27C040-20LM	32DW6 32LW	Military (-55°C to 125°C)
			AT27C040-20DM/883 AT27C040-20LM/883	32DW6 32LW	Military/883D Class B, Fully Compliant (-55°C to 125°C)

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	25	0.1	AT27C040-12TC	40T	Commercial (0°C to 70°C)
150	25	0.1	AT27C040-15TC	40T	Commercial (0°C to 70°C)

Package Type	
32DW6	32 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
40T	40 Lead, Plastic Thin Small Outline Package OTP (TSOP)

	Package Type
32DW6	32 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
40T	40 Lead, Plastic Thin Small Outline Package OTP (TSOP)

Features

- Wide Power Supply Range, 3.0 VDC to 5.5 VDC
- Compatible with JEDEC Standard AT27C040
- Low Power 3-Volt CMOS Operation
  - 100 µA max. Standby
  - 26 mW max. Active at 1 MHz for V_{CC} = 3.3 VDC
  - 138 mW max. Active at 5 MHz for V_{CC} = 5.5 VDC
- Read Access Time - 200 ns
- Wide Selection of JEDEC Standard Packages Including OTP
  - 32-Lead, 600-mil Cerdip and OTP Plastic DIP, or TSOP
  - 32-Pad LCC and OTP PLCC
- High Reliability CMOS Technology
  - 2000 V ESD Protection
  - 200 mA Latchup Immunity
- Rapid Programming - 100 µs/byte (typical)
- Two-line Control
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

Description

The AT27LV040 chip is a low power, low voltage 4,194,304 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized as 512K x 8 bits. It requires only one supply in the range of 3.0 to 5.5 VDC in normal read mode operation, making it ideal for battery powered systems.

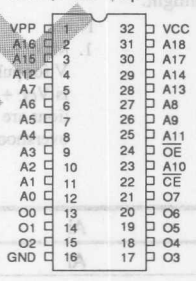
With a typical power draw of only 18 mW at 1 MHz and V_{CC} at 3.3 VDC, the AT27LV040 will draw less than one-fifth the power of a standard 5-volt EPROM. Standby mode supply current is typically less than 10 µA.

continued on next page

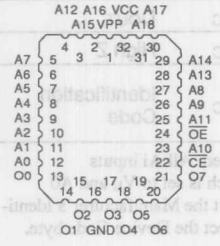
Pin Configurations

Pin Name	Function
A0-A18	Addresses
O0-O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable

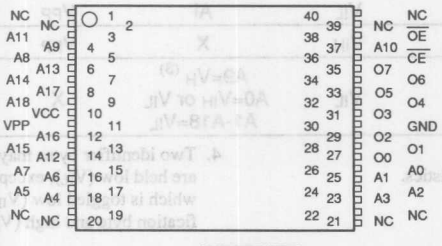
CDIP, PDIP Top View



PLCC, LCC Top View



TSOP Top View
Type 1



4 Megabit (512K x 8) Low Voltage UV Erasable CMOS EPROM

Preliminary

PRELIMINARY

Description (Continued)

The AT27LV040 comes in a choice of industry standard JEDEC-approved through hole and surface mount packages including windowed and one time programmable (OTP) packages, such as the OTP thin small outline package (TSOP). All devices feature two line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

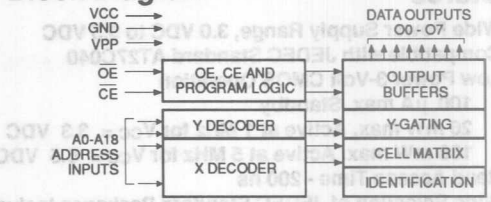
The AT27LV040 operating with V_{CC} at 3.0 VDC produces TTL level outputs that are compatible with standard TTL logic devices operating at V_{CC} = 5.0 VDC.

Atmel's 27LV040 has additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages. The AT27LV040 programs identically as an AT27C040.

Erasure Characteristics

The entire memory array of the AT27LV040 is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 µW/cm^2 intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 W·sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +125°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Voltage on A9 with Respect to Ground	-2.0 V to +14.0 V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0 V to +14.0 V(1)
Integrated UV Erase Dose	7258 W·sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75 V dc which may be exceeded if certain precautions are observed (consult application notes) and which may overshoot to +7.0 V for pulses of less than 20 ns.

Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	Ai	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	Ai	X(1)	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	X	X	V_{CC}	High Z
Standby	V_{IH}	X	X	X	V_{CC}	High Z
Fast Program(2)	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC}	D_{IN}
PGM Verify	X	V_{IL}	Ai	V_{PP}	V_{CC}	D_{OUT}
PGM Inhibit	V_{IH}	V_{IH}	X	V_{PP}	V_{CC}	High Z
Product Identification(4)	V_{IL}	V_{IL}	A9=V_H (3) A0=V_{IH} or V_{IL} A1-A18=V_{IL}	X	V_{CC}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. V_H = 12.0 ± 0.5 V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

D.C. and A.C. Operating Conditions for Read Operation

		AT27LV040		
		-20	-25	-30
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		3.0 V to 5.5 V	3.0 V to 5.5 V	3.0 V to 5.5 V

4

D.C. and Operating Characteristics for Read Operation

(V_{CC} = 3.0 V to 5.5 V unless otherwise specified)

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1 V to V_{CC}+1 V			5	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1 V to V_{CC}+0.1 V			10	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}-0.7 V to V_{CC}+0.3 V			10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC}-0.3 to V_{CC}+1.0 V			100	µA
		I_{SB2} (TTL), $\overline{CE}$= 2.0 to V_{CC}+1.0 V			1	mA
I_{CC}	V_{CC} Active Current	I_{CC1} f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}, V_{CC} = 5.5 V	Com.		25	mA
			Ind.		30	mA
		I_{CC2} f = 1 MHz, I_{OUT} = 0 mA $\overline{CE}$ = V_{IL}, V_{CC} = 3.3 V	Com.		8	mA
			Ind.		10	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC}+0.75	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			.45	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA		V_{CC}-0.3		V
		I_{OH} = -400 µA		2.4		V

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

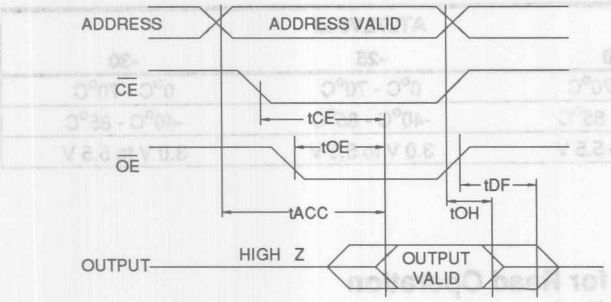
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

A.C. Characteristics for Read Operation (V_{CC} = 3.0V to 5.5V)

			AT27LV040						
			-20		-25		-30		
Symbol	Parameter	Condition	Min	Max	Min	Max	Min	Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$= V_{IL}		200		250		270	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		200		250		300	ns
t_{OE} (2,3)	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}		100		120		150	ns
t_{DF} (4,5)	$\overline{OE}$ High to Output Float	$\overline{CE}$ = V_{IL}		50		50		50	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0		0		0		ns

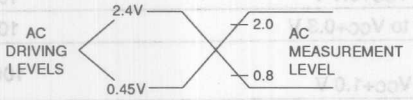
Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

A.C. Waveforms for Read Operation [1]



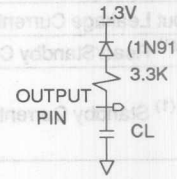
Notes:
1. Timing measurement references are 0.8 V and 2.0 V. Input AC driving levels are 0.45 V and 2.4 V. See Input Test Waveforms and Measurement Levels.
2. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

Input Test Waveforms and Measurement Levels



t_R, t_F < 20 ns (10% to 90%)

Output Test Load



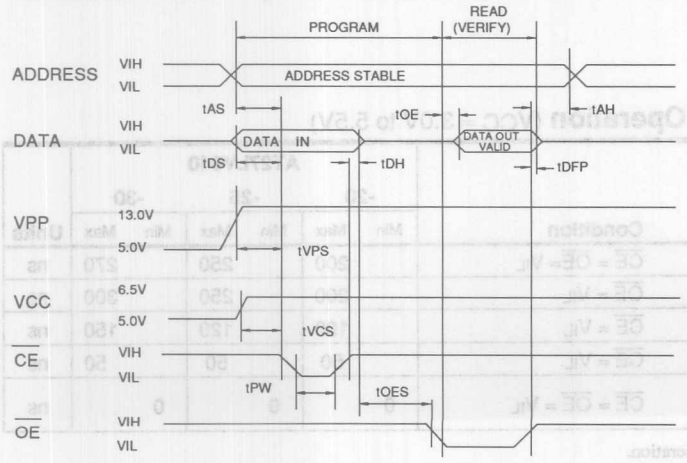
Note: C_L = 100 pF including jig capacitance.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	8	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Notes: 1. Typical values for 5-V supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes:
1. The Input Timing Reference is 0.8 V for V_{IL} and 2.0 V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27LV040 a 0.1-µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

D.C. Programming Characteristics

$T_A = 25 \pm 5^oC$, $V_{CC} = 6.5 \pm 0.25$ V, $V_{PP} = 13.0 \pm 0.25$ V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	$V_{CC}+1$	V
V_{OL}	Output Low Volt.	I_{OL}=2.1 mA		.45	V
V_{OH}	Output High Volt.	I_{OH}=-400 µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			40	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE}=V_{IL}$		20	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

$T_A = 25 \pm 5^oC$, $V_{CC} = 6.5 \pm 0.25$ V, $V_{PP} = 13.0 \pm 0.25$ V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Limits Max	Units
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CE}$ Program Pulse Width	(Note 3)	95	105	µs
t_{OE}	Data Valid from $\overline{OE}$	(Note 2)		150	ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) ..... 20 ns
Input Pulse Levels ..... 0.45 V to 2.4 V
Input Timing Reference Level ..... 0.8 V to 2.0 V
Output Timing Reference Level ..... 0.8 V to 2.0 V

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100 µsec ± 5%.

Atmel's 27LV040 Integrated Product Identification Code[1]

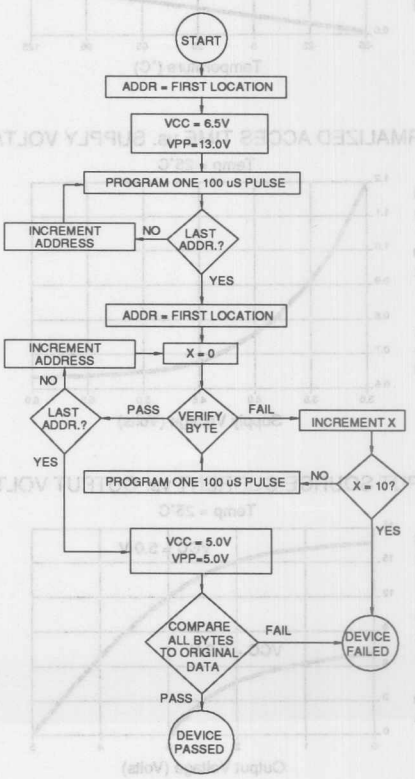
Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	0	0	0	0	1	0	1	1	0B

Note: 1. The AT27LV040 has the same Product Identification Code as the AT27C040. Both are programming compatible.

4

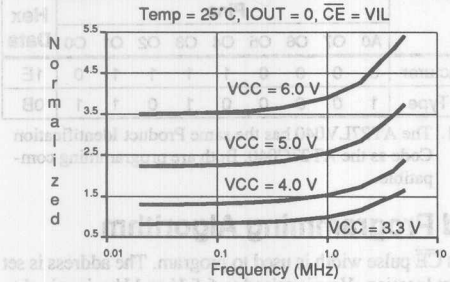
Rapid Programming Algorithm

A 100 µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5 V and V_{PP} is raised to 13.0 V. Each address is first programmed with one 100 µs $\overline{CE}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0 V and V_{CC} to 5.0 V. All bytes are read again and compared with the original data to determine if the device passes or fails.

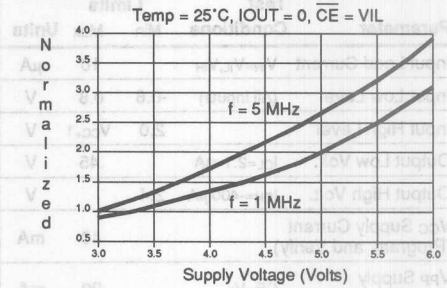


LV EPROM Product Characteristics

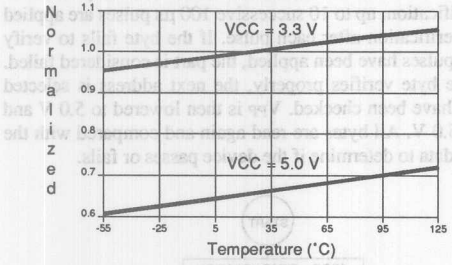
NORMALIZED SUPPLY CURRENT vs. FREQUENCY



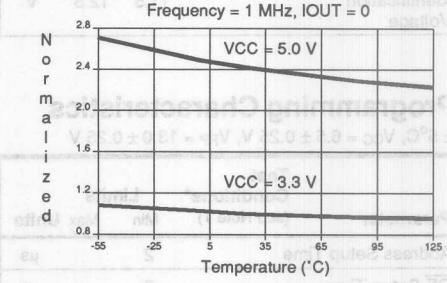
NORMALIZED SUPPLY CURRENT vs. VOLTAGE



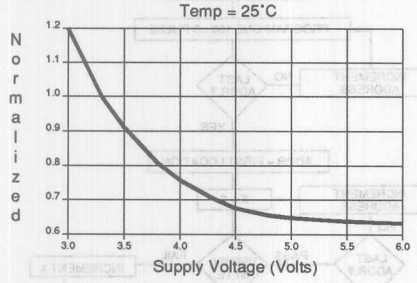
NORMALIZED ACCESS TIME vs. TEMPERATURE



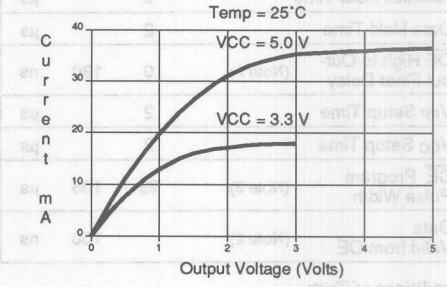
NORMALIZED SUPPLY CURRENT vs. TEMP.



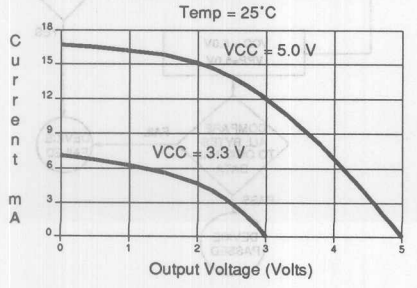
NORMALIZED ACCES TIME vs. SUPPLY VOLTAGE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



Ordering Information

t_{ACC} (ns)	I_{CC} (mA) V_{CC} = 3.3 V		Ordering Code	Package	Operation Range
	Active	Standby			
200	8	0.1	AT27LV040-20DC AT27LV040-20LC	32DW6 32LW	Commercial (0°C to 70°C)
200	10	0.1	AT27LV040-20DI AT27LV040-20LI	32DW6 32LW	Industrial (-40°C to 85°C)
250	8	0.1	AT27LV040-25DC AT27LV040-25LC	32DW6 32LW	Commercial (0°C to 70°C)
250	10	0.1	AT27LV040-25DI AT27LV040-25LI	32DW6 32LW	Industrial (-40°C to 85°C)
300	8	0.1	AT27LV040-30DC AT27LV040-30JC AT27LV040-30LC AT27LV040-30PC	32DW6 32J 32LW 32P6	Commercial (0°C to 70°C)
300	10	0.1	AT27LV040-30DI AT27LV040-30LI	32DW6 32LW	Industrial (-40°C to 85°C)

t_{ACC} (ns)	I_{CC} (mA) V_{CC} = 3.3 V		Ordering Code	Package	Operation Range
	Active	Standby			
250	8	0.1	AT27LV040-25TC	40T	Commercial (0°C to 70°C)
300	8	0.1	AT27LV040-30TC	40T	Commercial (0°C to 70°C)

Package Type	
32DW6	32 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
40T	40 Lead, Plastic Thin Small Outline Package OTP (TSOP)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA) V_{CC} = 3.3 V Active	Standby	Ordering Code	Package	Operation Range
200	8	0.1	AT27LV040-20DC AT27LV040-20JC	32DW6 32LW	Commercial (0°C to 70°C)
200	10	0.1	AT27LV040-20DI AT27LV040-20JI	32DW6 32LW	Industrial (-40°C to 85°C)
250	8	0.1	AT27LV040-25DC AT27LV040-25JC	32DW6 32LW	Commercial (0°C to 70°C)
250	10	0.1	AT27LV040-25DI AT27LV040-25JI	32DW6 32LW	Industrial (-40°C to 85°C)
300	8	0.1	AT27LV040-30DC AT27LV040-30JC AT27LV040-30LC AT27LV040-30PC	32DW6 32J 32LW 32P6	Commercial (0°C to 70°C)
300	10	0.1	AT27LV040-30DI AT27LV040-30JI	32DW6 32LW	Industrial (-40°C to 85°C)

t_{ACC} (ns)	I_{CC} (mA) V_{CC} = 3.3 V Active	Standby	Ordering Code	Package	Operation Range
250	8	0.1	AT27LV040-25TC	40T	Commercial (0°C to 70°C)
300	8	0.1	AT27LV040-30TC	40T	Commercial (0°C to 70°C)

Package Type	
32DW6	32 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
40T	40 Lead, Plastic Thin Small Outline Package OTP (TSOP)

Interfacing Atmel LV EPROMs on a Mixed Three-Volt/Five-Volt Data Bus

Introduction

Interfacing Atmel Corporation's low voltage (LV) EPROMs on a common data bus with standard five-volt devices can be achieved with relative ease if a few simple guidelines are followed. By controlling the data bus voltages and currents, problems associated with latchup, electromigration and battery damage can be eliminated. This application note describes each problem, along with recommended solutions, and analyzes the associated trade-offs.

Background

Definition of Terms:

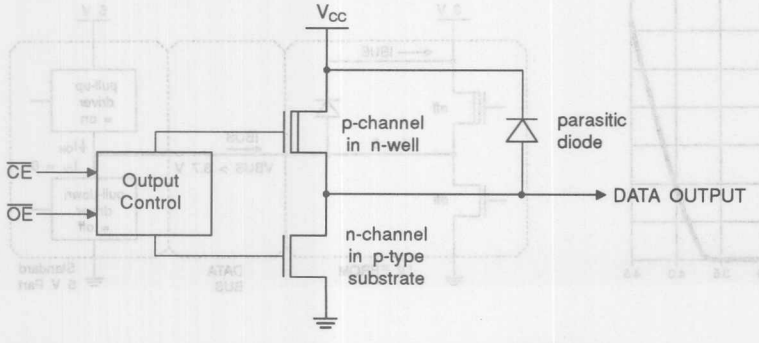
A. *Latchup* – a destructive phenomenon associated with CMOS-based semiconductors. Parasitic SCRs (silicon-controlled rectifiers or p-n-p-n devices) exist on inputs and outputs. Once an SCR is activated, it can conduct high current. The current can only be turned off by disconnecting the power supply.

B. *Electromigration* – Metal interconnects in semiconductors are carefully sized to ensure they are wide enough to safely carry the amount of current required by the design. The interconnects may physically open up when these limits are exceeded for a long time.

C. *Venting* – When a battery overheats (as a result of dissipating excessive power) the battery case may open, allowing the contents of the battery to be "vented" or leaked to the outside world. This is both messy and potentially dangerous.

Understanding issues related to interfacing Atmel LV EPROMs with standard five-volt devices requires an understanding of the EPROM output. The output is basically a CMOS inverter constructed with p-channel pull-up and n-channel pull-down transistors (see Figure 1). The source of the p-channel and the n-well are connected to V_{CC}. The source of the n-channel and the substrate are connected to ground. It is important to note that the p+ drain of the p-channel device in the n-well forms a parasitic p-n diode. The parasitic diode is between the output of the LV part and the V_{CC} supply, with the diode cathode connected to V_{CC} and the anode connected to the output node. If the Atmel LV EPROM is operated from a three-volt supply and the output node rises to 3.7 volts, the parasitic p-n junction is forward biased by 0.7 volts and will conduct current. This diode current will flow even though the LV EPROM output is supposed

Figure 1. Atmel LV CMOS EPROM Output Buffer



to be tri-stated (high-Z) via the CE or OE control signals. The room temperature I/V characteristic of the diode is shown in Figure 2. The y-axis of the graph, designated "IBUS," represents the DC current flowing from the bus into the Atmel LV EPROM output. The x-axis, designated "VBUS," is the data bus voltage when the supply level of the LV EPROM is exactly 3.0 volts. For example, if the voltage on the data bus is 4.0 volts, the corresponding diode current into the LV part's output is approximately 20 mA. If VBUS is increased to 4.5 volts, the corresponding diode current in just one output increases to 60 mA, and would be destructive over time. It is important to note that the LV EPROM data sheets refer to output pin voltage. The data sheet section under "Absolute Maximum Ratings" specifically states that the "Maximum output pin voltage is V_{CC} + 0.75 VDC which may be exceeded if certain precautions are observed." What does this mean? It means that, because of the effects demonstrated by the parasitic diode, voltages on the output pins in excess of V_{CC} + 0.75 volts can cause large currents to flow into the EPROM outputs and short the two power supplies together (see Figure 3).

Each Atmel EPROM output is designed to withstand an IBUS current of less than 10 mA without any exposure to electromigration, and over 200 mA without latchup. Since the current capability for latchup is so much larger than the amount of current required to induce electromigration, it is clear that the electromigration requirement will dictate the maximum IBUS current. The balance of this application note focuses on ensuring by system design that the magnitude of the IBUS current into the EPROM is less than 10 mA. The effects of exceeding the normal output voltage of the LV supply (over-volting) will not be discussed in detail here. Those characteristics should be obtained from the battery or voltage regulator manufacturers.

Results

Clearly, the most attractive design option is to select five-volt bus driver devices which do not have strong output drive current (I_{OH}) capability. An example of this type of device is a 8096 microcontroller. Its I_{OH} characteristic is shown in Figure 4. We are only concerned about how much I_{OH} (= IBUS) the 8096 can supply into the LV EPROM above a V_{OH} (= VBUS) of three volts. The maximum current the 8096 can supply when its V_{OH} is above three volts is less than the 10 mA allowed to safely enter the LV EPROM. Therefore, electromigration is not a concern in this case. However, allowing both power supplies to couple across the parasitic diode of the LV EPROM may still speed the discharge of a five-volt battery and may cause the three-volt battery to overheat and vent.

Contrast the 8096 example with the output characteristics of a high-current output drive 74HC00 CMOS logic gate (Figure 5). Note how the amount of I_{OH} current available above a three-volt V_{OH} can be 30 mA, more than triple the maximum safe IBUS current to prevent electromigration. What actual IBUS will occur when such a 74HC00 part (connected to a five-volt supply) is driving an Atmel LV EPROM (connected to a three-volt supply)? The answer can be obtained using a graphical technique called *load line analysis*.

With load line analysis, you can find the maximum DC IBUS and VBUS values for any situation. For example, continue the analysis for the 74HC00 part to see what the actual IBUS current will be. A load line is created by simply superimposing the Atmel LV EPROM IBUS versus VBUS curve (Figure 2) with the 74HC00 I_{OH} versus V_{OH} curve (Figure 5). Figure 6 is the resulting load line. The place the two curves intersect is called the *operating point* and gives an IBUS value of about 20 mA. The data bus will then sit at a VBUS voltage of about four volts. This analysis confirms the suspicion that using a 74HC00 will not be safe. Recall that you want an IBUS value below 10 mA to prevent reliability damage to the LV EPROM.

The type of curves used in this load line analysis can be easily obtained for any conditions and any part. You should beware to use curves obtained for the worst case conditions that the system will encounter. Most I_{OH} and V_{OH} data sheet specifications are minimum values and sometimes grossly understate the real current drive capability of a part. When was the last time you encountered a CMOS part with only 400 µA I_{OH} at 2.4-volts V_{OH}? Such a specification is a holdover from the days when an NMOS design was considered fast at 500 ns. Many data sheets

Figure 2. Atmel LV EPROM IBUS versus VBUS

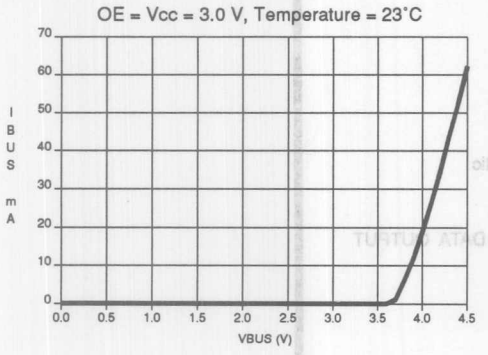
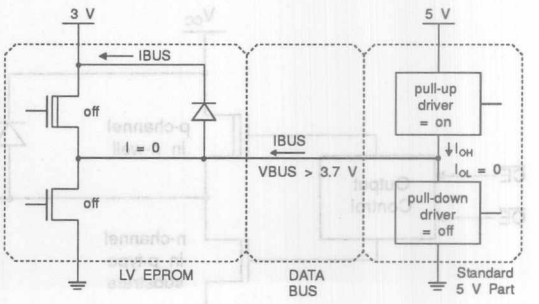


Figure 3. Parasitic Diode in LV Output Shorts Three-Volt and Five-Volt Supplies



provide output drive curves only for typical conditions (i.e., V_{CC} = 5 V, temperature = 25°C). Most data sheets also provide data for only the minimum output drive since most customers are worried if the part has enough current drive for a heavily loaded bus line. However, for this mixed power supply design analysis we need the maximum output drive current for the five-volt driven part. The conditions for that maximum output current would occur at lowest temperature and highest V_{CC}, and with only one output driving. The last condition is due to the parasitic resistance in a chip's package and die metal. That resistance will cause a voltage drop inside the chip that will decrease the output current drive. On parts with more than one output, the highest I_{OH} current will occur when the internal voltage drop is minimum or when only one output is driving. The variation in I_{OH} with number of outputs driving, V_{CC}, and temperature will exceed the variations due to processing in most chips today. You may have to measure the I_{OH} characteristics yourself to get the data you need.

The Atmel LV EPROM IBUS versus VBUS characteristics will also need to be measured at conditions giving the highest current for the load line operating point. That current will depend strongly on the V_{CC} used for the LV parts. The higher the LV V_{CC}, the higher the bus voltage can go before forward-biasing the parasitic diode in the LV part. For the load line analysis, the LV EPROM IBUS versus VBUS curve measured at V_{CC} = 3 V is shifted to the right by the difference between the LV supply voltage to be used and three volts. Increasing the LV V_{CC} will reduce IBUS quickly since I_{OH} for the five-volt part decreases rapidly as the operating point moves to the right. The worst case LV IBUS versus VBUS curve will be obtained for highest temperature, lowest V_{CC}, and a single output high. Figure 7 shows the LV EPROM IBUS as a function of VBUS for a range of temperatures from -55°C to 85°C.

In some applications, there may be requirements for a high output current five-volt device or no alternate part available with limited I_{OH}. The following techniques may be useful in that case. One technique is to clamp the bus with respect to ground. Clamp the bus so that the parasitic p-n junction in the LV part cannot be forward biased. A three-volt zener diode with grounded anode and cathode connected to the data bus can provide

Figure 4. I_{OH} versus V_{OH} for 8096

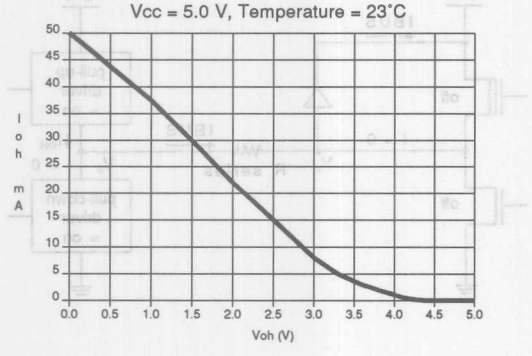


Figure 5. I_{OH} versus V_{OH} for 74HC00

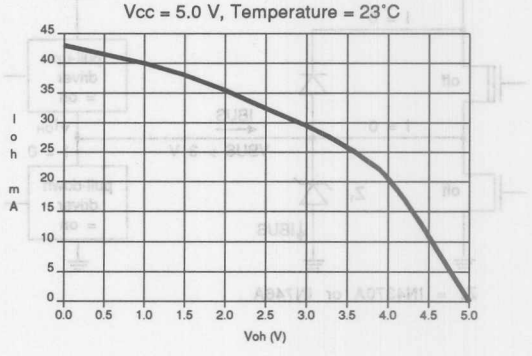


Figure 6. 74HC00 Load Line on LV EPROM

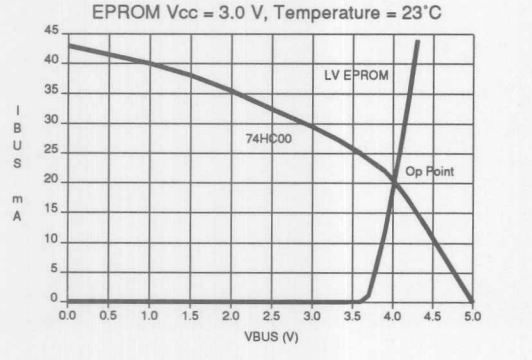
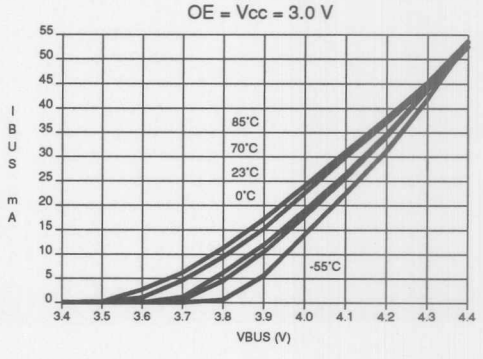


Figure 7. LV IBUS versus VBUS versus Temperature



1N4370A- or 1N746A-series zener diodes could be used. The trade-off is the power dissipated by the zeners. A three-volt zener shunting 20 mA of current will consume 60 mW of power. For eight outputs, this could be as high as 480 mW, which is a significant amount of power to waste in a battery environment. This will speed the discharge of the five-volt battery, but does a very good job of protecting the three-volt supply from over-volting (or possibly venting the three-volt battery).

Another technique is to add a small series resistor on each of the LV part's outputs (Figure 9). The resistor will limit the IBUS current. Figure 10 uses the 74HC00 example again to show how the load line plot from Figure 6 is used to quickly calculate the value of series resistance needed. You want to move the IBUS operating point from the original 20 mA down to 10 mA. The circuit consists of the original 74HC00 pull-up circuit, represented by the original load line, and the new series resistor. The current in the resistor and the pull-up will be the same since they are in series and should be set to our recommended safe 10 mA level. In Figure 10 you will see two points called V_a and V_b which are where the LV EPROM and 74HC00 pull-up load lines intersect the 10 mA IBUS current level. The difference between V_b and V_a will be the voltage drop across the series resistor when 10 mA of current is flowing. The series resistance Rseries is then calculated by the formula:

$$Rseries = (Vb - Va) / Idesired$$
$$= (4.55 - 3.85)\ V / 10\ mA$$
$$= 70\ ohms$$

The power dissipated in each resistor would be given by:

$$Pseries = Idesired^2 \times Rseries$$
$$= (10\ mA)^2 \times 70\ ohms$$
$$= 7\ mW$$

For eight outputs, the series resistor method only drains 56 mW from the five-volt supply, which is much less power than that wasted by the zener circuit. Notice that the three-volt supply will still be over-volted by 0.85 volts. You still need to determine

Figure 8. Zener Clamp Bus to Three Volts

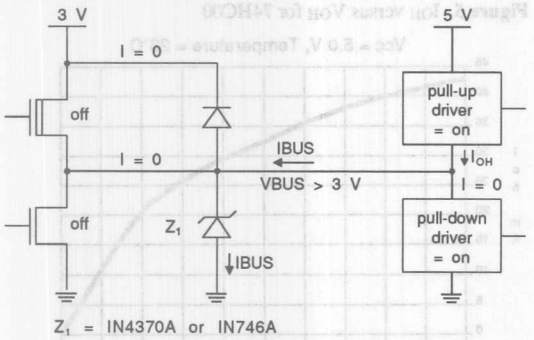
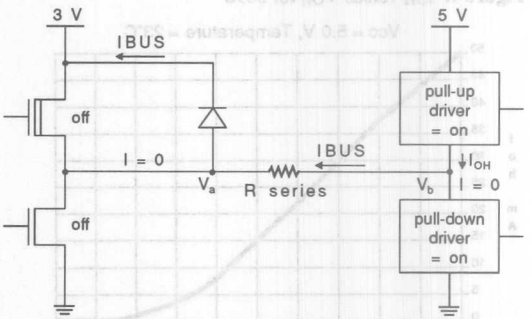
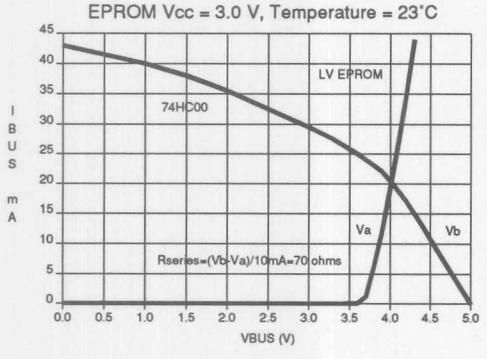


Figure 9. Series Output Resistor Reduces IBUS



if that over-volting will cause excessive battery heating and a possible venting problem. The resistor's effect on bus signal speed will probably not be detrimental since the 70 ohms needed in this example is just slightly higher than the value used for a series transmission line termination. It may be necessary to place the series resistors between the high output drive part and the common data bus. That way the resistors are only in the circuit when the high output part is driving the bus, and lower drive current parts will not be current-limited. Also, remember this example was done for room temperature and a five-volt supply on the 74HC00. For higher temperature, the 74HC00 will have less current drive, but the parasitic LV EPROM diode will start to forward bias at a lower VBUS value. You may need to do several load line models before finding a design that covers the worst case temperature and power supply conditions for a particular system.

Figure 10. Calculating Rseries for 74HC



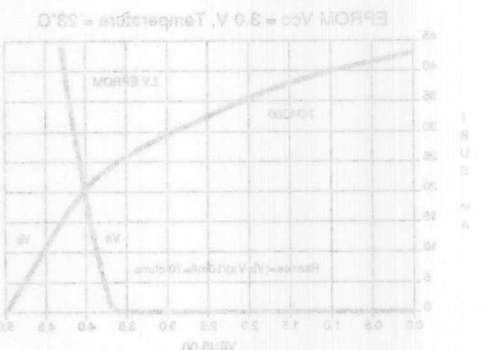
Conclusion

Interfacing Atmel LV EPROMs on a common data bus with standard five-volt devices can be achieved if the output drives of the five-volt powered parts are controlled through careful device selection or by adding external components. The problems to avoid are:

1) failure of the LV part due to electromigration, and

2) battery venting of the LV supply.

Following these guidelines will allow design of mixed power supply systems which exhibit sound component and system reliability.


LV EPROM
74HC00
Va
Vb
VBUS (V)

The Atmel Three-Volt EPROM Family AT27LV256R, AT27LV512R, AT27LV010

- Why three-volt operation?
- Does the whole system have to be operated at three volts?
- How do you program a three-volt EPROM?
- What happens if you run a three-volt device at 3.6 or 4.0 volts?

The Atmel AT27LVXXX series of EPROMs was designed to operate over a wide range of supply voltages from 3.0 to 5.5 volts. This offers the designer the opportunity to take advantage of either the greatly reduced power consumption at three volts or the ability to tolerate large power supply fluctuations.

The three-volt series of EPROMs is specified to draw a maximum of 8.0 mA at 3.3 MHz when operated at 3.3 VDC. This is one-fourth of the specified maximum current of a standard EPROM operating at 5.0 VDC. Because of the low supply voltage, the power savings calculations are even more dramatic: 26 mW for the LV series compared to 150 mW for standard five-volt devices. That means much longer battery life.

The LV series has CMOS inputs and outputs specified for TTL levels and three-volt CMOS levels (Rail-to-Rail). In other words, an LV device with V_{CC} = 3.0 VDC can drive standard five-volt TTL logic devices on its data output lines making interface with five-volt logic easy. The LV series of EPROMs can even be safely driven by five-volt signals, even though their V_{CC} is at 3.0 VDC. The next question that comes to mind is "Why run just one EPROM at three volts while the rest of the system uses five volts?" One reason is if your system is on a very tight power budget, such as battery operated equipment, daughter boards or phone line powered products, the six times power savings might make significant difference. Of course your design might use more than one EPROM, for map memory, operating system, font storage or maybe smart cards. In this case the total power savings can be very large. Remember at 150 mW each, eight EPROMs at five volts use 1.2 Watts instead of 210 mW for the three-volt devices!

When the three-volt devices are in a programmer they work just like their standard Atmel five-volt counterparts. Absolutely no difference! Programming support is already in place and widely available on most programmers on the market today. Again they erase and program exactly the same as five-volt devices.

The AT27LVXXX series of EPROMs are specified to operate from 3.0 to 5.5 volts. So what happens when the device is operated above three volts? It speeds up and draws more power, but never more than a standard EPROM. This feature offers the most flexibility for system manufacturers. The data sheets include a full set of curves that show speed and power variations versus power supply voltage.

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On-Board, System EPROM Programming with V_{CC} = 5 Volts

Present day EPROMs use V_{CC} = 6-6.25 V during programming. This non-5-volt supply level occasionally presents a system design problem with applications where a commercially available programmer cannot be used. This application note will briefly address the issues associated with using a 5-volt V_{CC} supply during programming.

Modern EPROM programming algorithms can be divided into two sections, namely, programming and verify (or read). The programming algorithm usually proceeds by selecting the desired voltage levels and address. A programming pulse is applied followed by a verify at the elevated V_{CC} used for programming.

During programming, the MOS threshold voltage (Vt) of a previously erased N-channel floating gate EPROM cell (Vt = 1.0-2.0 V) is raised to 6.5-9.0 V via the accumulation of electrons on the floating gate by hot electron injection. In normal read mode operation the address decoding circuitry in the chip selects the desired cell by pulling the gate voltage of the cell to V_{CC}. Since V_{CC} is typically 4.5-5.5 V, an erased cell with Vt = 1.5 V would be turned on while a programmed cell with Vt = 7.5 V would remain in an off state. If V_{CC} were raised above the threshold voltage for the programmed cell (i.e. V_{CC} > 7.5 V), the cell would begin to conduct and the programmed data would no longer be valid until V_{CC} was again lowered.

The V_{CC} voltage that causes data loss on a programmed EPROM is called the programming margin. During the programming algorithm the V_{CC} level is held at 6-6.25 V to make sure that each cell is guaranteed to have a programming margin at least to that level. This is verified by reading each byte twice, once during the initial programming section and again during a final read where all addresses are compared to the desired data.

The 0.5-V difference between the guaranteed programming margin and the 5.5-V V_{CC} maximum supply rating provides a reliability guardband for long term data charge retention and, more importantly, for system noise immunity. Poor programming margin can lead to EPROM memory chip instability which can cause apparently slower operation due to oscillations and false reading. This in turn makes the problem directly related to the specific system noise environment and will vary from application to application.

By lowering the V_{CC} voltage to 5.0 V during the programming algorithm two effects may occur. First, the part may not be able to program (i.e., programmed cell threshold = 5.0 V). Second, the part may not have enough programming margin to reliably work over worst case conditions over the lifetime of the part.

The first problem is rare since most manufacturers design their EPROM technology to provide a large programming margin guardband to account for statistical variations in the manufacturing process.

The second problem is also considerably reduced by the same margin guardband, but unlike the first problem which is easily detectable at the time of programming, the second problem may only occur later when the parts are in the field. The resulting field failure rate may still be acceptably small depending on the application.

The second problem may also result in a failure mode even when the nominal V_{CC} programming voltage is used. In that case standard accelerated reliability tests and statistical sampling techniques can be used to determine failure rates. But such test results only apply to parts with the same programming technique. Since those tests require great expenditure of labor, time, and units, significant reliability data for V_{CC} = 5 V programming is not readily available. An-

other way to get around the possible reliability problem is testing the parts in such a way so as to screen out any low margin parts. This specially tested group will then have the same programming margin as parts programmed at the nominal V_{CC} even when they are programmed using V_{CC} = 5 V.

We have discussed general EPROM operation for most currently available EPROM chips on the market today including Atmel's EPROM line. Atmel's chips specifically do not have any programming problem "of the first kind" with V_{CC} = 5 V. This is due to the proprietary programming circuits used in Atmel EPROMs. That same programming circuitry also makes an Atmel EPROM quite insensitive (compared to other EPROM suppliers) to the level of V_{PP} voltage used during programming. However, just as with other EPROM suppliers, Atmel can guarantee the same product reliability for V_{CC} = 5 V programming as with nominal V_{CC} programming only if parts are specially tested.

On-Board EPROM Programming Tips and Rules for Success

Users of programmable memory devices, such as EPROMs, sometimes take for granted how they actually are programmed. In the case of a socketed EPROM a socket must be mounted on the PC board, the EPROM is programmed with a commercially available EPROM programmer, and then the EPROM is put in the socket on the PC board. If the EPROM needs new code it must be erased in a UV eraser, reprogrammed in the EPROM programmer and then returned to the socket. All of this seems very simple and routine, but what about applications where the EPROM is soldered directly to the PC board, such as surface-mount assembly and high-reliability applications? To make matters even more complicated, what if the V_{CC} line on the PC board can't be elevated to 6.5 volts during programming, but must be kept at 5 volts to keep from damaging other circuits on the PC board? Fundamentally, this is one of the most difficult problems in EPROM applications: programming EPROMs with only a 5-volt supply **in situ** on the board. For this reason, Atmel offers easy-to-program Flash PEROMs. For users that insist on sticking with EPROMs, and expect to reprogram in the system, this article provides you with some important guidelines.

Although a commercially available board-level programmer can be used, such as the Data I/O Boardsite, the distance between the device and the programmer's pin drivers (which is on the system PC board) can cause some uncertainty. If the EPROMs are poorly programmed, then low programming yield, low noise immunity and lower long-term data retention problems may result.

Why should on-board programming with 5 volts be so difficult? One would think you could just run some extra traces for V_{PP}, V_{CC} and so on, put a connector on the side of the PC board and that's it! It really isn't that simple. Most engineers who design microprocessor systems have a good understanding of what it takes to design a PC board for those systems. But when you design a PC board for on-board programming, you're essentially designing a programmer as well. And not every engineer has designed EPROM programmers. It's not an impossible task, but you have to know what you are doing.

The solution to the 5-volt, on-board programming problem is two-fold. First, one has to understand 5-volt programming. One thing to read is the application note following this one, called *New EPROMs Speed Programming*. That application note, along with the section of this note on 5-volt programming, will help one understand the difficulties with it and how you need to get parts tested. Next, one has to understand about noise-free PC board design for programmers. The second section of this application note contains several design tips to be implemented when designing a system board if there will be EPROM programming on-board. If parts are correctly tested and these PC board design tips are followed, 5-volt, on-board programming will be a success.

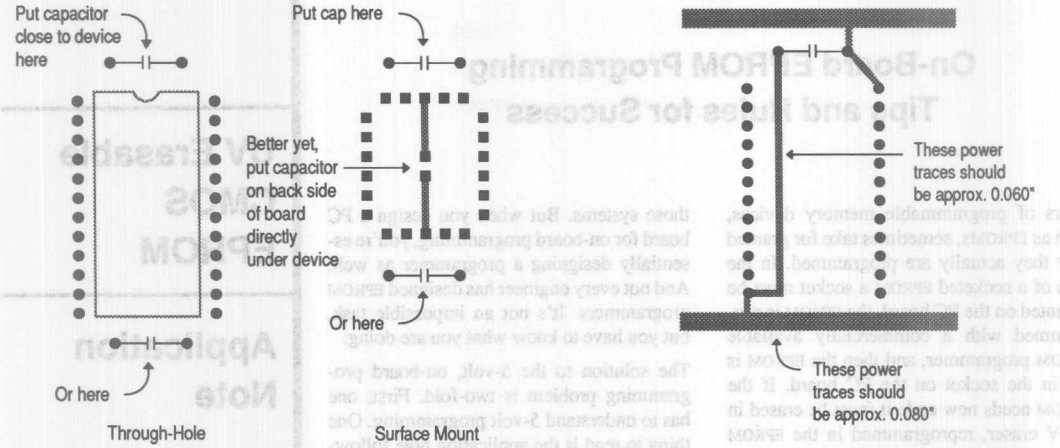
Programming EPROMs with V_{CC} = 5 Volts

There are several programming problems when someone tries to program an EPROM with V_{CC} = 5 volts. One of the most important reasons that V_{CC} is set at 6.5 volts when programming is to verify the programming margin of the device in the programmer. This way there is a guaranteed 1.5 volts of programming margin (6.5 volts - 5.0 volts = 1.5 volts). In reality, the programming margin will probably be greater, but using the value of V_{CC} used during programming is a worse-case situation when using the Atmel Rapid Programming Algorithm.

If a part is programmed at 5 volts, verification of the part after programming is also at 5 volts. If the minimum programming margin is the value of V_{CC} used during programming, then the EPROM is only guaranteed to work with V_{CC} = 5 volts. Most of the

close as possible to the device.

between the device and power supply as wide as possible.



EPROM cells in the memory core will program up so that their margins are more than 7 volts, which provides more than 2 volts of margin. But what if only a few cells, or even one cell, programs up to only 5.1 volts? This will pass the 5-volt verify during programming, but having only a 0.1-volt margin is not so good. If there is a noisy power supply, the V_{CC} noise spikes would cause the EPROM to give erroneous data, since the bad cell begins to change state at about 5.1 volts. Additionally, having only a 0.1-volt margin doesn't give much overhead for long-term data retention. The worst of these failures are marginally programmed parts that give sporadic failures while programming or in the field.

The solution to this problem is relatively simple: let Atmel know when you have a 5-volt programming requirement and the company will screen your parts for programmability at V_{CC} = 5 volts. What the screen does is to program your parts at 5 volts, then verify at 6.5 volts. This special test is performed with no programming repair sections in the algorithm. The cells must program up to 6.5 volts with only the initial programming pulse. With this test, when these components are programmed **in situ** with a 5-volt programming pulse, there will be a 1.5-volt programming margin guaranteed!

Board Design Layout Hints

Many people find that their **in situ** programming problems are caused not by their programming setup but by their PC board design. Most boards do look pretty good, but the layout was done while considering only reading the EPROM, not programming it. If the printed circuit board in an on-board programming setup is not designed correctly, all sorts of programming problems will crop up.

Following is a list of easy-to-follow design rules. The rules listed here are not all that elementary, although they may seem so. They come from the mistakes of many bad designs. Somebody else already made these mistakes, so you don't need to!

Design Rule 1: Install a bypass capacitor **right next to the EPROM**, and at every other multi-output device on your board (see Figure 1). If multilayer boards with power planes are used, mount the capacitor right next to the V_{CC} pin. CMOS components, although they may save you fair amounts of power, are notorious noise generators. When the outputs switch on these devices, so much current is dumped into the output that ground bounce can occur between the chip and the leadframe. (This is due to the inductance in the bonding wire. That's why Atmel uses two to three ground bond wires.) The combination of traces, lead frames, and bondwires can yield some pretty high inductances. High inductances and steep slew rates can lead to some severe switching noise spikes on the V_{CC} line.

The only way to prevent these switching noise spikes on the V_{CC} line is to supply current to the device when it needs it most, when it is switching. This can be accomplished by adding a 0.1-µF bypass capacitor between V_{CC} and ground. Use a stacked or monolithic ceramic capacitor rated at 50 volts with either X7R or Z5U dielectric. If the boards are surface-mount, use chip caps mounted directly next to the V_{CC} pin of the device. Ceramic capacitors are used because of their low ESL and low high-frequency impedance (inductance), and for the stability of the dielectric over temperature and time. Do not use tantalum capacitors, as their high impedances at high frequencies (from high ESLs and ESRs) prevent them from delivering charge to the device fast enough. Also, don't use 0.01-µF ceramics for

Figure 3. (Design Rule 3) Make the data bus traces as wide as possible.

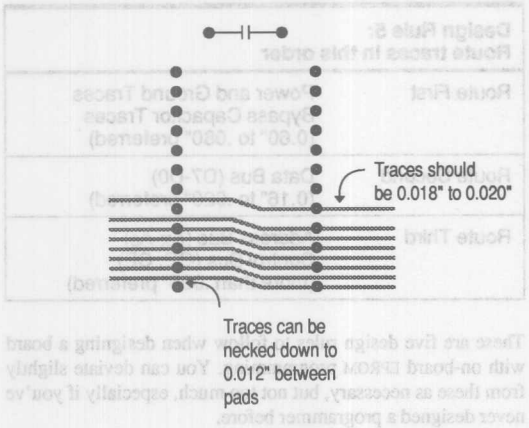
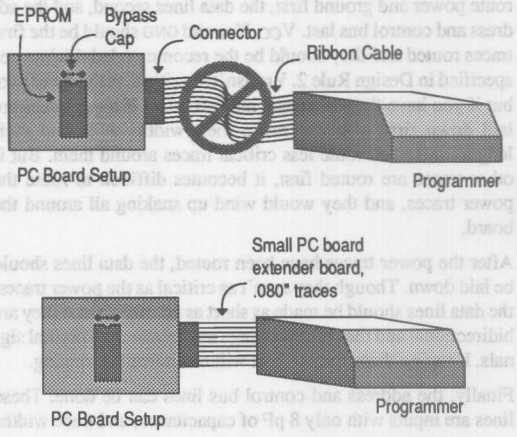


Figure 4. (Design Rule 4) Absolutely don't use ribbon cable!



bypassing. These capacitors have only one-tenth the charge capacity of a 0.1–µF capacitor, and that's not enough.

Position a 10-µF tantalum capacitor where the power supply cable mounts to the board and another one near the EPROM somewhere. You won't need to position a 0.1-µF bypass capacitor next to the 10-µF bulk capacitor, since there already is one at every device.

Design Rule 2: Keep the power supply traces big (and short). Trace widths should be no less than 0.025 inches, while trace lengths should be kept shorter than 0.375 inches. Obviously, when working with dual-in-line packaged components, these line lengths will be too short. In this case, trade off line length for trace width; if the traces have to be longer, make them a little wider. Finally, when you have the board made, specify 1.5- to 2.0-ounce copper clad. This will give you sufficient trace height.

The distance from the power supply to the EPROM should be less than six inches. If the power supply is remote (off board), then the total distance of power trace length and cable length should be less than six inches. Even if power and ground are on planes, the mean distance should be less than six inches. If power and ground must pass through a cable, the power leads should be at least 18-gauge wire (or maybe a 16- or 14-gauge wire depending on cable length), and there should be two leads for each, power and ground. The power and ground traces should be at least 0.060 inches wide, 0.080 inches is even better (see Figure 2). Major feed-throughs should use at least two vias, four would be even better, and they should be filled with solder.

Remember, this beef-up operation is only necessary between the power supply and the EPROM, and between the programming device and the EPROM.

Design Rule 3: Data lines (D7–D0) should be as wide as possible to reduce impedances. The data lines are used to write to the EPROM as well as read from it, forcing them to be bidirectional. When the EPROM outputs are switched on, large instantaneous currents get switched around. With inductive loading, these currents can cause the data lines to ring and generate large switching spikes. Although these spikes and the ringing will have dampened when the data is sampled, they could damage other parts that are sharing the same data bus.

Data line traces should be at least 0.012 inches wide, with 0.018 to 0.020 inches preferred. These traces should be routed so that their length is minimal (see Figure 3).

Design Rule 4: Use no ribbon cables! If you are adapting from a board-level programmer to your PC board (which is where the EPROM is located), use a printed circuit extender with short, wide traces and a good connector at either end, similar to a computer extender card (see Figure 4). Use a minimum of 0.060-inch trace widths with power and ground pushing 0.080 inches, on 2-ounce copper clad minimum. If you must use a cable, build your own with 18- (or 16- or 14-) gauge wire (double-up power and ground) and don't bundle it together with tie-wraps. Whatever you do, don't use ribbon cable. Ribbon cable was designed to carry low-frequency, low-power signals. The instantaneous currents present during programming will cause problems due to the cable's inductance. Additionally, the connectors on either end of the cable are only crimped on, and these

connections can sometimes be quite questionable. You'll experience nothing but problems if you use it.

Design Rule 5: When designing (laying out) the PC board, route power and ground first, the data lines second, and the address and control bus last. V_{CC}, V_{PP} and GND should be the first traces routed and they should be the recommended thicknesses specified in Design Rule 2. V_{PP} isn't as critical as the other two, but if you have the real estate, make it wide. If these traces are laid down first, you can make their widths wide and their lengths short and route less critical traces around them. But if other traces are routed first, it becomes difficult to route the power traces, and they would wind up snaking all around the board.

After the power traces have been routed, the data lines should be laid down. Though they aren't as critical as the power traces, the data lines should be made as short as possible, since they are bidirectional and the current swings are greater than normal signals. Keeping these traces short will minimize bus ringing.

Finally, the address and control bus lines can be done. These lines are inputs with only 8 pF of capacitance, and trace widths and lengths aren't critical. You can snake these traces around the power traces and the data line traces, and use as many vias as necessary.

Design Rule 5: Route traces in this order	
Route First	Power and Ground Traces Bypass Capacitor Traces (0.60" to .080" preferred)
Route Second	Data Bus (D7-D0) (0.16" to .020" preferred)
Route Third	Address Bus (A_X-A_0) Control Bus ($\overline{OE}$, $\overline{CE}$) (more than .005" preferred)

These are five design rules to follow when designing a board with on-board EPROM programming. You can deviate slightly from these as necessary, but not too much, especially if you've never designed a programmer before.

New EPROMs Speed Programming

Introduction

In designing and manufacturing certain modern-day products, the methods used to build these products are often as important to the design engineer as the components themselves. This is true about programmable memory devices as well, especially EPROMs. Since many vendors use their own unique programming algorithm, which is based on the process used to make EPROMs, the design engineer needs to know about the algorithm during the system cycle to insure that the EPROMs can ultimately be programmed.

This application note will introduce the Atmel RAPID programming algorithm and briefly explain why this algorithm is superior to others. In addition, it will give an introduction to EPROM technology and the mechanics of programming. These should provide a basic understanding in the growing field of EPROMs.

Programming EPROMs the RAPID Way

When Atmel reduced the geometry of some of its EPROM products recently from 1.5- to 1.2-µ linewidth, the Company adopted an entirely new programming algorithm for these devices. A reason for this algorithm change was to improve programming yields and lengthen long-term data retention. This was accomplished by using a shorter programming-pulse length during programming. The new RAPID algorithm reduces the 1-ms programming pulse width of the original FAST algorithm to only 100 µs, and it completely eliminates extra overprogramming pulses.

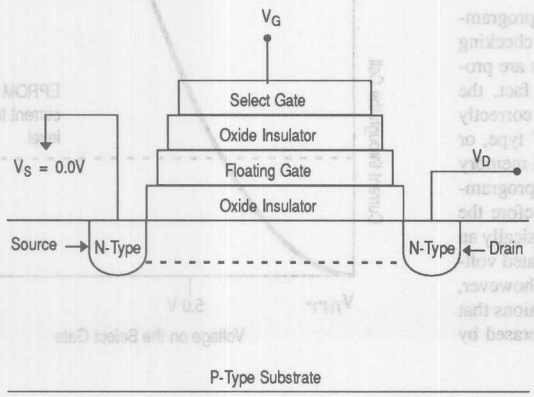
But higher yields and increased reliability aren't the only benefits the RAPID algorithm provides, it also takes less time to program these new devices. The RAPID algorithm can reduce the programming overhead costs by a factor of 40! Here's how it works:

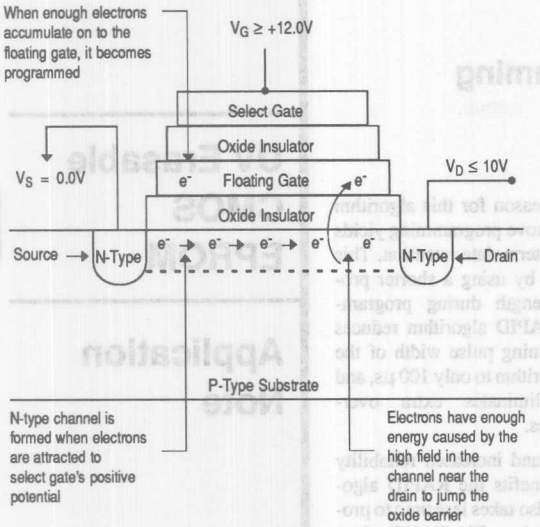
If you program an AT27C512R, 512-K EPROM in a single-device programmer, using the FAST or any other type of 1-ms algorithm (1-ms initial pulse, plus 3-ms overprogramming pulse) the time spent programming will be:

524288 bits ÷ 8 bits/byte = 65536 bytes

65536 bytes x .004 seconds/byte = 262 seconds

Figure 1. Cross section of a typical EPROM cell.





That's 262 seconds, or 4 minutes and 23 seconds. This works out to about a 75 cents programming cost, assuming an operator's rate of $10 per hour. Here's where the cost savings start: since we cannot reduce the number of bits to program, we reduce the total programming time by shortening the programming pulse width. Using 100 µs per byte, this is what happens:

65536 bytes x .0001 seconds/byte = 6.5 seconds

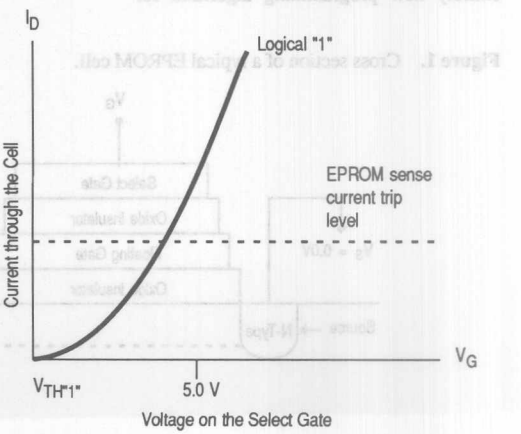
This amount of programming-time savings is what can be expected when using the RAPID algorithm. The big improvement is from reducing the total byte-programming time from 4 ms to 100 µs. With this example, total programming cost is about three cents. The RAPID algorithm can actually save up to 72 cents per device. Imagine how much can be saved with 10,000 EPROMs!

There's more to the RAPID algorithm than shorter programming times and cost savings. It has a special way of checking that each cell is correctly programmed, and that cells are programmed with the required amount of charge. In fact, the RAPID algorithm even guarantees that the EPROM is correctly programmed. Programming algorithms of the FAST type, or their relatives, the QUICK-PULSE types, check each memory location for the programmed data immediately after programming that location. This check, which takes place before the final verify at the end of the programming cycle, is basically an "insurance" check, because it is performed at an elevated voltage, which is a worst-case condition. There is a flaw, however, in this type of programming algorithm: memory locations that have been previously programmed can be partially erased by programming subsequent locations (due to the elevated voltage on the same row or column in the memory array) and marginally programmed cells will go virtually undetected. The question is, doesn't the programmer check each device during verify after programming? Wouldn't those failures be caught then? Not necessarily, because when parts are checked during the program verify mode, the voltage is not elevated as high as it was during programming.

The RAPID programming algorithm was designed to fix this oversight. First, it goes through the entire device and programs every cell without checking. Then it goes back to the beginning of the memory array and verifies the data in each cell at the elevated voltage. Once the device passes, another final verification is done at 5 V. The RAPID algorithm will do a better job at preventing any marginally programmed parts from passing the programmer than other algorithms.

An important fringe benefit of the RAPID algorithm, because of the way it guarantees successful programmability, is long-term data retention. Basically, long-term data retention is how long the EPROM stays programmed, which is typically greater than ten years. Although long-term data retention is not the same as device programmability, they are related in this way: programmability tells how well the electrons have accumulated on the EPROM's floating gate, long-term data retention tells how long the electrons will stay there. The programming algorithm has an overwhelming influence on programmability, making it an overwhelming influence on long-term data retention as well. Therefore, a poor programming algorithm, one that doesn't guarantee programmability, can be responsible for poor long-term data retention. The RAPID algorithm can add years of data retention to your parts, because of the way it checks for programmability. Marginally programmed parts just don't stand a chance of getting past the programmer.

Figure 3. Unprogrammed cell.



EPROM Programming, How it Works

Contemporary EPROM programming algorithms can be divided into two main sections, programming and verifying (or reading). Programming begins by selecting the desired voltage levels and byte address. It continues with a programming pulse applied to that byte, followed by a verify at the elevated V_{CC} used for programming. Verifying checks the data in two passes with the original data, with V_{CC} set to 5.5 V on the first pass, and 4.5 V on the second.

Basically, EPROMs are programmed through the accumulation of electrons on the floating gate of an N-Channel EPROM cell (see Figure 1) by the process of hot-electron injection. Hot-electron injection is where electrons, flowing as a current between the drain and source of a saturated EPROM cell, gain enough energy from the high electric field to jump the oxide barrier between the channel and the floating gate (see Figure 2). Before programming, the MOS threshold voltage, V_{TH} (otherwise known as the gate threshold voltage) of the erased floating-gate EPROM cell is about 1.0 to 2.0 V (see Figure 3). After programming, its threshold voltage is about 6.5 to 9.0 V, due to the accumulated electrons on the floating gate. In read mode, the address decoding circuitry in the chip selects the desired cell by pulling the gate voltage of the cell to V_{CC}. Since V_{CC} is typically 4.5 to 5.5 V, an erased cell with a V_{TH} = 1.5 V would be turned on (Figure 3), while a programmed cell with a V_{TH} = 7.5 V would remain off (see Figure 4). This floating-gate process is how a single MOSFET-like transistor can provide for the two logic levels used in digital circuitry.

If V_{CC} is gradually raised in voltage to a point near the threshold voltage of a programmed EPROM cell, the cell would just begin to conduct, and would no longer appear to be programmed. This point, where the programmed EPROM cell begins to look unprogrammed, is defined as the programming margin (see Figure 5). The value of the programming margin

Figure 4. Programmed cell. Note how V_{TH} raises after electrons are accumulated on the EPROM floating gate from programming.

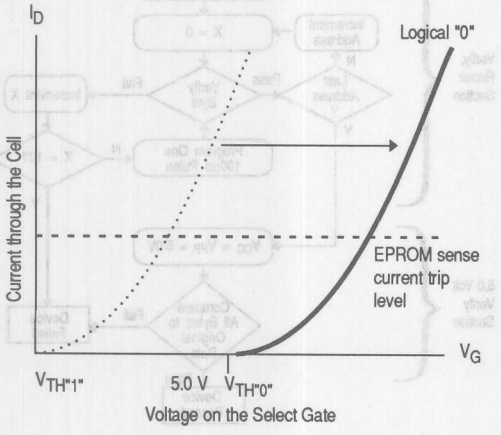
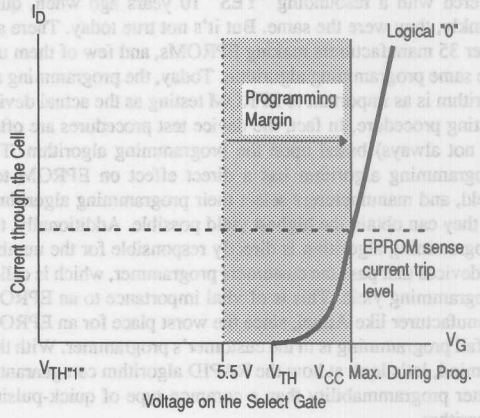


Figure 5. Programming margin. To find programming margin, increase gate voltage (V_{CC}) until the first "0" turns into a "1."



can, in some cases, be simply equal to the value of the V_{CC} voltage present during programming. This is why the RAPID algorithm holds the value of V_{CC} constant at 6.5 V during programming; to insure that each EPROM cell has a programming margin of at least that voltage. This margin is verified by reading each byte twice, once during the initial programming operation and again during the final read (or verify) operation, where the data from the EPROM is compared to the desired data. The difference between the value of V_{CC} during programming (the guaranteed programming margin) and the 5.5-V V_{CC} maximum supply rating (from the data sheet) serves as a reliability guardband for long-term data retention and, more importantly, for system noise immunity. Poor programming margin can reduce system noise immunity and lead to EPROM chip instability due to power-supply noise on the V_{CC} pin. This instability can cause oscillations and read-mode data glitching that can be a problem in even in the slowest and most noiseless of systems. Since power-supply noise is a somewhat random occurrence, data errors can happen non-reproducibly, which can undermine the reliability and integrity of the host system. These problems can be avoided by using the programming algorithm recommended by the EPROM chip vendor. The higher the guaranteed programming margin, the less likely any problems will occur.

Another important benefit of high-programming margin is that it extends the long-term data retention of the device. If the 6.0-V programming margin (FAST algorithm) on the EPROM gradually diminishes to 5.5 V over a 10-year time span, the randomly occurring noise spikes on the V_{CC} line can cause the EPROM to yield faulty data. On the other hand, given the same discharge rate (as a function of the silicon processing), an EPROM with a programming margin of 6.5 V (RAPID algorithm) would take over 20 years to reach the 5.5-V threshold that would lead to faulty data yield. All things being equal, better programming margin leads to longer data retention.

Guaranteeing Programmability

Most people might ask, "What's in a programming algorithm? Aren't they all the same?" That question would have been answered with a resounding "YES" 10 years ago when, quite frankly, they were the same. But it's not true today. There are over 35 manufacturers making EPROMs, and few of them use the same programming algorithm. Today, the programming algorithm is as important to EPROM testing as the actual device testing procedure. In fact, the device test procedures are often (if not always) based upon the programming algorithm. The programming algorithm has a direct effect on EPROM test yield, and manufacturers select their programming algorithms so they can obtain the highest yield possible. Additionally, the programming algorithm is directly responsible for the number of devices that pass the customers programmer, which is called programming yield. This is of vital importance to an EPROM manufacturer like Atmel, since the worst place for an EPROM to fail programming is in the customer's programmer. With this in mind, let's look at how the RAPID algorithm can guarantee better programmability than a common type of quick-pulsing algorithm.

We'll begin by comparing a common type of quick-pulsing algorithm with the Atmel RAPID algorithm. Examine Figure 6, which is the flowchart for the QUICK-PULSE type of algorithm. If you look very closely you will see that the algorithm is broken up in to two major sections. The main part is the program/verify section, the other part is the final verify section. Basically, the first section starts at byte address 0000H, programs the eight EPROM cells at that address, and verifies that those cells contain the correct data with a verify at 6.25 V on V_{CC}. If the byte passes, it goes on to the next byte. If it fails, it repeats everything up to 25 times before it fails the device. The second section lowers the V_{CC} voltage to 5.0 V and checks if all address locations read with the correct data. Although the flowchart specifies a one-pass final verify at 5.0 V, many programmers verify in two passes, one with V_{CC} at 4.75 V and the other with V_{CC} at 5.25 V.

Now examine Figure 7, the Atmel RAPID algorithm. It looks similar to the quick-pulsing type of algorithm, but with a slight difference. If you look closely you'll see that it consists of three sections instead of just two. The first section is the programming section, where the programmer programs every location

Figure 6: QUICK-PULSE type.

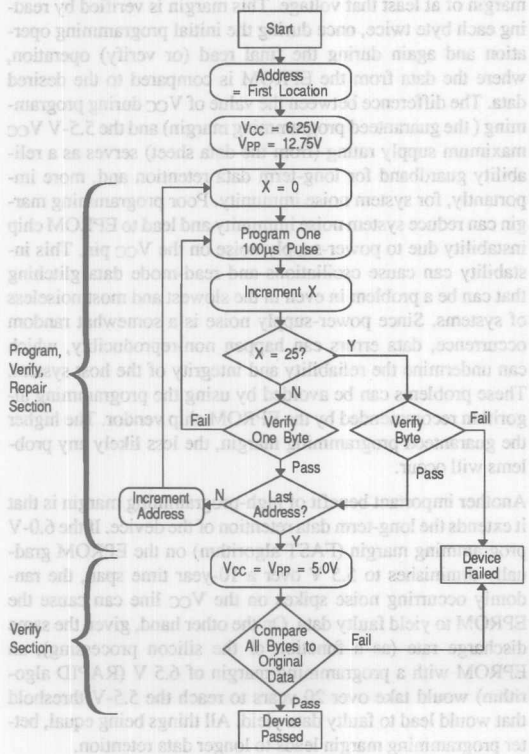


Figure 7: RAPID programming algorithm.

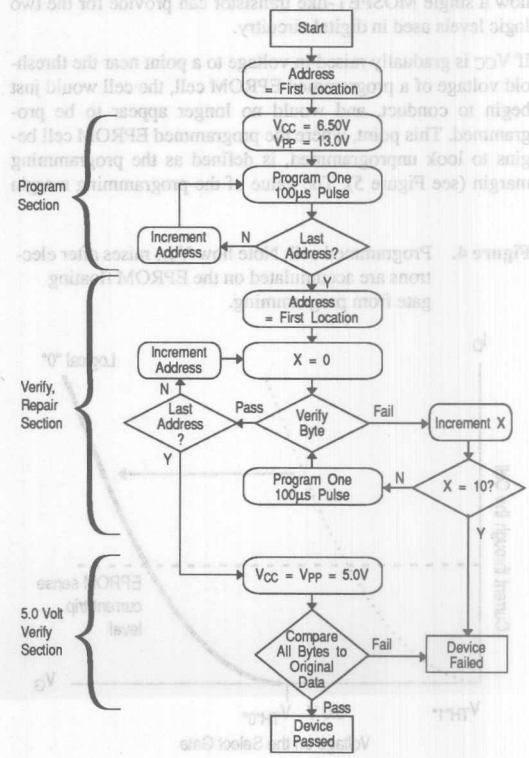


Figure 8: Row of EPROM cells from AT27C010. Note that the programming margin of each cell is 0, which allows each bit to read a "1".

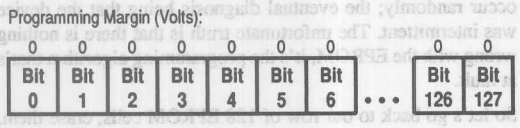


Figure 9: Bit 0 has been programmed, (QUICK-PULSE algorithm)

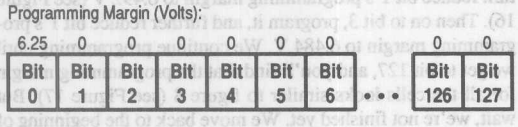
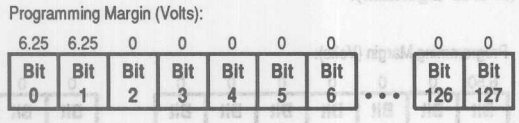


Figure 10: Bit 0 and bit 1 have been programmed.



in the EPROM without verifying. Next there is the verify/repair section, where the programmer starts at the beginning of the EPROM and verifies every location for the correct data at 6.5 V. Any cells that don't pass are reprogrammed up to ten times before the device is failed. The last section lowers V_{CC} to 5.0 V and does a final verify of the data (here again, most programmers verify in two passes, one with V_{CC} at 4.75 V and the other with V_{CC} at 5.25 V). This type of programming algorithm is called a two-pass algorithm, because it goes through the memory array twice during programming.

Well, this all sounds fine, but what difference can the programming algorithm possibly make? We can find the answer to that question in a particularly sneaky deprogramming mode that EPROMs can exhibit. We all know that EPROMs are erased by exposing them to short-wave ultraviolet light, right? Nothing more than applying Einstein's discovery of the photoelectric effect. But there is another erasure mode that can occur, one that people in the E^2PROM business know about. If you were to examine some EPROM cells in an electron microscope, you might find a few that have small, tooth-like projections (called asperities) on the top of the floating gate polysilicon. These projections won't affect the normal operation of the EPROM, but they could give you problems during programming. When you program a row of cells on an EPROM, cells that have been previously programmed still feel the full brunt of the high V_{PP} voltage on their gates when subsequent cells on the same row are programmed, because all of the cells on a row have their gates connected together. The combination of high voltage on the gate and ground on the drain and source causes an intense electric field in each previously programmed cell. If any one of the cells on that row have these tooth-like projections on their floating gate polysilicon, the resulting electric field in the oxide above the projections will be much more intense than normal. This intensified electric field can give some of the electrons on the floating gate enough energy to jump the oxide barrier, thereby partially erasing the EPROM cell. This unwanted effect, called programming erase, can be responsible for poor programming margins unless the programming algorithm takes this problem into account.

Before we continue, it's important to realize that this type of cell doesn't have a **reliability** problem, it has a **programmability** problem. This cell will have the same long-term data retention as any other cell in the device, even if it loses part of its programming charge. Although it is an EPROM, it has the same charge retention characteristics as many manufacturers' E^2PROM cells that use this type of erasure mode, and they all exhibit excellent long-term data retention. The challenge is to find these low-margin cells in the device with our programming algorithm, and to repair them so that the device functions normally.

Let's see what kind of impact a cell like this can have on programming margin by programming a row of EPROM cells from our AT27C010 one-megabit EPROM with both algorithms. The array geometry on the one-megabit is 128 columns by 1024 rows, by 8 outputs. This means that a single row from a single output has 128 EPROM cells. Let's say that the second cell on this row, bit 1 (we'll call them bits and start with bit 0), has an asperity, just like the one mentioned above. When we go to program bits 2, 3, 4, etc., the voltage present on the gate of bit 1 causes the E^2PROM-like erasure mode. Given enough subsequent bits to program, bit 1 may lose enough charge to appear unprogrammed. Let's take a look at how the QUICK-PULSE type of algorithm will fail the device, or even worse, pass it with poor programming margin. Then we'll see how the RAPID algorithm will program it such that it works perfectly!

If we examine Figure 8, we see the row of EPROM cells taken from our AT27C010 one-megabit device. Recall that bit 1 is the cell that's having the programmability problem, while the rest of the bits function normally. For the sake of example, let's say that for each subsequent bit after bit 1 that's programmed, bit 1 will lose eight millivolts (mV) of programming margin. Let's also assume that the nominal programming margin for each cell is at least the value of V_{CC} present during programming, which is 6.25 V for QUICK-PULSE type algorithms and 6.5 V for the RAPID algorithm. Starting with the QUICK-PULSE type of algorithm at bit 0, we program it, verify it, and find that it passes (remember our flowchart from Figure 6?) with the correct margin (see Figure 9). We move to cell 1, program it, verify it, and

has been slightly erased.

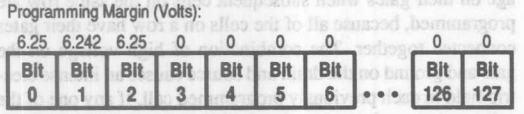


Figure 12: Bit 3 has just been programmed. Notice that bit 1 has been further erased.

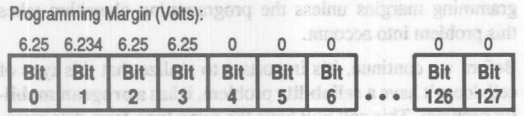
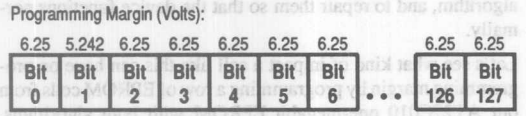


Figure 13: The entire row has been programmed. Notice how much bit 1 has been erased.



it passes (see Figure 10). Remember, bit 1 only loses voltage margin when subsequent cells are programmed. Now we move on to bit 2, program it, verify it, and in the process reduce bit 1's programming margin down to 6.242 V (see Figure 11). Next we go to bit 3, program it, verify it, and in turn reduce bit 1's programming margin down to 6.234 V (see Figure 12). This process continues until we get to bit 127. By this time bit 1 has experienced 126 subsequent cell programming cycles, and its programming margin will be reduced to 5.242 V (see Figure 13). Since the QUICK-PULSE type of algorithm does its high-voltage verify immediately after programming, the algorithm has no way of knowing what has happened to bit 1, once it finishes programming it. Only when the algorithm does its final verify with V_{CC} set at 5.25 V could it detect that bit 1 is not fully programmed.

In this example we were able to detect bit 1 as being bad, and we would fail the device. But what if bit 1's erasure rate was slightly less than 8 mV per subsequent cell, say 7.7 mV? Bit 1's margin might be somewhere around 5.3 V, which would probably pass the 5.25-V verify check on our programmer. But remember the problem that we discussed earlier, about the power supply noise glitches messing up the operation of devices with low programming margin? A device with only 5.3 V of margin

glitch occurring during data access on the V_{CC} line of this EPROM could easily change the output from a "0" to a "1". And, to make matters worse, this problem would probably occur randomly; the eventual diagnosis being that the device was intermittent. The unfortunate truth is that there is nothing wrong with the EPROM, it's the programming algorithm that's at fault.

So let's go back to our row of 128 EPROM cells, erase them, and reprogram them with the RAPID algorithm. Remember that with the RAPID algorithm the initial program and verify routines are located in different sections of the algorithm, they are not contained within the same loop. Starting at bit 0, we program it (to 6.5 V this time, see Figure 14). Then move to bit 1, and program it (see Figure 15). Next to bit 2, program it, and in turn reduce bit 1's programming margin to 6.492 V (see Figure 16). Then on to bit 3, program it, and further reduce bit 1's programming margin to 6.484 V. We continue programming until we get to bit 127, and you'll find that the programming margin for all the cells looks similar to figure 8 (see Figure 17). But wait, we're not finished yet. We move back to the beginning of the EPROM array, which is bit 0, and verify that it has 6.5 V of

Figure 14: Bit 0 has just been reprogrammed (RAPID algorithm).

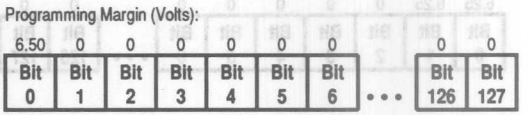


Figure 15: Bit 1 has just been programmed.

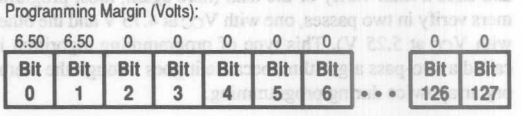


Figure 16: Bit 2 has just been programmed. Notice how bit 1 has been slightly erased again.



programming margin. Since we are verifying at 6.5 V, we pass it. We now move to bit 1 and notice that its programming margin is 5.492 V. This fails our 6.5-V verify, so we program it one more time and raise its margin back to 6.5 V, then pass it (see Figure 18). Then we move to bit 2, and pass it, since its programming margin is also 6.5 V. Notice that we didn't deprogram bit 1 in the process of verifying bit 2. We only deprogram bit 1 when we program subsequent cells; reading or verifying (which is reading) doesn't generate the intense electric fields needed to deprogram EPROM cells. After verifying (and repairing) this row of cells, we return V_{CC} to 5.25 V, do a final data verify, then pass the row (see Figure 18). Now compare Figure 18 with Figure 13. That's how the RAPID algorithm can guarantee programmability!

Well, you may ask, what if we had five problem cells on the same row? Wouldn't the additional programming pulses during the verify function deprogram previously programmed and verified cells? They probably would, but the maximum amount of deprogramming on the first bit (using this model) would be only 32 mV (4 x 8 mV). This gives us a programming margin of 6.468 V, which is still an excellent programming margin.

When you compare the QUICK-PULSE type algorithms to the RAPID algorithm, there really is no comparison. The RAPID algorithm simply guarantees programmability, and we demonstrated this with the deprogramming bit example, which is one of the trickiest programming problems you can have. But the RAPID algorithm caught the problem, and repaired the bit so that the EPROM will function normally. That's why Atmel has changed its EPROMs programming algorithms over to the RAPID algorithm, and why all new devices will use this algorithm. You'll be glad we did!

Figure 17: The entire row has just been programmed. Notice how much bit 1 has been erased.

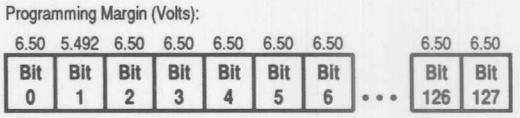
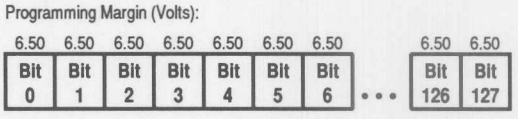


Figure 18: The entire row has just been verified at 6.50 volts. Notice how bit 1 has been repaired, its margin being returned to 6.50 volts using the RAPID algorithm.




Byte
0
Bit
7
Bit
6
Bit
5
Bit
4
Bit
3
Bit
2
Bit
1
Bit
0
6.50
6.50
6.50
6.50
6.50
6.50
6.50
5.492
6.50
Bit
127
Bit
126
6.50
6.50

Byte
0
Bit
7
Bit
6
Bit
5
Bit
4
Bit
3
Bit
2
Bit
1
Bit
0
6.50
6.50
6.50
6.50
6.50
6.50
6.50
6.50
6.50
Bit
127
Bit
126
6.50
6.50

Programming Socket Adapter

As the market for nonvolatile memory parts in surface mount packages increases, so does the interest in simple, low cost programming socket adapters. These adapters allow users of standard programming equipment to program any package type including LCC (leadless), SOIC (gull-wing), PLCC (J-Lead), and flatpack. The adapter plugs into the programmer in place of a 600-mil or 300-mil DIP package of the same part. The surface mount part to be programmed then plugs into the socket on the adapter.

The two major disadvantages of building a socket adapter are:

- Little or no support from programmer manufacturers.
- Prolonged use of socket adapters using wire-wrap pins is not recommended due to spring tension loss damage of the programmer's zero insertion force sockets. That may degrade the reliability of the programmer when the adapter is not used.

The advantages are more obvious. Some manufacturers charge up to $500 for an adapter which slides or plugs into the programmer compared to about $100 for the hardware described here.

Assembly of a custom programming adapter is very simple. Table 1 describes the typical piece-parts needed. Table 2 lists sockets and piece-part sources for different package configurations. The finished adapter is about 2 inches square and 1.5 inches high.

As listed in Table 2, Emulation Technology, Inc., (408) 982-0660, can supply the adapter sockets preassembled, but we recommend you order the parts as an UNSOLDERED KIT to facilitate attaching the decoupling capacitors. The additional wire shunts (not re-

Table 1. Piece-Part Descriptions (see Figure 1)

Item No.	Qty.	Description
(1)	1	Zero insertion force socket.
(2)	2	Wire wrap strips with 100 mils pin centers and about 500 mils long on the end which will plug into the programmer's socket and 200 mils long on the opposite end to attach to (5) below.
(3)	2	Wire wrap strips similar to (2) above except only 100 mils and 200 mils long to connect (4) and (5) below.
(4)	1	PC board to accept the socket (1) and run traces to the edge of the card connecting to (3).
(5)	1	PC board to run traces from the card edge (3) to the two strips (2) (usually separated by 600 mils).
(6)	20"	#16-18 insulated stranded copper wire.
(7)	1-2	0.1-µF ceramic high-frequency decoupling capacitors.
(8)	1	(Recommended) Pin socket board to fit between (1) and (4) to allow easy replacement of the socket (1). (8) is soldered to (4) and (1) plugs into (8). Zero insertion force sockets wear out quickly so replaceability is a good feature to have.

quired if a -LN kit is ordered from ET) and capacitors are essential to reduce inductive noise effects during programming and to maintain adequate programming yield. It is necessary to "beef-up" all the power (V_{CC}, V_{PP}) and ground (Gnd) connections by adding short jumpers of wire (6) running from the socket (1), around the edge of the module and finally to the pins of item (2) on the bottom of the module. Bypass capacitors (7) must be soldered between Gnd and V_{CC} or V_{PP} (if applicable). The leads on the capacitors must be trimmed as short as possible and soldered as close to the socket (1) as possible (on the wide traces on the -LN board (4)). The other end of each capacitor will be connected to short stranded wires (6) running from the top, around the edge of the adapter, and finally soldered to the ground pin of item (2).

Assembly proceeds as follows (see Figure 1 and note that jumper wires (6) are not required if a -LN kit is used):

1) Trim the leads on the jumper wires (6) to about 3.0 inches. Solder capacitors (7) with shrink-wrap insulation on the cap leads, and jumper wires (6) under the socket (1) (or under (8) if socket replaceability is needed) in such a way that they do not interfere with attaching the socket (or (8)) to the board (4). (If a -LN kit is used, just solder the capacitors on the wide traces provided on board (4).)
2) Solder the socket (or item (8)) to the PC board (4) and trim the pins on the socket flush to the board (4).
3) Solder the shorter pin strips (3) to the outside of board (4) with the spacers on the side away from the socket (1).
4) Solder the longer pin strips (2) into the other PC board (5) such that the spacers stick out of the bottom of the adapter. These longer pins will be used to plug directly into the programmer socket. Trim the shorter leads of (2) flush with the board (5) after soldering.
5) Solder the PC board (5) to the short pins protruding below PC board (4).
6) (Omit this step if a -LN kit is used.) Connect all the V_{CC}, V_{PP} (if applicable) and Gnd wires which were connected in step (1) to their appropriate pins on item (2) on the underside of the assembly close to the protruding spacer in such a way that they will not interfere with plugging the completed module into the programmer DIP socket. Trim these shunt wires as short as possible to minimize inductance effects.

This application note has described how to build a simple and cheap programming adapter socket to support a wide variety of nonvolatile memory product packages available from Atmel.

Figure 1.

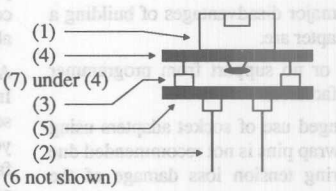


Table 2. Vendors / Part Numbers by Package Type

Package Type	Pin Count	Emulation Technology[1]	Socket Manufacturer	Part No.
LCC	28	AS-28-28-01-L6-LN	Textool[2,3]	228-4960
	32	AS-32-28-01-P6-LN	Yamaichi	IC51-0324-453
	32 (27C010)	AG-32-32-01-L6-LOW	Textool	232-5427
	44	AS-44-40-08-L6-LN	Textool	244-5292
	32 (27C010)	AG-32-32-01-P6-LOW	Textool	232-6917
PLCC	32	AS-32-28-01P-P6-LN	Yamaichi	IC51-0324-453
	44	AS-44-40-08-P6-LN	Textool	244-5292
JLCC	32	AS-32-28-01-K6-YAM	Yamaichi	IC5I-453-K510011
	32 (27C010)	AS-32-32-01-K6-YAM	Yamaichi	IC5I-453-K510011
	44	AS-44-40-08-P6-LN	Textool	244-5292
SOIC	28	AS-28-28-015-6-GANG	Enplas	FB-28-1-27-07
	28	Call Atmel	Yamaichi	IC51-937-K510369

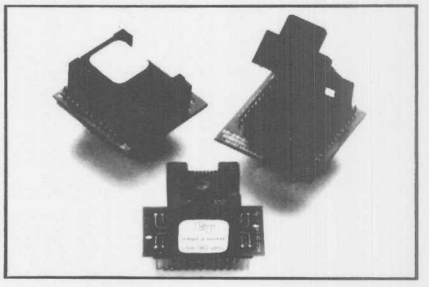
Notes: 1. ET can also supply finished adapter sockets built per this application note or other customer requirements.
2. Made by 3M. Check with your local distributor.
3. Windowed LCC packages (i.e., EPROMs) require removal of the circular bumper in the Textool socket lid which snaps apart. Non-windowed packages (i.e., E^2PROMs, OTPs) do not require any socket adjustment.

Figure 2.

LCC / PLCC / SOIC to DIP Adapter

ADAPT-A-SOCKET®
LCC / PLCC / SOIC to DIP

Prices from $67.00 to $148.00



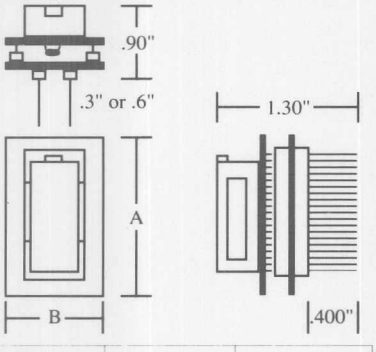
- For programming PROMS, PLDS, EPROMS, EEPROMS, PALS†
- Production ATE testing
- Test points provided for each signal
- Decoupling capacitors can be added.
- Available for LCC, PLCC and SOIC.
- Natural for prototype processing.
- Sturdy base contact pins.
- Saves development $$$.

† PAL is a registered trademark of Monolithic Memories, Inc.

When Your Equipment is Designed for DIPs

ADAPT-A-SOCKET converts your Dual-In-Line (DIP) sockets to ceramic Leadless Chip Carrier (LCC), Plastic Leaded Chip Carrier (PLCC) and Small Outline Integrated Circuits (SOIC) sockets in just seconds. Without having to purchase expensive equipment. Just plug ADAPT-A-SOCKET into your programmer socket, burn-in board or test head and you're ready to go.

Call Factory for *Cross Reference Guide*



Number of Top Pins	A	B
16	1.60 Max	1.45
20	"	"
24	"	"
28	"	"
32	1.65	1.60
32 AG*	1.70	.90
52	2.70	1.80

* AG-32-28-01P-6 is available for gang programmers

Specifications

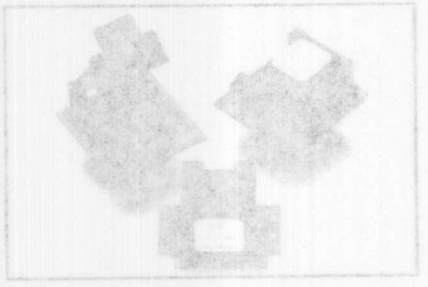
- **SOCKET** (LCC, PLCC, SOIC, FLAT PACK)
  Body Material ..... Ryton
  Contact Material ..... BeCu
  Contact Plating ..... 30 Microinches of Gold over Nickel
- **PHYSICAL**
  Lids and latches are replaceable.
- **BASE** (DIP, PGA, LCC, PLCC)
  Body Material FR4
  Contact Material ..... BeCU
  Contact Plating ..... 30 Microinches of Gold over Nickel
- **ELECTRICAL**
  Contact Resistance ..... 25 MilliOHMs per Contact MAX.
  Insulation Resistance ..... 20 MegOHMs MIN. @50 VDC
  Capacitance ..... 2.0 Pico-Farads between any pair of isolated contacts
- **TEMPERATURE RATING** ..... -55°C to +125°C

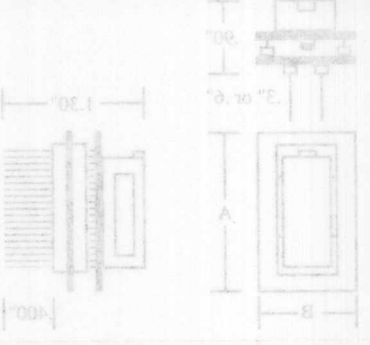
Test Point Specifications

Insulator Material ..... Glass-filled nylon black, UL94V-0
Contact Material ..... Phosphor Bronze
Current Rating ..... 1 Amp
Voltage Rating ..... 300 VRMS
Dielectric Withstanding Voltage ..... 500 VRMS
Insulation Resistance ..... >1,000 MegOHMs
Temperature Rating ..... -55°C to 125°C

® ADAPT-A-SOCKET is registered trademark of Emulation Technology, inc.

Emulation Technology, Inc. • 2368B Walsh Avenue, Bldg. D • Santa Clara, CA 95051 • (408) 982-0660
FAX: (408) 982-0664 TLX: 981 866





Number of Top Pins	A	B
16	1.60 Max	1.65
20	"	"
24	"	"
28	"	"
32	1.65	1.60
32 AD*	1.70	.90
52	2.70	1.80

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E^2PROMs 2
PEROMs (Flash) 3
EPROMs 4
PROMs 5
SRAMs 6
EPLDs 7
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1 Product Information

2 E²PROMs

3 PERROMs (Flash)

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Contents

Section 5

CMOS PROMs

AT28HC191/L	2K x 8	High Speed, 16K Reprogrammable [E^2]PROM.....	5-3
AT28HC291/L	2K x 8	High Speed, 16K Reprogrammable [E^2]PROM.....	5-11
AT27HC641R/2R	8K x 8	High Speed, 64K Reprogrammable [UV]PROM ...	5-19

16K (2K x 8) High Speed Electrically Erasable CMOS PROM

Features

- **Fast Access Time - 35 ns**
- **Low Power Dissipation**
  - **100 µA Standby Current (AT28HC191L)**
  - **80 mA Active Current**
- **E^2PROM Technology - 100% Reprogrammable**
- **Direct Replacement for Bipolar PROMs**
- **Reprogrammable 1000 times**
- **Chip Clear**
- **JEDEC Approved Byte-Wide Pinout**
  - **Industry Standard 600-mil Wide Package**
- **CMOS and TTL Compatible Inputs and Outputs**
- **High Reliability High Speed CMOS Technology**
- **Full Military, Commercial, and Industrial Temperature Ranges**

Description

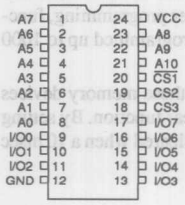
The AT28HC191/191L are a pair of high-speed, low-power 2,048 words by 8 bit CMOS PROMs. The high speed AT28HC191 offers access times to 35 ns while the AT28HC191L provides low standby current consumption of just 100 µA. Both devices are packaged in 24 pin dual inline packages using the JEDEC approved pinout for byte-wide PROMs. The AT28HC191 and AT28HC191L are packaged in the industry standard 600-mil wide package.

These devices are plug-in replacements for 16k bipolar PROMs, while offering distinct advantages in power consumption, performance and programming. Atmel's low power CMOS devices provide a direct power saving upgrade to systems originally using bipolar PROMs. The ultra-low standby power of the 28HC191L brings bipolar speeds to battery powered systems.

The electrically erasable and programmable memory cell allows for 100% testing of each memory location. The E^2PROM cell's low programming current permits devices to be programmed one byte at a time. On chip circuitry automatically erases each byte and rewrites it with the new data, permitting in socket reprogramming. The entire memory array can also be erased simultaneously, if desired, by using the device's "chip- clear" mode.

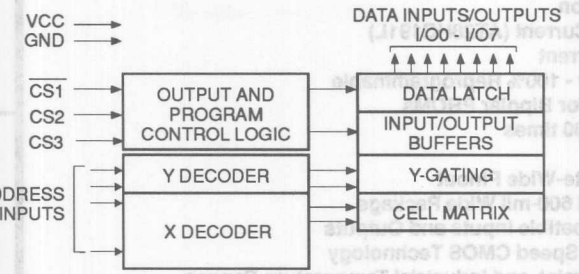
The fast access time of the devices makes them suitable for high-performance applications such as micro-control storage. In such an application the device allows for fast execution speeds, without penalizing storage density or power consumption. With a memory capacity of 2K bytes, these devices provide economical, reliable and high-performance means of storing program instructions. System reliability is enhanced by the low power and inherent reliability of Atmel's 1.5 micron floating poly technology.

Pin Configurations



Pin Name	Function
A0-A10	Addresses
$\overline{CS1}$	Chip Select (Power Down Option)
CS2	Chip Select
CS3	Chip Select
I/O0-I/O7	Data

Block Diagram



Operating Modes

Mode	CS3	CS2	$\overline{CS1}$	I/O
Read	V_{IH}	V_{IH}	V_{IL}	DOUT
Standby	X(1)	X	V_{IH}	High Z
Output Disable	V_{IL}	X	X	High Z
Output Disable	X	V_{IL}	X	High Z
Write(2)	V_{IL}	V_{IL}	V_H (3)	DIN
Verify	V_{IH}	V_{IH}	V_H	DOUT
Chip Clear	V_{IL}	V_H	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.
3. $V_H = 12.0 \pm 0.5$ V.

Device Operation

READ: When $\overline{CS1}$ is low and CS2 and CS3 are high, the data stored at the memory location determined by the address inputs is asserted on the outputs of the device. The outputs are put in a high impedance state whenever CS2 or CS3 is low or whenever $\overline{CS1}$ is high. The availability of three control lines gives the designer flexibility in preventing bus contention.

STANDBY: The AT28HC191L consumes less than 550 µW when deselected by raising $\overline{CS1}$ to V_{CC}-0.3 V. This part retains the fast chip select times from CS2 and CS3 that are common to the AT28HC191.

PROGRAMMING: A 12 volt input is required on the $\overline{CS1}$ pin in order to program the devices. This input voltage is not needed to supply the programming current required by the memory cells as all high voltages used inside the chip are self-generated. After $\overline{CS1}$ is raised to 12 volts with CS2 low and CS3 high, CS3 is pulsed low to begin the internally timed write cycle. The address location presented to the device on the falling edge of the CS3 signal is written with the data that is presented to the device on the rising edge of CS3. An entire eight bit byte is programmed during each programming cycle. Any byte can be programmed to any data pattern regardless of the current data in that byte. An internal timer uses 1 ms to program a byte. No additional time is required nor are any additional programming pulses.

VERIFY: A verify of programmed data may be performed with $\overline{CS1}$ at 12 volts by taking CS2 and CS3 to V_{IH}. The verify works exactly as a device read except that $\overline{CS1}$ is at 12 volts rather than V_{IL}.

MEMORY CELL: The AT28HC191 family of parts uses fully reprogrammable E^2PROM cells to store data. Unlike the one time programmable fuse link cells commonly found in bipolar PROMs, E^2PROM cells allow each bit to be fully tested before shipment by Atmel. The electrical reprogrammability of E^2PROM cells allows for multiple patterns to be written into each device during testing to ensure proper programming, functioning, and timing. All cells may be reprogrammed up to 1000 times by the user.

CHIP CLEAR: The entire contents of these memory devices may be set to the high state by the chip clear function. By setting $\overline{CS1}$ low and CS2 to 12 volts, the chip is cleared when a 10 msec low pulse is applied to CS3.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6 V to +6.25 V
All Output Voltages with Respect to Ground	-0.6 V to V_{CC} +0.6 V
Voltage on $\overline{CS1}$, CS2 and A9 with Respect to Ground	-0.6 V to +13.5 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5

D.C. and A.C. Operating Range

		AT28HC191-35	AT28HC191-45 AT28HC191L-45	AT28HC191-55 AT28HC191L-55
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	—	-40°C - 85°C	-40°C - 85°C
	Mil.	—	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 10%	5 V ± 10%	5 V ± 10%

D.C. Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}+1 V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0 V to V_{CC}			10	µA
I_{CC1}	V_{CC} Standby Current	$\overline{CS1}$ = V_{IH} ADDR = 0/V_{CC}	AT28HC191L		3	mA
			AT28HC191		60	mA
I_{CC}	V_{CC} Active Current	f = 10 MHz; I_{OUT} = 0 mA			80	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 12 mA			.4	V
V_{OH}	Output High Voltage	I_{OH} = -4.0 mA		2.4		V

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

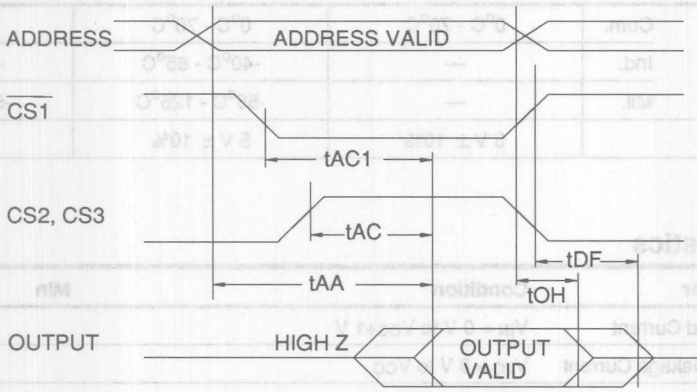
	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Note: 1. This parameter is only characterized and is not 100% tested.

A.C. Characteristics for Read Operation [1]

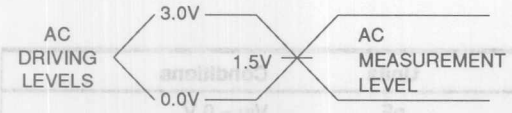
		AT28HC191						AT28HC191L				
		-35		-45		-55		-45		-55		
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{AA} [2]	Address to Output Delay		35		45		55		45		55	ns
t_{AC} [2]	CS2, CS3 to Output Delay		25		30		40		30		40	ns
t_{AC1} [2]	$\overline{CS1}$ to Output Delay		30		35		40		45		55	ns
t_{DF} [3,4]	$\overline{CS1}$, CS2, CS3 to Output Float	0	25	0	30	0	40	0	30	0	40	ns
t_{OH}	Output Hold from $\overline{CS1}$,CS2, CS3, or Address, whichever occurred first	0		0		0		0		0		ns

A.C. Read Waveforms



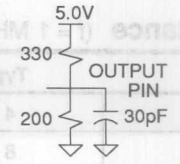
Notes:
1. CL = 30 pF
2. $\overline{CS}$, CS2 or CS3 may be delayed up to t_{AA}-t_{AC} after the address transition without impact on t_{AA}.
3. t_{DF} is specified from $\overline{CS1}$, CS2, or CS3, whichever occurs first.
4. This parameter is only characterized and is not 100% tested.

Input Test Waveforms and Measurement Levels



t_R, t_F < 5 ns

Output Test Load

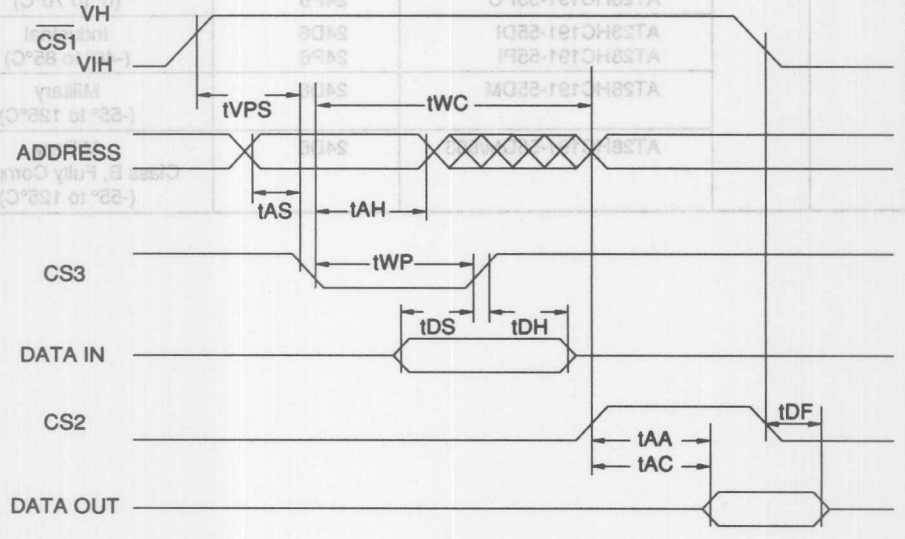


A.C. Write Characteristics

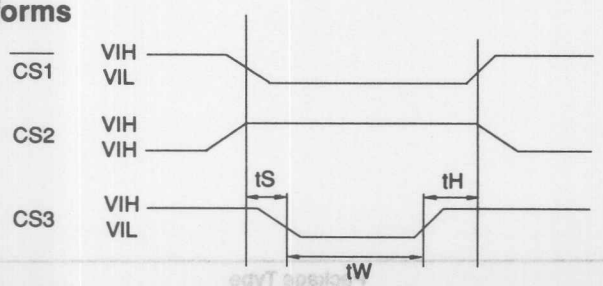
Symbol	Parameter	Min	Typ	Max	Units
t_{AS}	Address Set-up Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{WP}	Write Pulse Width	50		1000	ns
t_{DS}	Data Set-up Time	50			ns
t_{DH}	Data Hold Time	0			ns
t_{WC}	Write Cycle Time	1			ms
t_{VPS}	Programming Set-up Time	2			µs
t_{AA}	Address to Output Delay			100	ns
t_{AC}	CSn to Output Delay			100	ns
t_{DF}	CSn to Output Float			60	ns

5

A.C. Write Waveforms



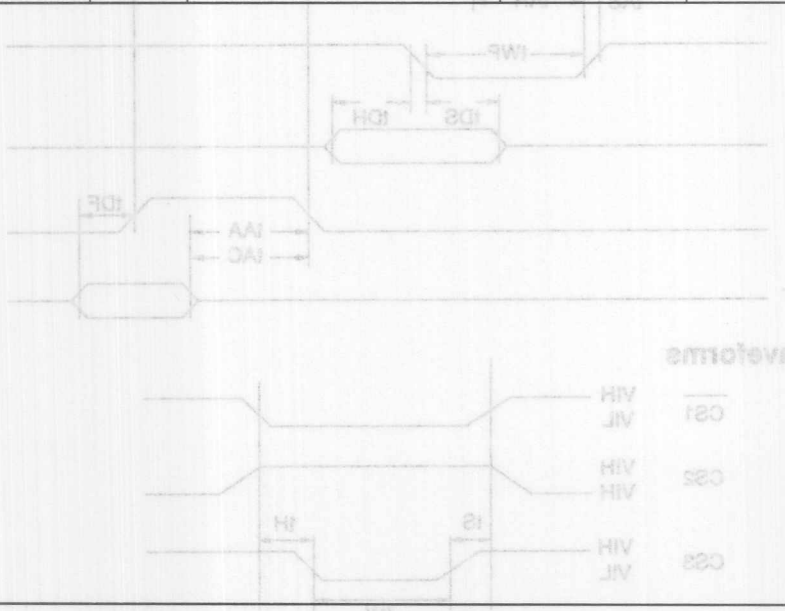
Chip Erase Waveforms



$t_S = t_H = 1$ µsec (min.)
$t_W = 10$ msec (min.)
$V_H = 12 \pm 0.5$ V

Ordering Information

tACC (ns)	ICC (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
35	80	60	AT28HC191-35DC AT28HC191-35PC	24D6 24P6	Commercial (0° to 70°C)
45	80	60	AT28HC191-45DC AT28HC191-45PC	24D6 24P6	Commercial (0° to 70°C)
			AT28HC191-45DI AT28HC191-45PI	24D6 24P6	Industrial (-40° to 85°C)
			AT28HC191-45DM	24D6	Military (-55° to 125°C)
			AT28HC191-45DM/883	24D6	Military/883C Class B, Fully Compliant (-55° to 125°C)
55	80	60	AT28HC191-55DC AT28HC191-55PC	24D6 24P6	Commercial (0° to 70°C)
			AT28HC191-55DI AT28HC191-55PI	24D6 24P6	Industrial (-40° to 85°C)
			AT28HC191-55DM	24D6	Military (-55° to 125°C)
			AT28HC191-55DM/883	24D6	Military Class B, Fully Compliant (-55° to 125°C)



Package Type	
24D6	24 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
24P6	24 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
45	80	3	AT28HC191L-45DC AT28HC191L-45PC	24D6 24P6	Commercial (0° to 70°C)
			AT28HC191L-45DI AT28HC191L-45PI	24D6 24P6	Industrial (-40° to 85°C)
			AT28HC191L-45DM	24D6	Military (-55° to 125°C)
			AT28HC191L-45DM/883	24D6	Military/883C Class B, Fully Compliant (-55° to 125°C)
55	80	3	AT28HC191L-55DC AT28HC191L-55PC	24D6 24P6	Commercial (0° to 70°C)
			AT28HC191L-55DI AT28HC191L-55PI	24D6 24P6	Industrial (-40° to 85°C)
			AT28HC191L-55DM	24D6	Military (-55° to 125°C)
			AT28HC191L-55DM/883	24D6	Military/883C Class B, Fully Compliant (-55° to 125°C)

5

Package Type	
24D6	24 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
24P6	24 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)

Ordering Code	Package	Operation Range
AT28HC16-45JC AT28HC16-45PC	24JS 24P6	Commercial (0° to 70°C)
AT28HC16-45JI AT28HC16-45PI	24JS 24P6	Industrial (-40° to 85°C)
AT28HC16-45DM	24DS	Military (-55° to 125°C)
AT28HC16-45DM/883	24DS	Military/883C Class B, Fully Compliant (-55° to 125°C)
AT28HC16-55JC AT28HC16-55PC	24JS 24P6	Commercial (0° to 70°C)
AT28HC16-55JI AT28HC16-55PI	24JS 24P6	Industrial (-40° to 85°C)
AT28HC16-55DM	24DS	Military (-55° to 125°C)
AT28HC16-55DM/883	24DS	Military/883C Class B, Fully Compliant (-55° to 125°C)

Package Type	
24DS	24 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
24P6	24 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)

Features

- Fast Access Time - 35 ns
- Low Power Dissipation
  - 100 µA Standby Current (AT28HC291L)
  - 80 mA Active Current
- E^2PROM Technology - 100% Reprogrammable
- Direct Replacement for Bipolar PROMs
- Reprogrammable 1000 times
- Chip Clear
- JEDEC Approved Byte-Wide Pinout
  - Space-Saving 300-mil Wide Package
- CMOS and TTL Compatible Inputs and Outputs
- High Reliability High Speed CMOS Technology
- Full Military, Commercial, and Industrial Temperature Ranges

16K (2K x 8) High Speed Electrically Erasable CMOS PROM

5

Description

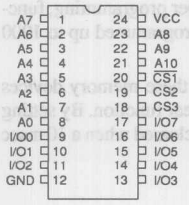
The AT28HC291/291L are a pair of high-speed, low-power 2,048 words by 8 bit CMOS PROMs. The high speed AT28HC291 offers access times to 35 ns while the AT28HC291L provides low standby current consumption of just 100 µA. Both devices are packaged in 24 pin dual inline packages using the JEDEC approved pinout for byte-wide PROMs. The AT28HC291 and AT28HC291L are supplied in space-saving 300-mil wide packages and also in 28 pad leadless chip carriers.

These devices are plug-in replacements for 16k bipolar PROMs, while offering distinct advantages in power consumption, performance and programming. Atmel's low power CMOS devices provide a direct power saving upgrade to systems originally using bipolar PROMs. The ultra-low standby power of the 28HC291L brings bipolar speeds to battery powered systems.

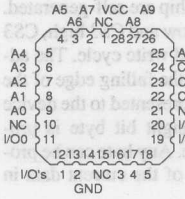
The electrically erasable and programmable memory cell allows for 100% testing of each memory location. The E^2PROM cell's low programming current permits devices to be programmed one byte at a time. On chip circuitry automatically erases each byte and rewrites it with the new data, permitting in socket reprogramming. The entire memory array can also be erased simultaneously, if desired, by using the device's "chip- clear" mode.

The fast access time of the devices makes them suitable for high-performance applications such as micro-control storage. In such an application the device allows for fast execution speeds, without penalizing storage density or power consumption. With a memory capacity of 2K bytes, these devices provide economical, reliable, and high-performance means of storing program instructions. System reliability is enhanced by the low power and inherent reliability of Atmel's 1.5 micron floating poly technology.

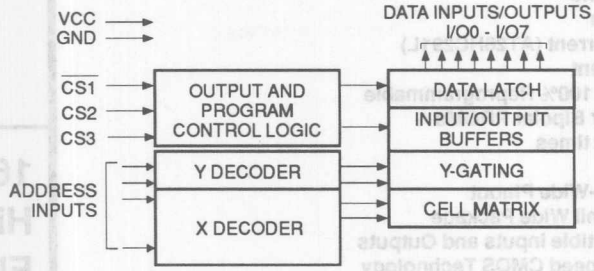
Pin Configurations



Pin Name	Function
A0-A10	Addresses
$\overline{CS1}$	Chip Select (Power Down Option)
CS2	Chip Select
CS3	Chip Select
I/O0-I/O7	Data
NC	No Connect



Block Diagram



Operating Modes

Mode	CS3	CS2	$\overline{CS1}$	I/O
Read	V_{IH}	V_{IH}	V_{IL}	D_{OUT}
Standby	X(1)	X	V_{IH}	High Z
Output Disable	V_{IL}	X	X	High Z
Output Disable	X	V_{IL}	X	High Z
Write(2)	V_{IL}	V_{IL}	V_H (3)	D_{IN}
Verify	V_{IH}	V_{IH}	V_H	D_{OUT}
Chip Clear	V_{IL}	V_H	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.
3. $V_H = 12.0 \pm 0.5$ V.

Device Operation

READ: When $\overline{CS1}$ is low and CS2 and CS3 are high, the data stored at the memory location determined by the address inputs is asserted on the outputs of the device. The outputs are put in a high impedance state whenever CS2 or CS3 is low or whenever $\overline{CS1}$ is high. The availability of three control lines gives the designer flexibility in preventing bus contention.

STANDBY: The AT28HC291L consumes less than 550 µW when deselected by raising $\overline{CS1}$ to V_{CC}-0.3V. This part retains the fast chip select times from CS2 and CS3 that are common to the AT28HC291.

PROGRAMMING: A 12 volt input is required on the $\overline{CS1}$ pin in order to program the devices. This input voltage is not needed to supply the programming current required by the memory cells as all high voltages used inside the chip are self-generated. After $\overline{CS1}$ is raised to 12 volts with CS2 low and CS3 high, CS3 is pulsed low to begin the internally timed write cycle. The address location presented to the device on the falling edge of the CS3 signal is written with the data that is presented to the device on the rising edge of CS3. An entire eight bit byte is programmed during each programming cycle. Any byte can be programmed to any data pattern regardless of the current data in that byte. An internal timer uses 1 ms to program a byte. No additional time is required nor are any additional programming pulses.

VERIFY: A verify of programmed data may be performed with $\overline{CS1}$ at 12 volts by taking CS2 and CS3 to VIH. The verify works exactly as a device read except that CS1 is at 12 volts rather than VIL.

MEMORY CELL: AT28HC291 family of parts uses fully reprogrammable E^2PROM cells to store data. Unlike the one time programmable fuse link cells commonly found in bipolar PROMs, E^2PROM cells allow each bit to be fully tested before shipment by Atmel. The electrical reprogrammability of E^2PROM cells allows for multiple patterns to be written into each device during testing to ensure proper programming, functioning and timing. All cells may be reprogrammed up to 1000 times by the user.

CHIP CLEAR: The entire contents of these memory devices may be set to the high state by the chip clear function. By setting $\overline{CS1}$ low and CS2 to 12 volts, the chip is cleared when a 10 msec low pulse is applied to CS3.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6 V to +6.25 V
All Output Voltages with Respect to Ground	-0.6 V to V_{CC} +0.6 V
Voltage on $\overline{CS1}$, CS2 and A9 with Respect to Ground	-0.6 V to +13.5 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5

D.C. and A.C. Operating Range

		AT28HC291-35	AT28HC291-45 AT28HC291L-45	AT28HC291-55 AT28HC291L-55
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	—	-40°C - 85°C	-40°C - 85°C
	Mil.	—	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 10%	5 V ± 10%	5 V ± 10%

D.C. Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}+1 V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0 V to V_{CC}			10	µA
I_{CC1}	V_{CC} Standby Current	$\overline{CS1}$ = V_{IH} ADDR = 0/V_{CC}	AT28HC291L		3	mA
			AT28HC291		60	mA
I_{CC}	V_{CC} Active Current	f = 10 MHz; I_{OUT} = 0 mA			80	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 12 mA			.4	V
V_{OH}	Output High Voltage	I_{OH} = -4.0 mA		2.4		V

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

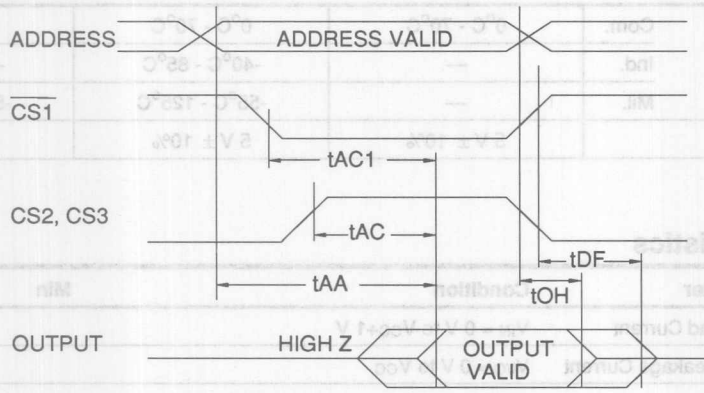
	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Note. 1. This parameter is only characterized and is not 100% tested.

A.C. Characteristics for Read Operation [1]

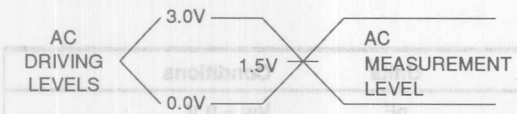
Symbol	Parameter	AT28HC291 -35 Min	AT28HC291 -35 Max	AT28HC291 -45 Min	AT28HC291 -45 Max	AT28HC291 -55 Min	AT28HC291 -55 Max	AT28HC291L -45 Min	AT28HC291L -45 Max	AT28HC291L -55 Min	AT28HC291L -55 Max	Units
t_{AA} [2]	Address to Output Delay		35		45		55		45		55	ns
t_{AC} [2]	CS2, CS3 to Output Delay		25		30		40		30		40	ns
t_{AC1} [2]	$\overline{CS1}$ to Output Delay		30		35		40		45		55	ns
t_{DF} [3,4]	$\overline{CS1}$, CS2, CS3 to Output Float	0	25	0	30	0	40	0	30	0	40	ns
t_{OH}	Output Hold from $\overline{CS1}$,CS2, CS3, or Address, whichever occurred first	0		0		0		0		0		ns

A.C. Read Waveforms



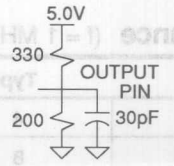
Notes:
1. CL = 30 pF
2. $\overline{CS}$, CS2 or CS3 may be delayed up to t_{AA}-t_{AC} after the address transition without impact on t_{AA}.
3. t_{DF} is specified from $\overline{CS1}$, CS2, or CS3, whichever occurs first.
4. This parameter is only characterized and is not 100% tested.

Input Test Waveforms and Measurement Levels



t_R, t_F < 5 ns

Output Test Load

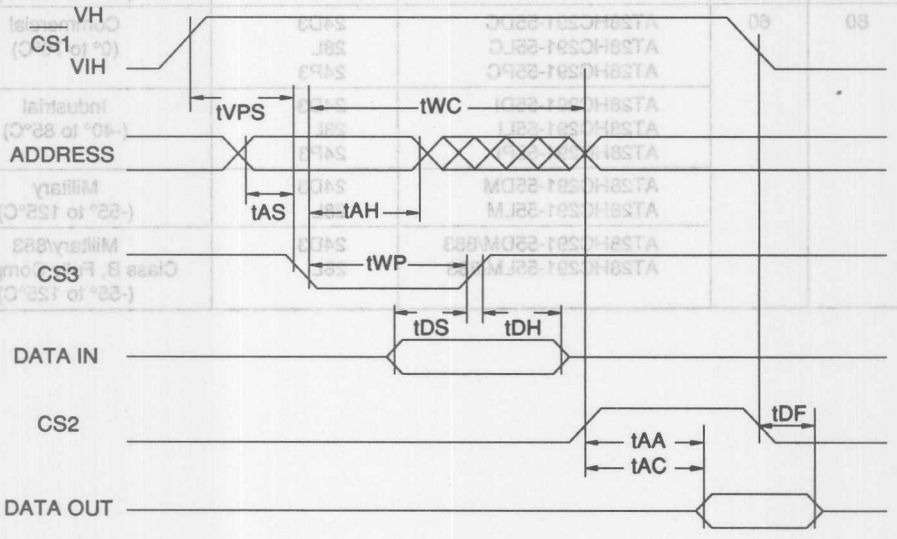


A.C. Write Characteristics

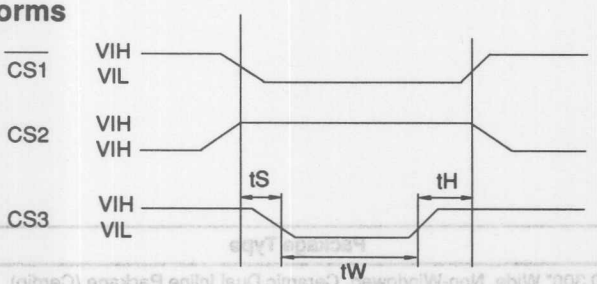
Symbol	Parameter	Min	Typ	Max	Units
t_{AS}	Address Set-up Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{WP}	Write Pulse Width	50		1000	ns
t_{DS}	Data Set-up Time	50			ns
t_{DH}	Data Hold Time	0			ns
t_{WC}	Write Cycle Time	1			ms
t_{VPS}	Programming Set-up Time	2			µs
t_{AA}	Address to Output Delay			100	ns
t_{AC}	CSn to Output Delay			100	ns
t_{DF}	CSn to Output Float			60	ns

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A.C. Write Waveforms



Chip Erase Waveforms



$t_S = t_H = 1$ µsec (min.)
$t_W = 10$ msec (min.)
$V_H = 12 \pm 0.5$ V

tACC (ns)	ICC (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
35	80	60	AT28HC291-35DC AT28HC291-35PC	24D3 24P3	Commercial (0° to 70°C)
45	80	60	AT28HC291-45DC AT28HC291-45LC AT28HC291-45PC	24D3 28L 24P3	Commercial (0° to 70°C)
			AT28HC291-45DI AT28HC291-45LI AT28HC291-45PI	24D3 28L 24P3	Industrial (-40° to 85°C)
			AT28HC291-45DM AT28HC291-45LM	24D3 28L	Military (-55° to 125°C)
			AT28HC291-45DM/883 AT28HC291-45LM/883	24D3 28L	Military/883C Class B, Fully Compliant (-55° to 125°C)
55	80	60	AT28HC291-55DC AT28HC291-55LC AT28HC291-55PC	24D3 28L 24P3	Commercial (0° to 70°C)
			AT28HC291-55DI AT28HC291-55LI AT28HC291-55PI	24D3 28L 24P3	Industrial (-40° to 85°C)
			AT28HC291-55DM AT28HC291-55LM	24D3 28L	Military (-55° to 125°C)
			AT28HC291-55DM/883 AT28HC291-55LM/883	24D3 28L	Military/883 Class B, Fully Compliant (-55° to 125°C)

Package Type	
24D3	24 Lead, 0.300" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
28L	28 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
24P3	24 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
45	80	3	AT28HC291L-45DC AT28HC291L-45PC	24D3 24P3	Commercial (0° to 70°C)
			AT28HC291L-45DI AT28HC291L-45PI	24D3 24P3	Industrial (-40° to 85°C)
			AT28HC291L-45DM	24D3	Military (-55° to 125°C)
			AT28HC291L-45DM/883	24D3	Military/883C Class B, Fully Compliant (-55° to 125°C)
55	80	3	AT28HC291L-55DC AT28HC291L-55LC AT28HC291L-55PC	24D3 28L 24P3	Commercial (0° to 70°C)
			AT28HC291L-55DI AT28HC291L-55LI AT28HC291L-55PI	24D3 28L 24P3	Industrial (-40° to 85°C)
			AT28HC291L-55DM AT28HC291L-55LM	24D3 28L	Military (-55° to 125°C)
			AT28HC291L-55DM/883 AT28HC291L-55LM/883	24D3 28L	Military/883 Class B, Fully Compliant (-55° to 125°C)

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Package Type	
24D3	24 Lead, 0.300" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
28L	28 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
24P3	24 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
45	80	3	AT28HC29TL-45DC AT28HC29TL-45PC	24D3 24P3	Commercial (0° to 70°C)
			AT28HC29TL-45DI AT28HC29TL-45PI	24D3 24P3	Industrial (-40° to 85°C)
			AT28HC29TL-45DM	24D3	Military (-55° to 125°C)
			AT28HC29TL-45DM/883	24D3	Military/883C Class B, Fully Compliant (-55° to 125°C)
55	80	3	AT28HC29TL-55DC AT28HC29TL-55LC AT28HC29TL-55PC	24D3 28L 24P3	Commercial (0° to 70°C)
			AT28HC29TL-55DI AT28HC29TL-55LI AT28HC29TL-55PI	24D3 28L 24P3	Industrial (-40° to 85°C)
			AT28HC29TL-55DM AT28HC29TL-55LM	24D3 28L	Military (-55° to 125°C)
			AT28HC29TL-55DM/883 AT28HC29TL-55LM/883	24D3 28L	Military/883 Class B, Fully Compliant (-55° to 125°C)

Package Type	
24D3	24 Lead, 0.300" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
28L	28 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
24P3	24 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)

Features

- **Bipolar Speed**
  - **Read Access Time - 35 ns**
- **Low Power CMOS Operation**
  - **25 mA max. Standby**
  - **45 mA max. Active at 10 MHz**
- **Direct Bipolar PROM Replacement**
- **High Output Drive Capability**
- **Reprogrammable - 100 µs/byte (typical)**
  - **Tested 100% for Programmability**
- **JEDEC Approved Byte-Wide Pinout**
  - **300-mil DIP, 600-mil DIP and LCC packages**
- **CMOS and TTL Compatible Inputs and Outputs**
- **High Reliability Latch-Up Resistant CMOS Technology**
- **Integrated Product Identification Code**
- **Full Military, Industrial and Commercial Temperature Ranges**
- **Fully Compatible with AT27HC641/2**

64K (8K x 8) Reprogrammable CMOS PROM

5

Description

The AT27HC641R/642R chip family is a high-speed, low-power 65,536 bit reprogrammable read only memory (PROM), which is UV erasable, organized as 8K x 8 bits. All devices require only one 5 V power supply in normal read mode operation. All bytes on the 641R and 642R parts can be accessed in less than 35 ns, making these parts ideal for high-performance systems without penalizing bit density or power consumption.

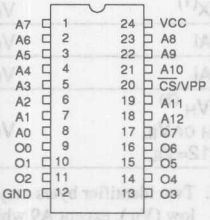
The 640R series of devices come in a choice of JEDEC-approved 24-pin DIP or 28-pad LCC packages, providing a direct power saving CMOS upgrade for systems originally using Bipolar PROMs. The AT27HC641R is available in a standard 600-mil cerdip or one-time programmable plastic (OTP) package, and LCC package, while the AT27HC642R is available in a space-saving 300-mil cerdip or plastic (OTP) package.

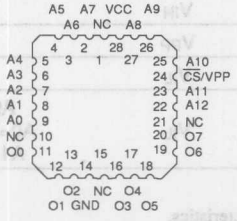
Atmel's 1.2-micron, high-speed CMOS technology provides optimum speed, low-power and high noise immunity. Power consumption on the AT27HC641 and AT27HC642 is typically only 30 mA in Active Mode and less than 10 mA in Standby. The high speed CMOS process is an extension of Atmel's high quality and highly manufacturable floating poly PROM technology. The ability to reprogram the PROM, which is fully tested before shipment, provides inherently better programmability and reliability than one-time fusable PROMs.

continued on next page

Pin Configurations

Pin Name	Function
A0-A12	Addresses
$\overline{CS}$/VPP	Chip Select/VPP
O0-O7	Outputs





Description (Continued)

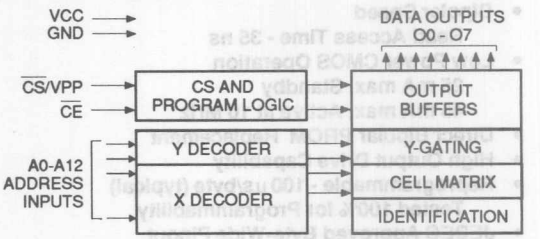
With a storage capacity of 8K bytes, Atmel's 640R series parts allow firmware to be stored reliably and to be accessed at bipolar PROM speeds. All the 640R series parts have exceptional output drive capability - source 4 mA and sink 16 mA per output.

Atmel's 640R series chips also have additional features to ensure high-quality and efficient production use. The Rapid programming algorithm reduces the time required to program the chip and guarantees reliable programming. The Integrated Product Identification Code electronically identifies the device and manufacturing origin. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Erasure Characteristics

The entire memory array of an Atmel 640R series chip is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15W·sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any PROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Voltage on A9 with Respect to Ground	-2.0 V to +14.0 V(1)
$\overline{CS}$/VPP Supply Voltage with Respect to Ground	-2.0 V to +14.0 V(1)
Integrated UV Erase Dose	7258 W•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC}+0.75 V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

Operating Modes

MODE \ PIN	$\overline{CS}$/VPP	Ai	VCC	Outputs
Read	V_{IL}	Ai	VCC	DOUT
Standby	V_{IH}	X(1)	VCC	High Z
Rapid Program(2)	VPP	Ai	VCC	DIN
PGM Verify	V_{IL}	Ai	VCC	DOUT
Product Identification(4)	V_{IL}	A9=V_H (3) A0=V_{IH} or V_{IL} A1-A12=V_{IL}	VCC	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. V_H = 12.0 ± 0.5 V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

D.C. and A.C. Operating Conditions for Read Operation

		AT27HC641R / AT27HC642R				
		-35	-45	-55	-70	-90
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.		-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 5%	5 V ± 10%	5 V ± 10%	5 V ± 10%	5 V ± 10%

D.C. and Operating Characteristics for Read Operation

5

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1 V to V_{CC}+1 V			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1 V to V_{CC}+0.1 V			10	µA
I_{PP1}	$\overline{CS}/V_{PP}$ (1) Read/Standby Current	$\overline{CS}/V_{PP}$ = -0.1 V to V_{CC}+1 V			10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS) $\overline{CS}/V_{PP}$ = V_{CC}-0.3 to V_{CC}+1.0 V	Com.		25	mA
			Ind.,Mil.		30	mA
		I_{SB2} (TTL) $\overline{CS}/V_{PP}$ = 2.0 to V_{CC}+1.0 V	Com.		25	mA
			Ind.,Mil.		30	mA
I_{CC}	V_{CC} Active Current	f = 10 MHz, I_{OUT} = 0 mA, $\overline{CS}/V_{PP}$ = V_{IL}	Com.		45	mA
			Ind.,Mil.		50	mA
I_{OS} (2)	Output Short Circuit Current	V_{OUT} = 0 V			-100	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC}+0.75	V
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			.4	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA		V_{CC}-0.3		V
		I_{OH} = -4.0 mA		2.4		V

Notes: 1. V_{CC} must be applied simultaneously or before $\overline{CS}/V_{PP}$, and removed simultaneously or after $\overline{CS}/V_{PP}$.

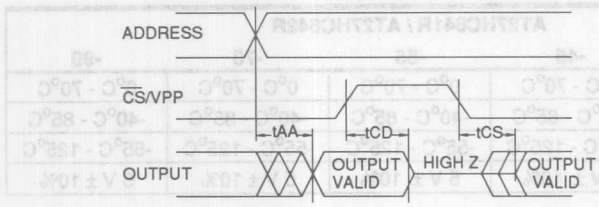
2. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec. This parameter is only sampled and is not 100% tested. See Absolute Maximum Ratings.

A.C. Characteristics for Read Operation

			AT27HC641R / AT27HC642R										
			-35		-45		-55		-70		-90		
Symbol	Parameter		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{AA} (4)	Address to Output Delay	Com.		35		45		55		70		90	ns
		Ind.,Mil				45		55		70		90	ns
t_{CS} (2,4)	$\overline{CS}/V_{PP}$ to Output Delay			25		30		35		45		55	ns
t_{CD} (3,4,5)	$\overline{CS}/V_{PP}$ to Output Float		0	25	0	30	0	35	0	40	0	45	ns

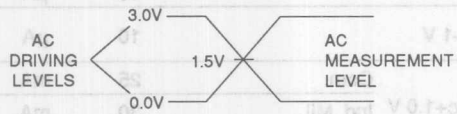
Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

A.C. Waveforms for Read Operation (1)



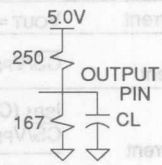
Notes:
1. Timing measurement reference is 1.5 V. Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.
2. Asserting $\overline{CS}/V_{PP}$ may be delayed up to t_{AA} - t_{CS} after the address transition without impact on access time.
3. This parameter is only sampled and is not 100% tested.
4. C_L = 30 pF, add 10 ns for C_L = 100 pF.
5. Output float is defined as the point when data is no longer driven.

Input Test Waveforms and Measurement Levels



t_R, t_F < 5 ns (10% to 90%)

Output Test Load



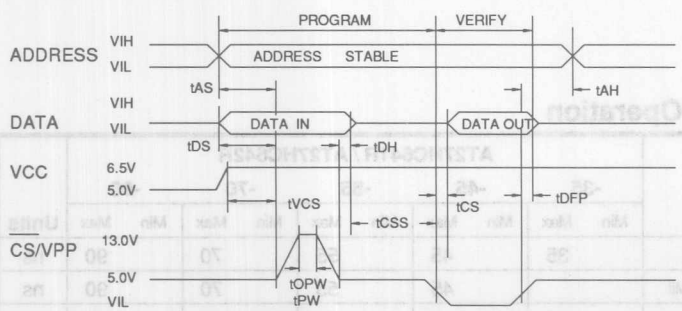
Note: C_L=30pF including jig capacitance.

Pin Capacitance (f = 1 MHz T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms (1)



Notes:
1. The Input Timing References are 0.0 V for V_{IL} and 3.0 V for V_{IH}.
2. t_{CS} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

D.C. Programming Characteristics

T_A= 25 ± 5°C, V_{CC} = 6.5± 0.25 V, $\overline{CS}/V_{PP}$ = 13.0 ± 0.25 V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC}+1	V
V_{OL}	Output Low Volt.	I_{OL} = 16 mA		.4	V
V_{OH}	Output High Volt.	I_{OH}= -4.0 mA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			50	mA
I_{PP2}	$\overline{CS}/V_{PP}$ Supply Current	$\overline{CS}/V_{PP}=V_{PP}$		30	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

T_A = 25 ± 5°C, V_{CC}= 6.5 ± 0.25 V, $\overline{CS}/V_{PP}$=13.0 ± 0.25 V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Limits Max	Units
t_{AS}	Address Setup Time		2		µs
t_{CSS}	$\overline{CS}/V_{PP}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{CS}/V_{PP}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CS}/V_{PP}$ Program Pulse Width	(Note 3)	95	105	µs
t_{CS}	Data Valid from $\overline{CS}/V_{PP}$			70	ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) ..... 5 ns
Input Pulse Levels ..... 0.0 V to 3.0 V
Input Timing Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V

Notes:

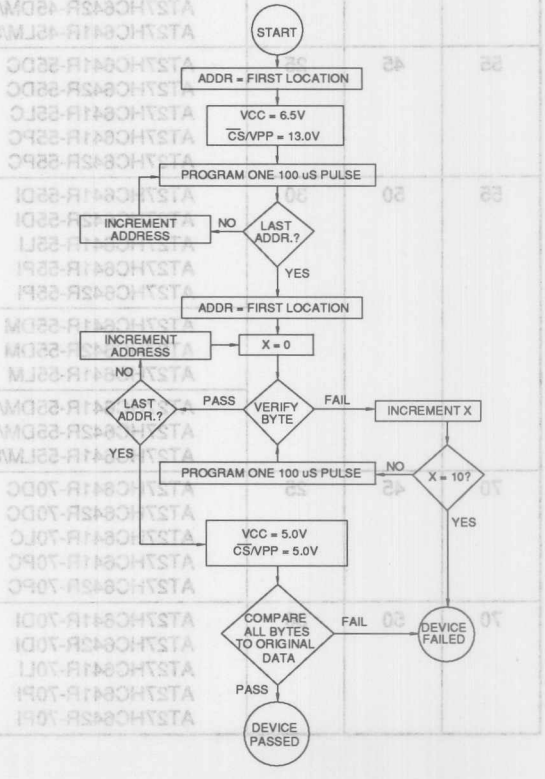
1. V_{CC} must be applied simultaneously or before $\overline{CS}/V_{PP}$ and removed simultaneously or after $\overline{CS}/V_{PP}$.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100 µsec ± 5%.

Atmel's 27HC641R/2R Integrated Product Identification Code

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	0	0	0	1	0	0	0	0	10

Rapid Programming Algorithm

A 100 µs $\overline{CS}/V_{PP}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5 V and $\overline{CS}/V_{PP}$ is raised to 13.0 V. Each address is first programmed with one 100 µs $\overline{CS}/V_{PP}$ pulse without verification. Then a verification / reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. $\overline{CS}/V_{PP}$ is then lowered to 5.0 V and V_{CC} to 5.0 V. All bytes are read again and compared with the original data to determine if the device passes or fails.



5

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
35	45	25	AT27HC641R-35DC AT27HC642R-35DC AT27HC641R-35LC	24DW6 24DW3 28LW	Commercial (0°C to 70°C)
45	45	25	AT27HC641R-45DC AT27HC642R-45DC AT27HC641R-45LC AT27HC641R-45PC AT27HC642R-45PC	24DW6 24DW3 28LW 24P6 24P3	Commercial (0°C to 70°C)
45	50	30	AT27HC641R-45DI AT27HC642R-45DI AT27HC641R-45LI AT27HC641R-45PI AT27HC642R-45PI	24DW6 24DW3 28LW 24P6 24P3	Industrial (-40°C to 85°C)
			AT27HC641R-45DM AT27HC642R-45DM AT27HC641R-45LM	24DW6 24DW3 28LW	Military (-55°C to 125°C)
			AT27HC641R-45DM/883 AT27HC642R-45DM/883 AT27HC641R-45LM/883	24DW6 24DW3 28LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
55	45	25	AT27HC641R-55DC AT27HC642R-55DC AT27HC641R-55LC AT27HC641R-55PC AT27HC642R-55PC	24DW6 24DW3 28LW 24P6 24P3	Commercial (0°C to 70°C)
55	50	30	AT27HC641R-55DI AT27HC642R-55DI AT27HC641R-55LI AT27HC641R-55PI AT27HC642R-55PI	24DW6 24DW3 28LW 24P6 24P3	Industrial (-40°C to 85°C)
			AT27HC641R-55DM AT27HC642R-55DM AT27HC641R-55LM	24DW6 24DW3 28LW	Military (-55°C to 125°C)
			AT27HC641R-55DM/883 AT27HC642R-55DM/883 AT27HC641R-55LM/883	24DW6 24DW3 28LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
70	45	25	AT27HC641R-70DC AT27HC642R-70DC AT27HC641R-70LC AT27HC641R-70PC AT27HC642R-70PC	24DW6 24DW3 28LW 24P6 24P3	Commercial (0°C to 70°C)
70	50	30	AT27HC641R-70DI AT27HC642R-70DI AT27HC641R-70LI AT27HC641R-70PI AT27HC642R-70PI	24DW6 24DW3 28LW 24P6 24P3	Industrial (-40°C to 85°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	50	30	AT27HC641R-70DM AT27HC642R-70DM AT27HC641R-70LM	24DW6 24DW3 28LW	Military (-55°C to 125°C)
			AT27HC641R-70DM/883 AT27HC642R-70DM/883 AT27HC641R-70LM/883	24DW6 24DW3 28LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	45	25	AT27HC641R-90DC AT27HC642R-90DC AT27HC641R-90LC AT27HC641R-90PC AT27HC642R-90PC	24DW6 24DW3 28LW 24P6 24P3	Commercial (0°C to 70°C)
90	50	30	AT27HC641R-90DI AT27HC642R-90DI AT27HC641R-90LI AT27HC641R-90PI AT27HC642R-90PI	24DW6 24DW3 28LW 24P6 24P3	Industrial (-40°C to 85°C)
			AT27HC641R-90DM AT27HC642R-90DM AT27HC641R-90LM	24DW6 24DW3 28LW	Military (-55°C to 125°C)
			AT27HC641R-90DM/883 AT27HC642R-90DM/883 AT27HC641R-90LM/883	24DW6 24DW3 28LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
45	50	30	5962-87515 01 JX 5962-87515 01 KX 5962-87515 01 LX 5962-87515 01 3X	24DW6 24CW 24DW3 28LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
55	50	30	5962-87515 02 JX 5962-87515 02 KX 5962-87515 02 LX 5962-87515 02 3X	24DW6 24CW 24DW3 28LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
70	50	30	5962-87515 03 JX 5962-87515 03 KX 5962-87515 03 LX 5962-87515 03 3X	24DW6 24CW 24DW3 28LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	50	30	5962-87515 04 JX 5962-87515 04 KX 5962-87515 04 LX 5962-87515 04 3X	24DW6 24CW 24DW3 28LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
24CW	24 Lead, Windowed, Ceramic Flat Package (Cerpack)
24DW3	24 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
24DW6	24 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
28LW	28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
24P3	24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
24P6	24 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	50	30	AT27HC641R-70DM AT27HC642R-70DM AT27HC641R-70JM	24DW6 24DW3 28JW	Military (-55°C to 125°C)
			AT27HC641R-70DM/883 AT27HC642R-70DM/883 AT27HC641R-70JM/883	24DW6 24DW3 28JW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	45	25	AT27HC641R-90DC AT27HC642R-90DC AT27HC641R-90JC AT27HC641R-90PC AT27HC642R-90PC	24DW6 24DW3 28JW 24P6 24P3	Commercial (0°C to 70°C)
90	50	30	AT27HC641R-90DI AT27HC642R-90DI AT27HC641R-90JI AT27HC641R-90PI AT27HC642R-90PI	24DW6 24DW3 28JW 24P6 24P3	Industrial (-40°C to 85°C)
			AT27HC641R-90DM AT27HC642R-90DM AT27HC641R-90JM	24DW6 24DW3 28JW	Military (-55°C to 125°C)
			AT27HC641R-90DM/883 AT27HC642R-90DM/883 AT27HC641R-90JM/883	24DW6 24DW3 28JW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
45	50	30	5962-87515 01 JX 5962-87515 01 KX 5962-87515 01 LX 5962-87515 01 3X	24DW6 24CW 24DW3 28JW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
55	50	30	5962-87515 02 JX 5962-87515 02 KX 5962-87515 02 LX 5962-87515 02 3X	24DW6 24CW 24DW3 28JW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
70	50	30	5962-87515 03 JX 5962-87515 03 KX 5962-87515 03 LX 5962-87515 03 3X	24DW6 24CW 24DW3 28JW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	50	30	5962-87515 04 JX 5962-87515 04 KX 5962-87515 04 LX 5962-87515 04 3X	24DW6 24CW 24DW3 28JW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
24CW	24 Lead, Windowed, Ceramic Flat Package (Cerpack)
24DW3	24 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
24DW6	24 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
28JW	28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
24P3	24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
24P6	24 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)

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E^2PROMs 2
PEROMs (Flash) 3
EPROMs 4
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SRAMs 6
EPLDs 7
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Product Information

2 E²PROMs

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Contents

Section 6

CMOS SRAMs

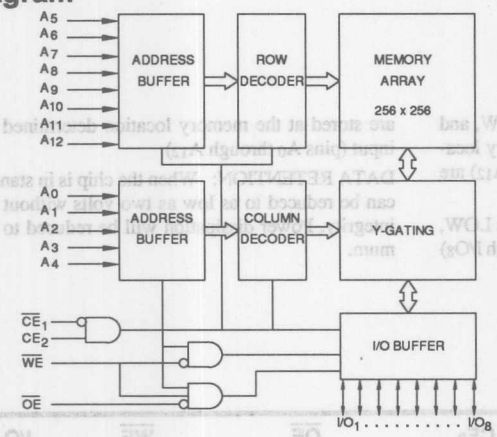
AT3864L	8K x 8	64K SRAM	6-3
AT3864L-15DMB	8K x 8	64K SRAM, Full Military Temperature	6-11
AT38H256	32K x 8	256K SRAM	6-19
AT38LV256	32K x 8	Low Voltage, 256K SRAM	6-27

Features

- Fast Read Access Time - 100 ns
- Low Power
  - 35 mA Maximum (Active)
  - 100 µA Maximum (Standby)
- 2-V Data Retention
- Fully Static: No Clock Required
- Three Control Inputs ($\overline{CE_1}$, CE_2, and $\overline{OE}$)
- TTL Compatible Inputs and Outputs
- 5 V ± 10% Supply
- 28-Lead Dual In-line and Surface Mount Packages
- JEDEC Pinout
- Commercial and Industrial Temperature Ranges

64K (8K x 8) CMOS SRAM

Block Diagram



Description

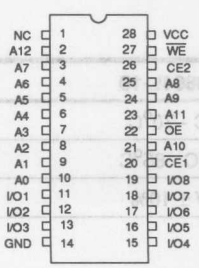
The AT3864L is a high performance CMOS static Random Access Memory. Its 64K of memory is organized as 8192 words by 8 bits. Manufactured with an advanced CMOS technology, the AT3864L offers access times down to 100 ns with power dissipation of under 200 mW. When the AT3864L is deselected, the standby current is just 100 µA. In addition, the AT3864L offers a data retention capability of only 100 µW power dissipation when operated on a 2-volt power supply.

The AT3864L powers down to the standby mode when deselected ($\overline{CE_1}$ is HIGH or CE_2 is LOW). The I/O pins remain in the high impedance state unless the chip is selected ($\overline{CE_1}$ is LOW and CE_2 is HIGH), the outputs are enabled ($\overline{OE}$ is LOW), and Write Enable is not active ($\overline{WE}$ is HIGH).

The AT3864L is completely TTL compatible and requires a single 5-volt power supply. The device is fully static and does not need any clocks or refresh control signals for operation.

Pin Configurations

Pin Name	Function
A_0-A_{12}	Addresses
I/O_1-I/O_8	Outputs
$\overline{CE_1}$, CE_2	Chip Enables
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}, GND	Power, Ground
NC	No Connect



Absolute Maximum Ratings*

Temperature Under Bias	-40° C to 85° C
Storage Temperature	-55° C to 125° C
All Input Voltages (including NC Pins) with Respect to Ground	-0.3 V to V_{CC}+0.3 V
All Output Voltages with Respect to Ground	-0.3 V to V_{CC}+0.3 V
Maximum Supply Voltage	+7.0 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: When $\overline{CE_1}$ is LOW, CE_2 is HIGH, $\overline{OE}$ is LOW, and $\overline{WE}$ is HIGH, the eight bits of data stored at the memory location determined by the address input (pins A_0 through A_{12}) are inserted on the data outputs (pins I/O_1 through I/O_8).

WRITE: When $\overline{CE_1}$ is LOW, CE_2 is HIGH, and $\overline{WE}$ is LOW, the eight bits of data placed on the input pins (I/O_1 through I/O_8) are stored at the memory location determined by the address input (pins A_0 through A_{12}).

DATA RETENTION: When the chip is in standby mode, V_{CC} can be reduced to as low as two volts without impacting data integrity. Power dissipation will be reduced to 100 µW maximum.

Operating Modes

MODE\PIN	$\overline{CE_1}$	CE_2	$\overline{OE}$	$\overline{WE}$	I/O
Read	L	H	L	H	D_{OUT}
Write	L	H	X(1)	L	D_{IN}
$Standby_1$	H	X	X	X	High Z
$Standby_2$	X	L	X	X	High Z
Output Disable	X	X	H	X	High Z

Note: 1. X can be L (Low) or H (High)

D.C. and A.C. Operating Range

		AT3864L-10	AT3864L-12	AT3864L-15
Operating Temperature (Case)	Commercial	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Industrial	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5 V ± 10%	5 V± 10%	5 V± 10%

D.C. and Operating Characteristics

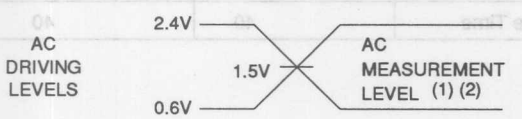
Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0 to V_{CC}	-1.0		1.0	µA
I_{LO}	Output Leakage Current	$\overline{CE_1}$ = 2.2 V to V_{CC} + 0.3 V or CE_2 = -0.3 V to 0.8 V or $\overline{OE}$ = 2.2 V to V_{CC} + 0.3 V or $\overline{WE}$ = -0.3 V to 0.8 V $V_{I/O}$ = 0 to V_{CC}	-1.0		1.0	µA
I_{SB1}	Standby Current (CMOS)	$CE_2 \le 0.2$ V or $\overline{CE_1} \ge V_{CC}$ - 0.2 V, $CE_2 \ge V_{CC}$ - 0.2 V or $CE_2 \le 0.2$ V V_{IN} = 0 to V_{CC}		2	100	µA
I_{SB2}	Standby Current (TTL)	CE_2 = -0.3 V to 0.8 V or $\overline{CE_1}$ = 2.2 V to V_{CC} +0.3 V, V_{IN} = 0 to V_{CC}			3	mA
I_{CC}	V_{CC} Active Current (TTL)	$\overline{CE_1}$ = -0.3 V to 0.8 V, CE_2 = 2.2 V to V_{CC} + 0.3 V, I_{OUT} = 0 mA, min cycle		20	35	mA
V_{IL}	Input Low Voltage		-0.3		0.8	V
V_{IH}	Input High Voltage		2.2 V		V_{CC}+0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -1.0 mA	2.4			V

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0 V		6	10	pF
C_{IN}	Input Capacitance	V_{IN} = 0 V		6	10	pF

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Input Test Waveforms and Measurement Levels



Notes: 1. Input rise and fall time 5 ns.
2. Output load: 1TTL gate + 10 0pF.

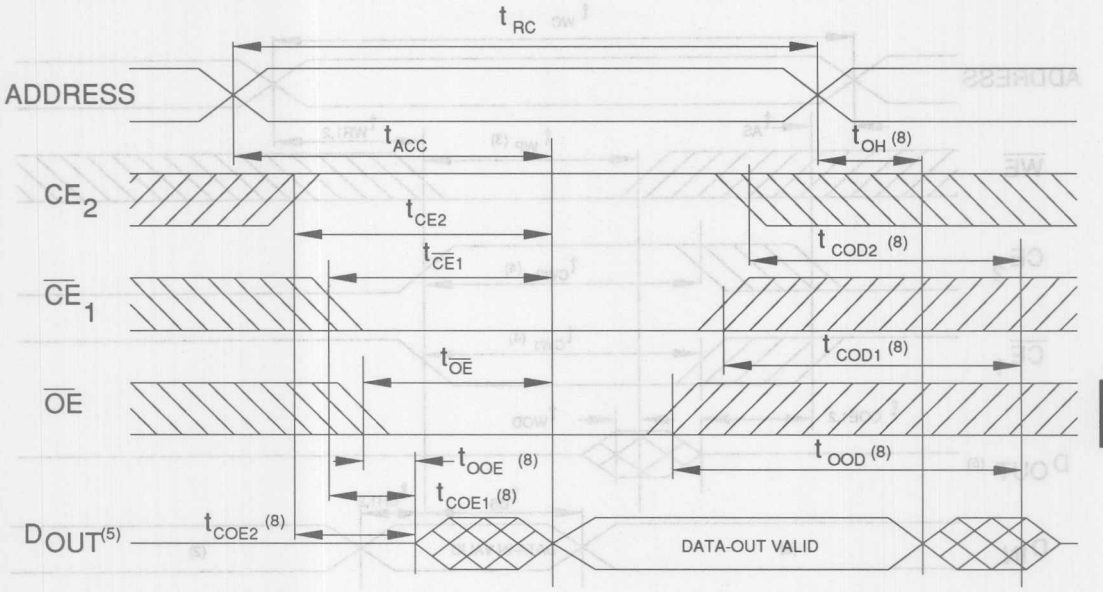
A.C. Characteristics for Read

Symbol	Parameter	AT3864L-10		AT3864L-12		AT3864L-15		Units
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	100		120		150		ns
t_{ACC}	Address Access Time		100		120		150	ns
$t_{\overline{CE}1}$,t_{CE2}	$\overline{CE}_1$,CE_2 Access Time		100		120		150	ns
$t_{\overline{OE}}$	$\overline{OE}$ Access Time		50		60		70	ns
t_{OH}	Output Hold Time	15		15		15		ns
$t_{COE1,2}$	$\overline{CE}_1$, CE_2 Output Enable Time	10		10		10		ns
t_{OOE}	$\overline{OE}$ Output Enable Time	5		5		5		ns
$t_{COD1,2}$	$\overline{CE}_1$, CE_2 Output Disable Time		45		45		60	ns
t_{OOD}	$\overline{OE}$ Output Disable Time		40		40		50	ns

A.C. Characteristics for Write

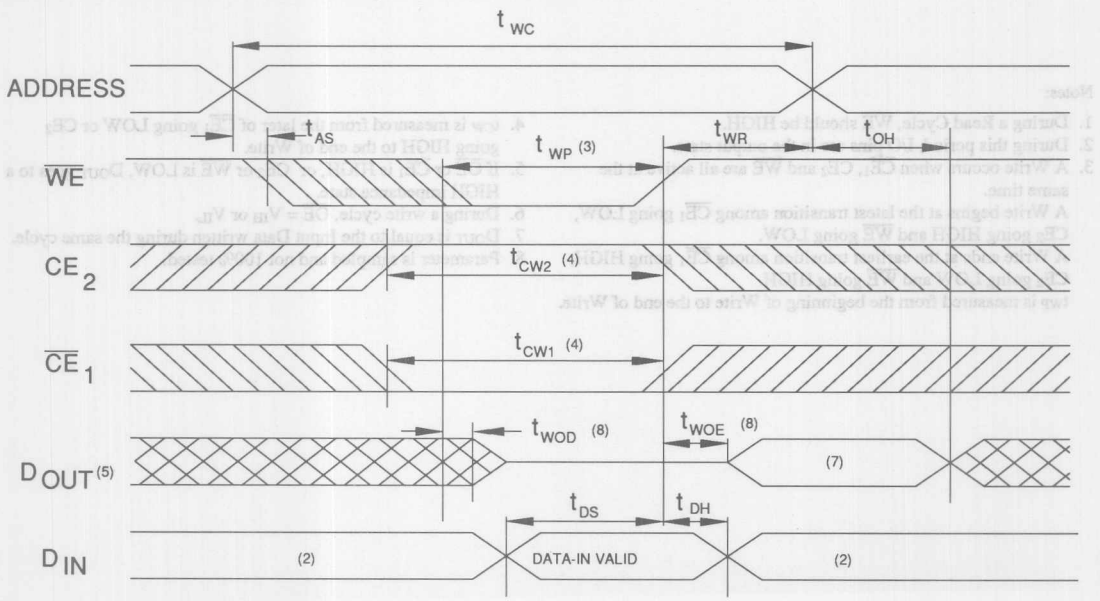
Symbol	Parameter	AT3864L-10		AT3864L-12		AT3864L-15		Units
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	100		120		150		ns
t_{AS}	Address Setup Time	0		0		0		ns
t_{WP}	Write Pulse Width	60		70		90		ns
$t_{CW1,2}$	$\overline{CE}_1$, CE_2 Setup Time	80		80		90		ns
t_{WR}	Write Recovery Time	0		0		0		ns
$t_{WR1,2}$	$\overline{CE}_1$, CE_2 Write Recovery Time	0		0		0		ns
t_{DS}	Data Setup Time	40		50		60		ns
t_{DH}	Data Hold Time	0		0		0		ns
$t_{DH1,2}$	$\overline{CE}_1$, CE_2 Data Hold Time	0		0		0		ns
t_{WOE}	$\overline{WE}$ Output Enable Time	5		5		5		ns
t_{WOD}	$\overline{WE}$ Output Disable Time		40		40		50	ns

A.C. Waveforms for Read Cycle [1]

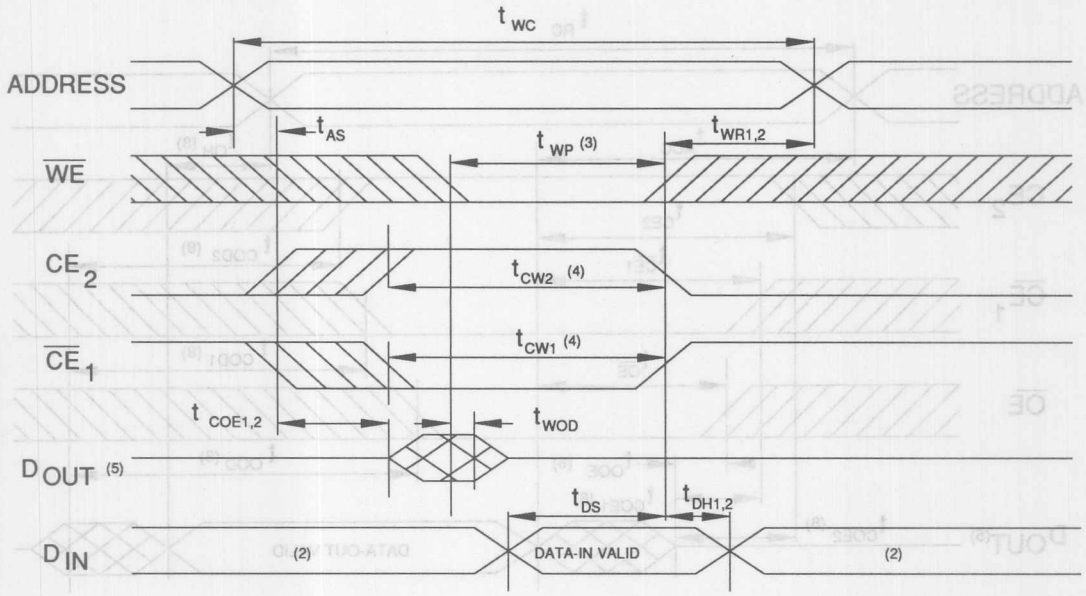


6

A.C. Waveforms for Write Cycle 1 ($\overline{WE}$ Write) [6]



A.C. Waveforms for Write Cycle 2 ($\overline{WE}$ Write) (6)



Notes:

1. During a Read Cycle, $\overline{WE}$ should be HIGH.
2. During this period, I/O pins are in the output state.
3. A Write occurs when $\overline{CE_1}$, CE_2 and $\overline{WE}$ are all active at the same time.
   A Write begins at the latest transition among $\overline{CE_1}$ going LOW, CE_2 going HIGH and $\overline{WE}$ going LOW.
   A Write ends at the earliest transition among $\overline{CE_1}$ going HIGH, CE_2 going LOW and $\overline{WE}$ going HIGH.
   t_{WP} is measured from the beginning of Write to the end of Write.
4. t_{CW} is measured from the later of $\overline{CE_1}$ going LOW or CE_2 going HIGH to the end of Write.
5. If $\overline{OE}$ or $\overline{CE_1}$ is HIGH, or CE_2 or $\overline{WE}$ is LOW, D_{OUT} goes to a HIGH impedance state.
6. During a write cycle, $\overline{OE}$ = V_{IH} or V_{IL}.
7. D_{OUT} is equal to the Input Data written during the same cycle.
8. Parameter is sampled and not 100% tested.

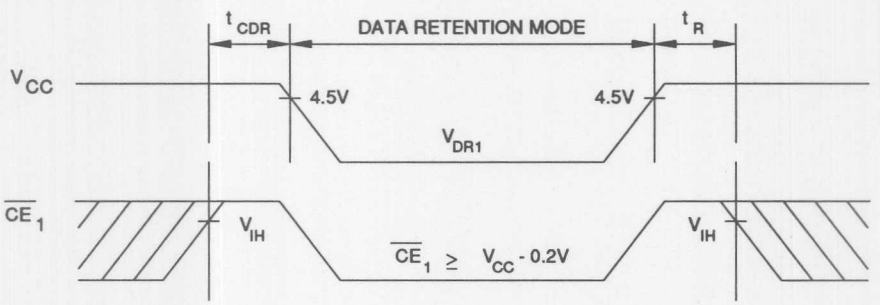
Data Retention Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Data Retention Power Supply Voltage	VDR1	$\overline{CE_1} \geq V_{CC}$ - 0.2 V $CE_2 \geq V_{CC}$ - 0.2 V or $CE_2 \leq 0.2$ V	2.0		5.5	V
	V_{DR2}	$CE_2 \leq 0.2$ V	2.0		5.5	
Data Retention Current	I_{CCDR1}	V_{CC} = 3.0 V $\overline{CE_1} \geq V_{CC}$ - 0.2 V $CE_2 \geq V_{CC}$-0.2 V or $CE_2 \leq 0.2$ V		1	50	µA
	I_{CCDR2}	V_{CC} = 3.0 V, $CE_2 \leq 0.2$ V		1	50	µA
Chip Enable Setup Time	t_{CDR}		0			ns
Chip Enable Hold Time	t_R		t_{RC} (1)			ns

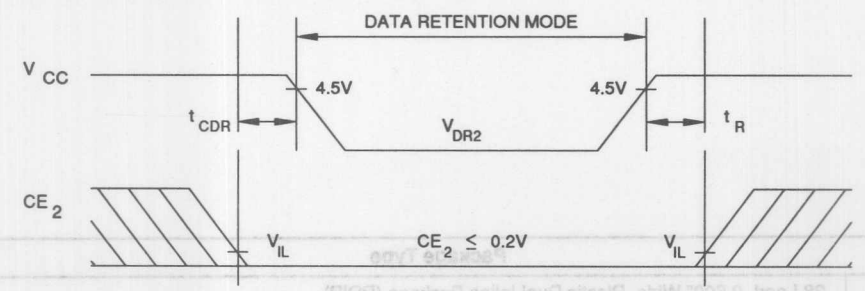
Note: 1. t_{RC} = Read Cycle Time

6

Data Retention Waveform 1 ($\overline{CE}_1$ Control)



Data Retention Waveform 2 (CE_2 Control)



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
100	35	0.1	AT3864L-10PC AT3864L-10RC	28P6 28R	Commercial (0° to 70°C)
			AT3864L-10PI AT3864L-10RI	28P6 28R	Industrial (-40° to 85°C)
120	35	0.1	AT3864L-12PC AT3864L-12RC	28P6 28R	Commercial (0° to 70°C)
			AT3864L-12PI AT3864L-12RI	28P6 28R	Industrial (-40° to 85°C)
150	35	0.1	AT3864L-15PC AT3864L-15RC	28P6 28R	Commercial (0° to 70°C)
			AT3864L-15PI AT3864L-15RI	28P6 28R	Industrial (-40° to 85°C)

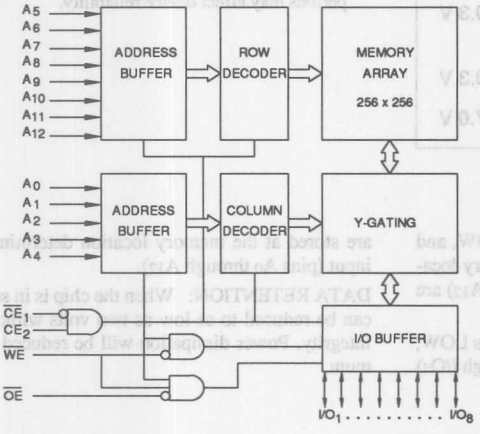
Package Type	
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28R	28 Lead, 0.330" Wide Plastic Gull Wing Small Outline (SOIC)

64K (8K x 8) CMOS SRAM

Features

- **Fast Read Access Time - 150 ns**
- **Low Power**
  - **40 mA Maximum (Active)**
  - **1 mA Maximum (Standby)**
- **2-V Data Retention**
- **Fully Static: No Clock Required**
- **Three Control Inputs ($\overline{CE_1}$, CE_2, and $\overline{OE}$)**
- **TTL Compatible Inputs and Outputs**
- **5 V ± 10% Supply**
- **28-Lead Dual In-line**
- **JEDEC Pinout**
- **Full Military Temperature Range**

Block Diagram



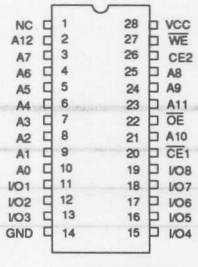
Description

The AT3864L-15DMB is a high performance CMOS static Random Access Memory. Its 64K of memory is organized as 8192 words by 8 bits. Manufactured with an advanced CMOS technology, the AT3864L-15DMB offers access times down to 150 ns with power dissipation of 220 mW maximum. When the AT3864L-15DMB is deselected, the standby current is just 1 mA. In addition, the AT3864L-15DMB offers a data retention capability of only 800 µW power dissipation when operated on a 2 V power supply.

continued on next page

Pin Configurations

Pin Name	Function
A_0-A_{12}	Addresses
I/O_1-I/O_8	Outputs
$\overline{CE_1}$, CE_2	Chip Enables
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}, GND	Power, Ground
NC	No Connect



Description (Continued)

The AT3864L-15DMB powers down to the standby mode when deselected ($\overline{CE_1}$ is HIGH or CE_2 is LOW). The I/O pins remain in the high impedance state unless the chip is selected ($\overline{CE_1}$ is LOW and CE_2 is HIGH), the outputs are enabled ($\overline{OE}$ is LOW), and Write Enable is not active ($\overline{WE}$ is HIGH).

The AT3864L-15DMB is completely TTL compatible and requires a single 5-V power supply. The device is fully static and does not need any clocks or refresh control signals for operation.

Absolute Maximum Ratings*

Temperature Under Bias	-55° C to 150° C
Storage Temperature	-65° C to 150° C
All Input Voltages (including NC Pins) with Respect to Ground	-0.3 V to V_{CC}+0.3 V
All Output Voltages with Respect to Ground	-0.3 V to V_{CC}+0.3 V
Maximum Supply Voltage	+7.0 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: When $\overline{CE_1}$ is LOW, CE_2 is HIGH, $\overline{OE}$ is LOW, and $\overline{WE}$ is HIGH, the eight bits of data stored at the memory location determined by the address input (pins A_0 through A_{12}) are inserted on the data outputs (pins I/O_1 through I/O_8).

WRITE: When $\overline{CE_1}$ is LOW, CE_2 is HIGH, and $\overline{WE}$ is LOW, the eight bits of data placed on the input pins (I/O_1 through I/O_8) are stored at the memory location determined by the address input (pins A_0 through A_{12}).

DATA RETENTION: When the chip is in standby mode, V_{CC} can be reduced to as low as two volts without impacting data integrity. Power dissipation will be reduced to 800 µW maximum.

Operating Modes

MODE\PIN	$\overline{CE_1}$	CE_2	$\overline{OE}$	$\overline{WE}$	I/O
Read	L	H	L	H	D_{OUT}
Write	L	H	X[1]	L	D_{IN}
$Standby_1$	H	X	X	X	High Z
$Standby_2$	X	L	X	X	High Z
Output Disable	X	X	H	X	High Z

Note: 1. X can be L (Low) or H (High)

D.C. and A.C. Operating Range

		AT3864L-15
Operating Temperature (Case)	Military	-55°C - 125°C
V_{CC} Power Supply		5 V ± 10%

D.C. and Operating Characteristics

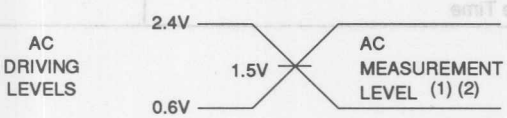
Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0 to V_{CC}	-1.0		1.0	µA
I_{LO}	Output Leakage Current	$\overline{CE_1}$ = 2.2 V to V_{CC} + 0.3 V or CE_2 = -0.3 V to 0.8 V or $\overline{OE}$ = 2.2 V to V_{CC} + 0.3 V or $\overline{WE}$ = -0.3 V to 0.8 V $V_{I/O}$ = 0 to V_{CC}	-1.0		1.0	µA
I_{SB1}	Standby Current (CMOS)	$CE_2 \le 0.2$ V or $\overline{CE_1} \ge V_{CC}$ - 0.2 V, $CE_2 \ge V_{CC}$ - 0.2 V or $CE_2 \le 0.2$ V V_{IN} = 0 to V_{CC}			1	mA
I_{SB2}	Standby Current (TTL)	CE_2 = -0.3 V to 0.8 V or $\overline{CE_1}$ = 2.2 V to V_{CC} +0.3 V, V_{IN} = 0 to V_{CC}			3	mA
I_{CC}	V_{CC} Active Current (TTL)	$\overline{CE_1}$ = -0.3 V to 0. 8V, CE_2 = 2.2 V to V_{CC} + 0.3 V, I_{OUT} = 0 mA, min cycle		20	40	mA
V_{IL}	Input Low Voltage		-0.3		0.8	V
V_{IH}	Input High Voltage		2.2 V		V_{CC}+0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -1.0mA	2.4			V

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0 V		6	10	pF
C_{IN}	Input Capacitance	V_{IN} = 0 V		6	10	pF

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Input Test Waveforms and Measurement Levels



Notes: 1. Input rise and fall time 5 ns.
2. Output load: 1TTL gate + 100 pF.

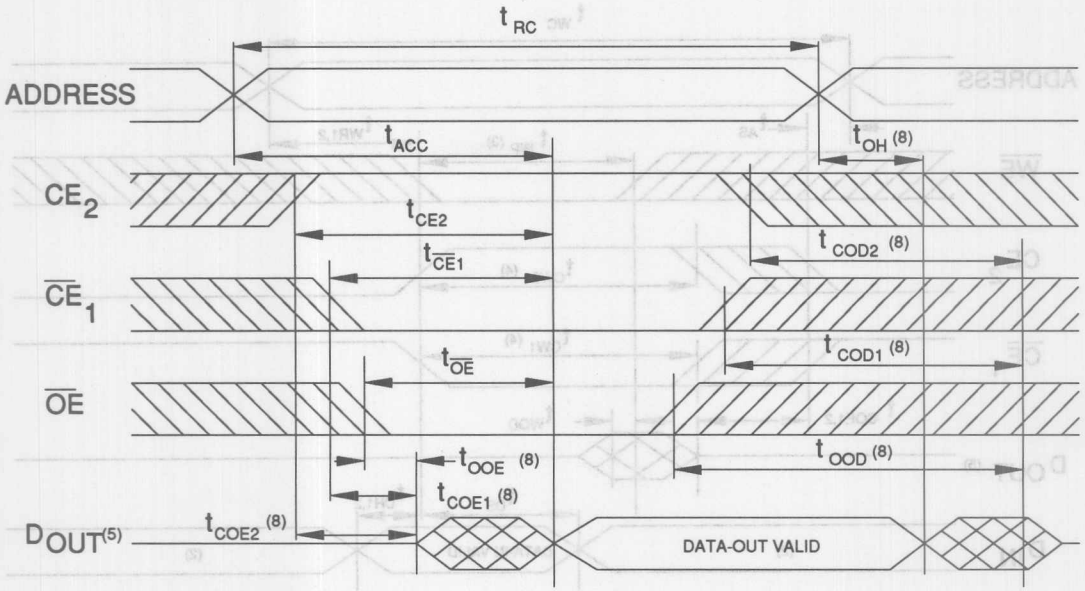
A.C. Characteristics for Read

Symbol	Parameter	AT3864L-15 Min	AT3864L-15 Max	Units
t_{RC}	Read Cycle Time	150		ns
t_{ACC}	Address Access Time		150	ns
$t_{\overline{CE}1}$,t_{CE2}	$\overline{CE}_1$,CE_2 Access Time		150	ns
$t_{\overline{OE}}$	$\overline{OE}$ Access Time		70	ns
t_{OH}	Output Hold Time	15		ns
$t_{COE1,2}$	$\overline{CE}_1$, CE_2 Output Enable Time	10		ns
t_{OOE}	$\overline{OE}$ Output Enable Time	5		ns
$t_{COD1,2}$	$\overline{CE}_1$, CE_2 Output Disable Time		60	ns
t_{OOD}	$\overline{OE}$ Output Disable Time		50	ns

A.C. Characteristics for Write

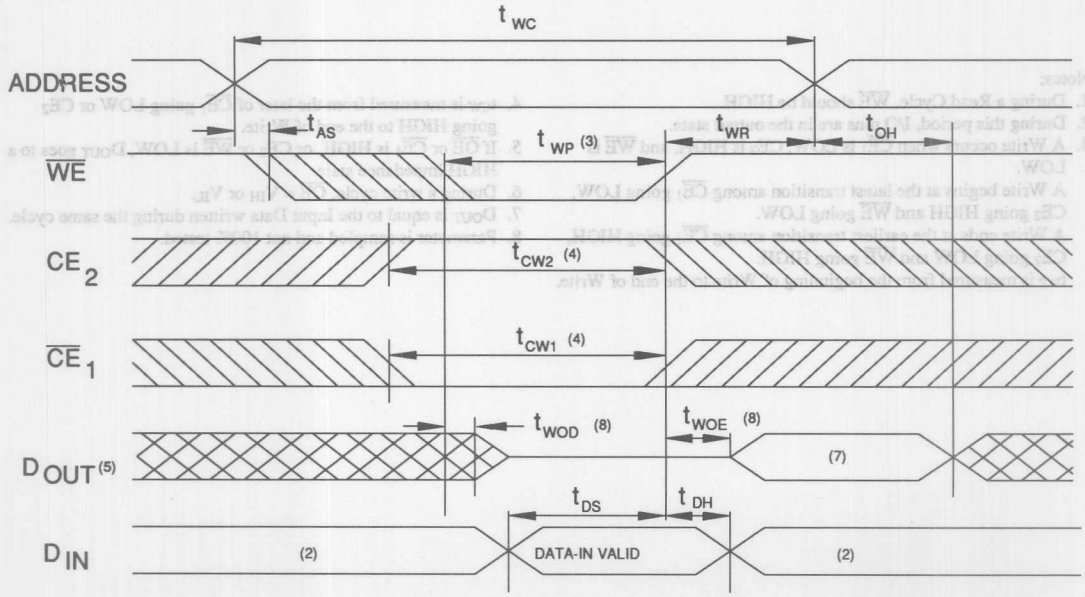
Symbol	Parameter	AT3864L-15 Min	AT3864L-15 Max	Units
t_{WC}	Write Cycle Time	150		ns
t_{AS}	Address Setup Time	0		ns
t_{WP}	Write Pulse Width	90		ns
$t_{CW1,2}$	$\overline{CE}_1$, CE_2 Setup Time	90		ns
t_{WR}	Write Recovery Time	0		ns
$t_{WR1,2}$	$\overline{CE}_1$, CE_2 Write Recovery Time	0		ns
t_{DS}	Data Setup Time	60		ns
t_{DH}	Data Hold Time	0		ns
$t_{DH1,2}$	$\overline{CE}_1$, CE_2 Data Hold Time	0		ns
t_{WOE}	$\overline{WE}$ Output Enable Time	5		ns
t_{WOD}	$\overline{WE}$ Output Disable Time		50	ns

A.C. Waveforms for Read Cycle [1]

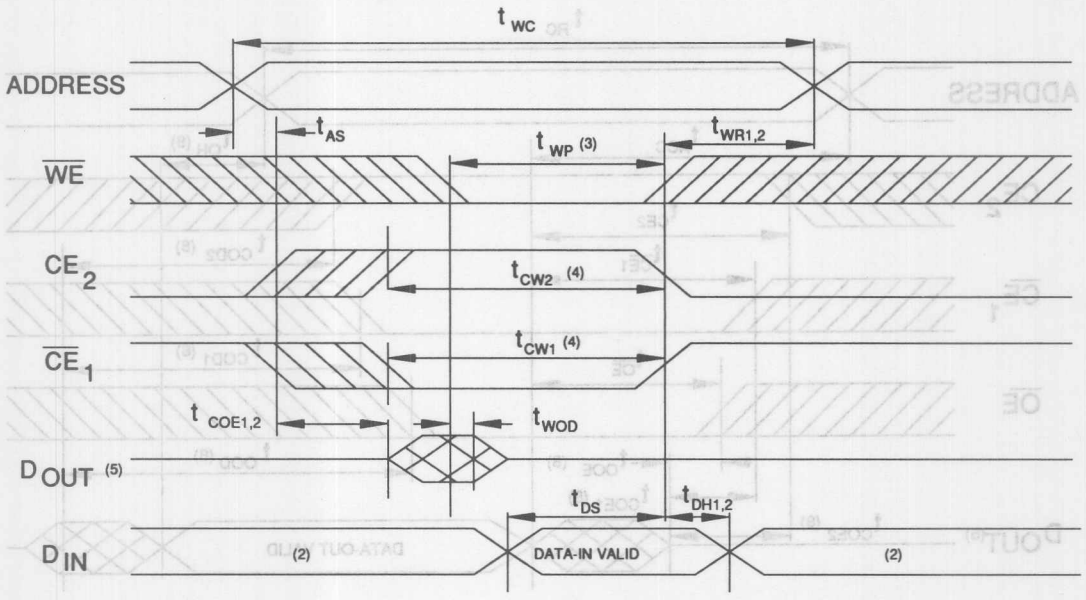


6

A.C. Waveforms for Write Cycle 1 ($\overline{WE}$ Write) [6]



A.C. Waveforms for Write Cycle 2 ($\overline{WE}$ Write) (6)



Notes:
1. During a Read Cycle, $\overline{WE}$ should be HIGH.
2. During this period, I/O pins are in the output state.
3. A Write occurs when $\overline{CE_1}$ is LOW, CE_2 is HIGH, and $\overline{WE}$ is LOW.
   A Write begins at the latest transition among $\overline{CE_1}$ going LOW, CE_2 going HIGH and $\overline{WE}$ going LOW.
   A Write ends at the earliest transition among $\overline{CE_1}$ going HIGH, CE_2 going LOW and $\overline{WE}$ going HIGH.
   t_{WP} is measured from the beginning of Write to the end of Write.
4. t_{CW} is measured from the later of $\overline{CE_1}$ going LOW or CE_2 going HIGH to the end of Write.
5. If $\overline{OE}$ or $\overline{CE_1}$ is HIGH, or CE_2 or $\overline{WE}$ is LOW, D_{OUT} goes to a HIGH impedance state.
6. During a write cycle, $\overline{OE}$ = V_{IH} or V_{IL}.
7. D_{OUT} is equal to the Input Data written during the same cycle.
8. Parameter is sampled and not 100% tested.

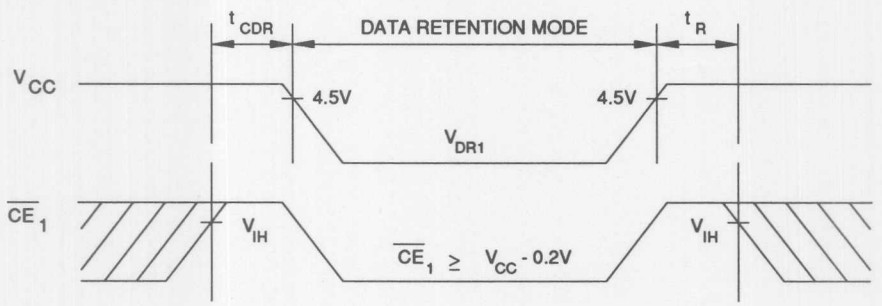
Data Retention Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Data Retention Power Supply Voltage	VDR1	$\overline{CE}_1 \geq V_{CC}$ - 0.2 V $CE_2 \geq V_{CC}$ - 0.2 V or $CE_2 \leq 0.2$ V	2.0		5.5	V
	V_{DR2}	$CE_2 \leq 0.2$ V	2.0		5.5	
Data Retention Current	I_{CCDR1}	V_{CC} = 3.0 V $\overline{CE}_1 \geq V_{CC}$ - 0.2 V $CE_2 \geq V_{CC}$-0.2 V or $CE_2 \leq 0.2$ V		1	400	µA
	I_{CCDR2}	V_{CC} = 3.0 V, $CE_2 \leq 0.2$ V		1	400	µA
Chip Enable Setup Time	t_{CDR}		0			ns
Chip Enable Hold Time	t_R		t_{RC}(1)			ns

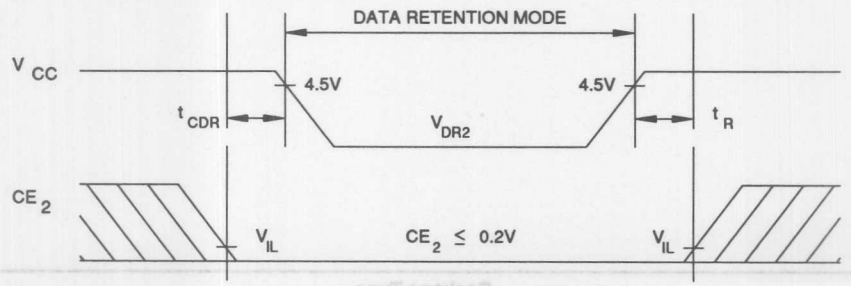
Note: 1. t_{RC} = Read Cycle Time

6

Data Retention Waveform 1 ($\overline{CE}_1$ Control)

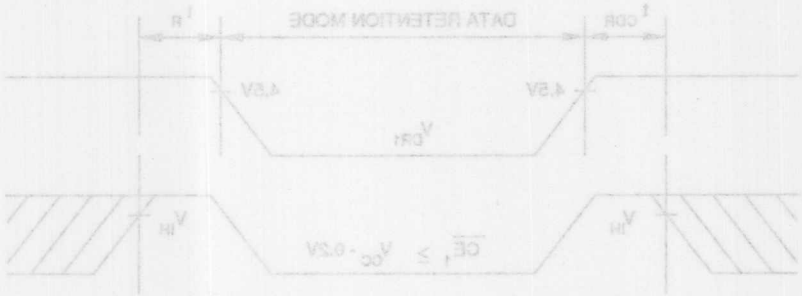


Data Retention Waveform 2 (CE_2 Control)



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	40	1.0	AT3864L-15DMB	28D6	Military (-55° to 125°C)





Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)

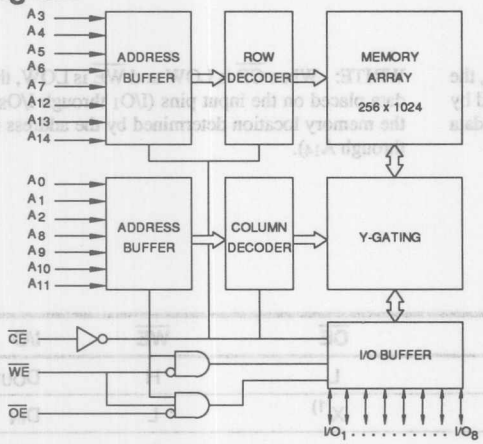
Features

- Fast Read Access Time - 20 ns
- Low Power
  - 100 mA Maximum (Active)
  - 0.1 mA Maximum (Standby)
- Fully Static: No Clock Required
- Two Control Inputs ($\overline{CE}$ and $\overline{OE}$)
- TTL Compatible Inputs and Outputs
- 5 V ± 10% Supply
- 28-Lead Dual In-line and Surface Mount Packages
- JEDEC Pinout
- Commercial and Industrial Temperature Ranges

256K (32K x 8) CMOS SRAM

6

Block Diagram



Description

The AT38H256 is a high performance CMOS static Random Access Memory. Its 256K of memory is organized as 32768 words by eight bits. Manufactured with an advanced CMOS technology, the AT38H256 offers access times down to 20 ns. When the AT38H256 is deselected, the standby current is just 0.1 mA.

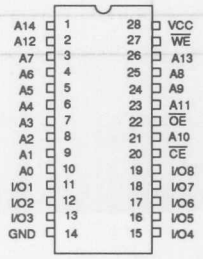
The AT38H256 powers down to the standby mode when deselected ($\overline{CE}$ is HIGH). The I/O pins remain in the high impedance state unless the chip is selected ($\overline{CE}$ is LOW), the outputs are enabled ($\overline{OE}$ is LOW), and Write Enable is not active ($\overline{WE}$ is HIGH).

The AT38H256 is completely TTL compatible and requires a single five-volt power supply. The device is fully static and does not need any clocks or refresh control signals for operation.

Pin Configurations

For .300 DIP/.600 DIP/.300 SOJ

Pin Name	Function
A_0-A_{14}	Addresses
I/O_1-I/O_8	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}, GND	Power, Ground



Absolute Maximum Ratings*

Temperature Under Bias	-55° C to 125° C
Storage Temperature	-65° C to 150° C
All Input Voltages (including NC Pins) with Respect to Ground	-0.3 V[(1)] to V_{CC} + 0.3 V
All Output Voltages with Respect to Ground	-0.3 V[(1)] to V_{CC} + 0.3 V
Maximum Supply Voltage	+7.0 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
1. Minimum input voltages are -3.5 V for pulse width less than 20 ns.

Device Operation

READ: When $\overline{CE}$ is LOW, $\overline{OE}$ is LOW, and $\overline{WE}$ is HIGH, the eight bits of data stored at the memory location determined by the address input (pins A_0 through A_{14}) are inserted on the data outputs (pins I/O_1 through I/O_8).

WRITE: When $\overline{CE}$ is LOW and $\overline{WE}$ is LOW, the eight bits of data placed on the input pins (I/O_1 through I/O_8) are stored at the memory location determined by the address input (pins A_0 through A_{14}).

Operating Modes

MODE\PIN	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	L	L	H	D_{OUT}
Write	L	X[(1)]	L	D_{IN}
Standby (Not Selected)	H	X	X	High Z
Output Disable (High Impedance)	X	H	X	High Z

Note: 1. X can be L (Low) or H (High)

D.C. and A.C. Operating Range

		AT38H256
Operating Temperature (Ambient)	Commercial	0°C - 70°C
	Industrial	-40°C - 85°C
V_{CC} Power Supply		5 V ± 10%

D.C. and Operating Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0 to V_{CC}				2	µA
I_{LO}	Output Leakage Current	$\overline{CE}$ = 2.2 V to V_{CC} + 0.3 V or $\overline{OE}$ = 2.2 V to V_{CC} + 0.3 V or $\overline{WE}$ = -0.3 V to 0.8 V $V_{I/O}$ = 0 to V_{CC}				2	µA
I_{SB1}	Standby Current (CMOS)	$\overline{CE} \geq V_{CC}$ - 0.2 V, $V_{IN} = (V_{CC} - 0.2\ V)$ or ≤ 0.2 V	Com.			0.1	mA
			Ind.			1.0	mA
I_{SB2}	Standby Current (TTL)	$\overline{CE}$ = 2.2 V to V_{CC} +0.3 V, $V_{IN} = V_{IL}$ or V_{IH}				25	mA
I_{CC}	V_{CC} Active Current (TTL)	$\overline{CE}$ = -0.3 V to 0.8 V, I_{OUT} = 0 mA, min cycle				100	mA
V_{IL} (1)	Input Low Voltage			-0.3 (2)		0.8	V
V_{IH} (1)	Input High Voltage			2.2 V		V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA				0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4.0 mA		2.4			V

Note: 1. These are voltages with repect to device GND.
2. V_{IL} = -3.0 V for pulse width less than 20 ns.

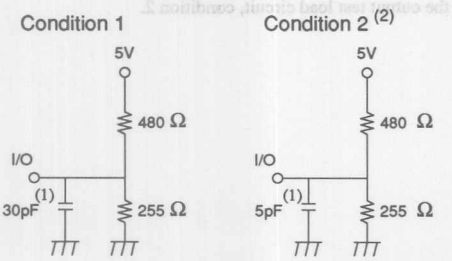
Pin Capacitance (f = 1 MHz, T = 25°C) (1)

Symbol	Parameter	Conditions	Min	Max	Units
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0 V		10	pF
C_{IN}	Input Capacitance	V_{IN} = 0 V		10	pF

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Output Test Load

Figure 1



Item	Condition
Input pulse "High" level	V_{IH} = 3.0 V
Input pulse "Low" level	V_{IL} = 0 V
Input rise time	t_R = 5 ns
Input fall time	t_F = 5 ns
Input and output reference level	1.5 V
Output load	See Figure 1

Notes: 1. Capacitance Load includes scope and jig capacitances.
2. For t_{COE}, t_{OOE}, t_{COD}, t_{OOD}, t_{WOE}, t_{WOD}.

6

A.C. Characteristics for Read

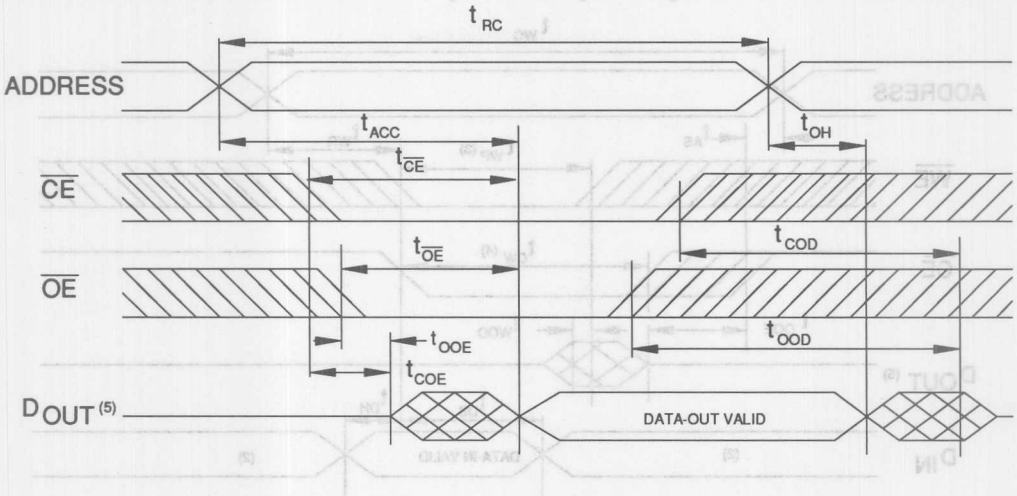
Symbol	Parameter	AT38H256-20		AT38H256-25		AT38H256-35		Units
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	20		25		35		ns
t_{ACC}	Address Access Time		20		25		35	ns
$t_{\overline{CE}}$	$\overline{CE}$ Access Time		20		25		35	ns
$t_{\overline{OE}}$	$\overline{OE}$ Access Time		12		12		20	ns
t_{OH}	Output Hold Time	5		5		5		ns
t_{COE} (1)	$\overline{CE}$ Output Enable Time	5		5		5		ns
t_{OOE} (1)	$\overline{OE}$ Output Enable Time	0		0		0		ns
t_{COD} (1)	$\overline{CE}$ Output Disable Time		10		10		15	ns
t_{OOD} (1)	$\overline{OE}$ Output Disable Time		13		13		15	ns

A.C. Characteristics for Write

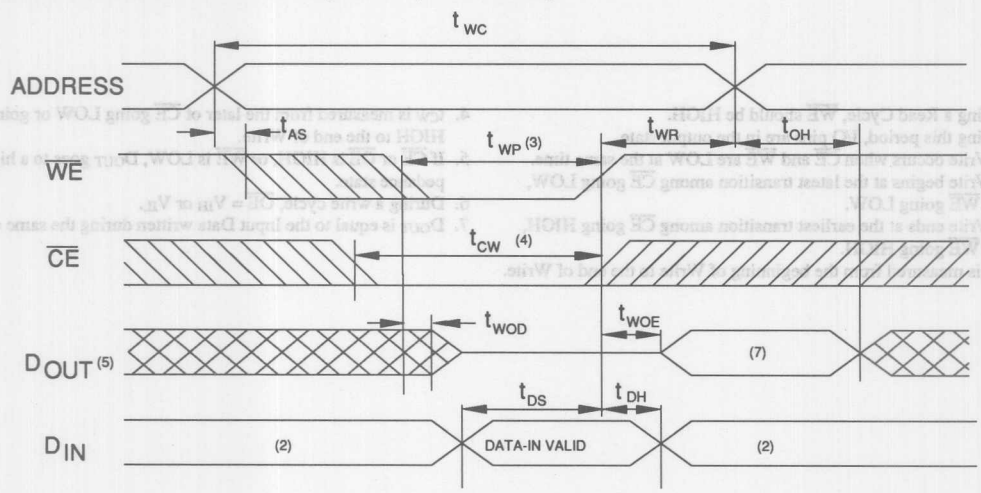
Symbol	Parameter	AT38H256-20		AT38H256-25		AT38H256-35		Units
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	20		25		35		ns
t_{AS}	Address Setup Time	0		0		0		ns
t_{WP}	Write Pulse Width	15		20		30		ns
t_{CW}	$\overline{CE}$ Setup Time	15		20		30		ns
t_{WR}	Write Recovery Time	2		2		2		ns
t_{DS}	Data Setup Time	12		12		15		ns
t_{DH}	Data Hold Time	0		0		0		ns
t_{WOE} (1)	$\overline{WE}$ Output Enable Time	0		0		0		ns
t_{WOD} (1)	$\overline{WE}$ Output Disable Time		8		13		15	ns

Note: 1. Transition is measured by ±500 mV from the normal state with the output test load circuit, condition 2. This parameter is sampled and is not 100% tested.

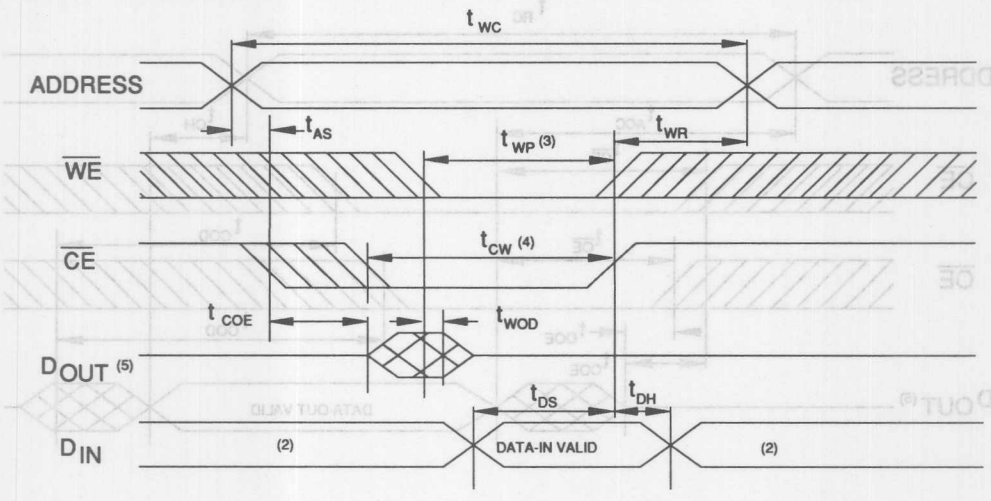
A.C. Waveforms for Read Cycle [1]



A.C. Waveforms for Write Cycle 1 ($\overline{WE}$ Write) [6]



A.C. Waveforms for Write Cycle 2 ($\overline{WE}$ Write) [6]



Notes:
1. During a Read Cycle, $\overline{WE}$ should be HIGH.
2. During this period, I/O pins are in the output state.
3. A Write occurs when $\overline{CE}$ and $\overline{WE}$ are LOW at the same time.
   A Write begins at the latest transition among $\overline{CE}$ going LOW, and $\overline{WE}$ going LOW.
   A Write ends at the earliest transition among $\overline{CE}$ going HIGH, and $\overline{WE}$ going HIGH.
   t_{WP} is measured from the beginning of Write to the end of Write.
4. t_{CW} is measured from the later of $\overline{CE}$ going LOW or going HIGH to the end of Write.
5. If $\overline{CE}$ or $\overline{OE}$ is HIGH, or $\overline{WE}$ is LOW, D_{OUT} goes to a high impedance state.
6. During a write cycle, $\overline{OE}$ = V_{IH} or V_{IL}.
7. D_{OUT} is equal to the Input Data written during the same cycle.

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
20	100	0.1	AT38H256-20NC AT38H256-20XC	28P3 28S2	Commercial (0° to 70°C)
20	100	1.0	AT38H256-20NI AT38H256-20XI	28P3 28S2	Industrial (-40° to 85°C)
25	100	0.1	AT38H256-25NC AT38H256-25XC	28P3 28S2	Commercial (0° to 70°C)
25	100	1.0	AT38H256-25NI AT38H256-25XI	28P3 28S2	Industrial (-40° to 85°C)
35	100	0.1	AT38H256-35NC AT38H256-35XC	28P3 28S2	Commercial (0° to 70°C)
35	100	1.0	AT38H256-35NI AT38H256-35XI	28P3 28S2	Industrial (-40° to 85°C)

Package Type	
28P3	28 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
28S2	28 Lead, 0.300" Wide, Plastic J-Leaded Small Outline (SOJ)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
20	100	0.1	AT38H256-20MC AT38H256-20XC	28P3 28S2	Commercial (0° to 70°C)
20	100	1.0	AT38H256-20MI AT38H256-20XI	28P3 28S2	Industrial (-40° to 85°C)
25	100	0.1	AT38H256-25MC AT38H256-25XC	28P3 28S2	Commercial (0° to 70°C)
25	100	1.0	AT38H256-25MI AT38H256-25XI	28P3 28S2	Industrial (-40° to 85°C)
35	100	0.1	AT38H256-35MC AT38H256-35XC	28P3 28S2	Commercial (0° to 70°C)
35	100	1.0	AT38H256-35MI AT38H256-35XI	28P3 28S2	Industrial (-40° to 85°C)

Package Type	
28P3	28 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
28S2	28 Lead, 0.300" Wide, Plastic J-Leaded Small Outline (SOJ)

Features

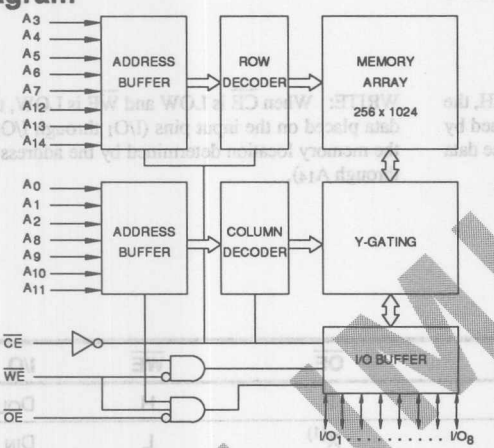
- **Low Power**
  - **25 mA Maximum (Active)**
  - **30 µA Maximum (Standby)**
- **3.3 V ± 10% Supply**
- **Fully Static: No Clock Required**
- **Two Control Inputs ($\overline{CE}$ and $\overline{OE}$)**
- **TTL Compatible Inputs and Outputs**
- **28-Pin SOIC Surface Mount Packages**
- **JEDEC Pinout**

256K (32K x 8) Low Voltage CMOS SRAM

Preliminary

6

Block Diagram



Description

The AT38LV256 is a high performance CMOS static Random Access Memory. Its 256K of memory is organized as 32768 words by eight bits. Manufactured with an advanced CMOS technology, the AT38LV256 offers access times down to 70 ns. When the AT38LV256 is deselected, the standby current is just 30 µA.

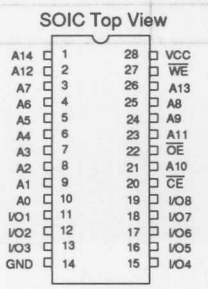
The AT38LV256 powers down to the standby mode when deselected ($\overline{CE}$ is HIGH). The I/O pins remain in the high impedance state unless the chip is selected ($\overline{CE}$ is LOW), the outputs are enabled ($\overline{OE}$ is LOW), and Write Enable is not active ($\overline{WE}$ is HIGH).

The AT38LV256 is completely TTL compatible and requires a single 3.3-volt power supply. The device is fully static and does not need any clocks or refresh control signals for operation.

Pin Configurations

Pin Name	Function
A_0-A_{14}	Addresses
I/O_1-I/O_8	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}, GND	Power, Ground

SOIC Top View



PRELIMINARY

Absolute Maximum Ratings*

Temperature Under Bias	-55° C to 125° C
Storage Temperature	-65° C to 150° C
All Input Voltages (including NC Pins) with Respect to Ground	-0.3 V[(1)] to V_{CC} + 0.3 V
All Output Voltages with Respect to Ground	-0.3 V[(1)] to V_{CC} + 0.3 V
Maximum Supply Voltage	+7.0 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
1. Minimum input voltages are -3.5 V for pulse width less than 20 ns.

Device Operation

READ: When $\overline{CE}$ is LOW, $\overline{OE}$ is LOW, and $\overline{WE}$ is HIGH, the eight bits of data stored at the memory location determined by the address input (pins A_0 through A_{14}) are inserted on the data outputs (pins I/O_1 through I/O_8).

WRITE: When $\overline{CE}$ is LOW and $\overline{WE}$ is LOW, the eight bits of data placed on the input pins (I/O_1 through I/O_8) are stored at the memory location determined by the address input (pins A_0 through A_{14}).

Operating Modes

MODE\PIN	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	L	L	H	D_{OUT}
Write	L	X[(1)]	L	D_{IN}
Standby (Not Selected)	H	X	X	High Z
Output Disable (High Impedance)	X	H	X	High Z

Note: 1. X can be L (Low) or H (High)

D.C. and A.C. Operating Range

		AT38LV256
Operating Temperature (Ambient)	Commercial	0°C - 70°C
V_{CC} Power Supply		3.3 V ± 10%

D.C. and Operating Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0 to V_{CC}			2	µA
I_{LO}	Output Leakage Current	$\overline{CE}$ = 2.2 V to V_{CC} + 0.3 V or $\overline{OE}$ = 2.2 V to V_{CC} + 0.3 V or $\overline{WE}$ = -0.3 V to 0.8 V $V_{I/O}$ = 0 to V_{CC}			30	µA
I_{SB1}	Standby Current (CMOS)	$\overline{CE} \geq V_{CC}$ - 0.2 V, $V_{IN} = (V_{CC} - 0.2\ V)$ or ≤ 0.2 V			30	µA
I_{SB2}	Standby Current (TTL)	$\overline{CE}$ = 2.2 V to V_{CC} +0.3 V, $V_{IN} = V_{IL}$ or V_{IH}			2.5	mA
I_{CC}	V_{CC} Active Current (TTL)	$\overline{CE}$ = -0.3 V to 0.5 V, I_{OUT} = 0 mA, min cycle			25	mA
V_{IL} (1)	Input Low Voltage		-0.3(2)		0.5	V
V_{IH} (1)	Input High Voltage		2.2 V		V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 1.0 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -0.5 mA	2.4			V

Note: 1. These are voltages with repect to device GND.
2. V_{IL} = -3.0 V for pulse width less than 20 ns.

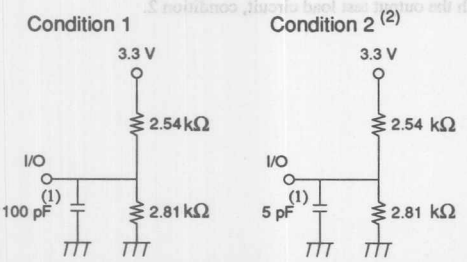
Pin Capacitance (f = 1 MHz, T = 25°C) (1)

Symbol	Parameter	Conditions	Min	Max	Units
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0 V		10	pF
C_{IN}	Input Capacitance	V_{IN} = 0 V		10	pF

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Output Test Load

Figure 1



Item	Condition
Input pulse "High" level	V_{IH} = 3.0 V
Input pulse "Low" level	V_{IL} = 0 V
Input rise time	t_R = 5 ns
Input fall time	t_F = 5 ns
Input and output reference level	1.5 V
Output load	See Figure 1

Notes: 1. Capacitance Load includes scope and jig capacitances.
2. For t_{COE}, t_{OOE}, t_{COD}, t_{OOD}, t_{WOE}, t_{WOD}.

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A.C. Characteristics for Read

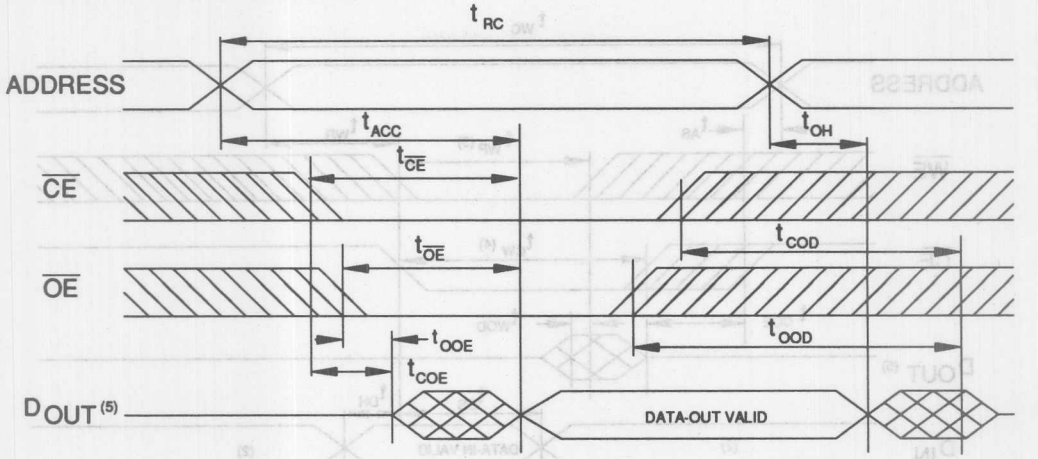
Symbol	Parameter	AT38LV256-70		AT38LV256-12		Units
		Min	Max	Min	Max	
t_{RC}	Read Cycle Time	70		120		ns
t_{ACC}	Address Access Time		70		120	ns
$t_{\overline{CE}}$	$\overline{CE}$ Access Time		70		120	ns
$t_{\overline{OE}}$	$\overline{OE}$ Access Time		35		60	ns
t_{OH}	Output Hold Time	10		10		ns
t_{COE} (1)	$\overline{CE}$ Output Enable Time	10		10		ns
t_{OOE} (1)	$\overline{OE}$ Output Enable Time	5		5		ns
t_{COD} (1)	$\overline{CE}$ Output Disable Time		30		40	ns
t_{OOD} (1)	$\overline{OE}$ Output Disable Time		30		40	ns

A.C. Characteristics for Write

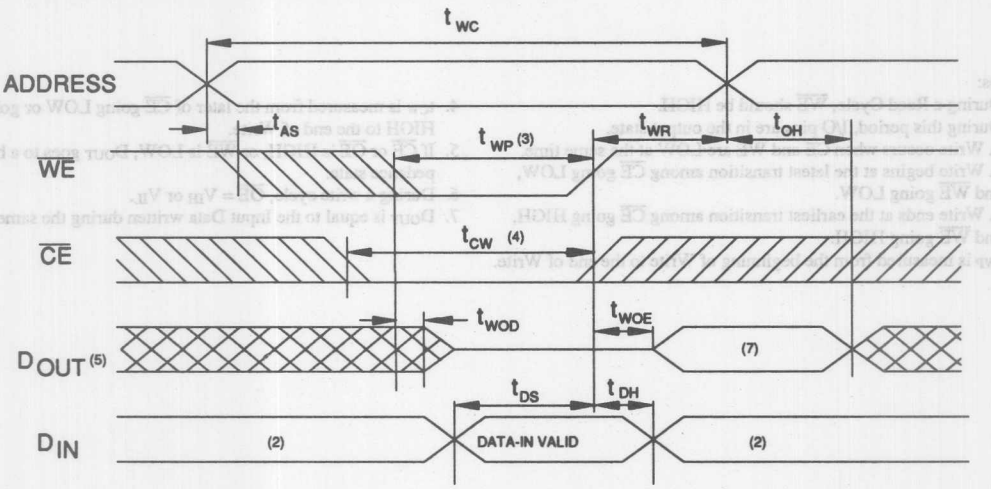
Symbol	Parameter	AT38LV256-70		AT38LV256-12		Units
		Min	Max	Min	Max	
t_{WC}	Write Cycle Time	70		120		ns
t_{AS}	Address Setup Time	0		0		ns
t_{WP}	Write Pulse Width	45		100		ns
t_{CW}	$\overline{CE}$ Setup Time	70		110		ns
t_{WR}	Write Recovery Time	5		5		ns
t_{DS}	Data Setup Time	30		70		ns
t_{DH}	Data Hold Time	0		0		ns
t_{WOE} (1)	$\overline{WE}$ Output Enable Time	10		10		ns
t_{WOD} (1)	$\overline{WE}$ Output Disable Time		30		40	ns

Note: 1. Transition is measured by ±500 mV from the normal state with the output test load circuit, condition 2. This parameter is sampled and is not 100% tested.

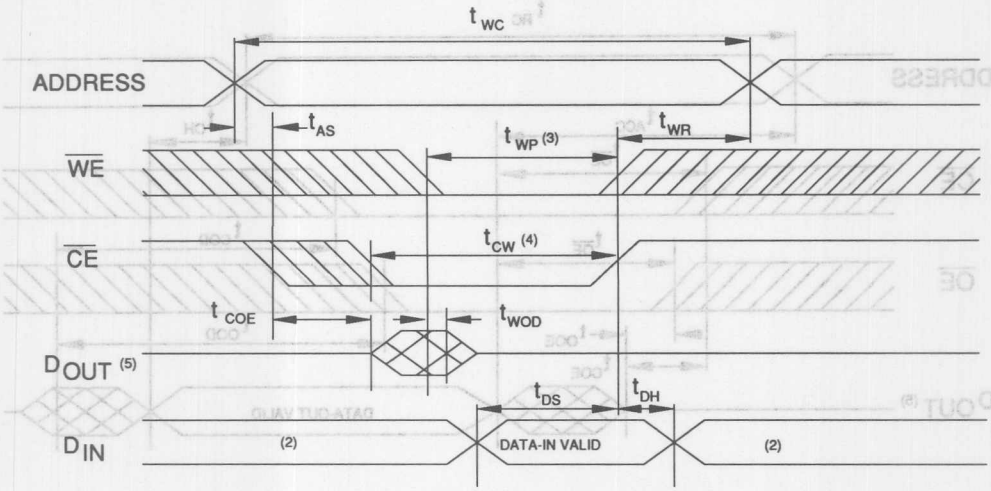
A.C. Waveforms for Read Cycle [1]



A.C. Waveforms for Write Cycle 1 ($\overline{WE}$ Write) [6]



A.C. Waveforms for Write Cycle 2 ($\overline{WE}$ Write) [6]



Notes:
1. During a Read Cycle, $\overline{WE}$ should be HIGH.
2. During this period, I/O pins are in the output state.
3. A Write occurs when $\overline{CE}$ and $\overline{WE}$ are LOW at the same time.
   A Write begins at the latest transition among $\overline{CE}$ going LOW, and $\overline{WE}$ going LOW.
   A Write ends at the earliest transition among $\overline{CE}$ going HIGH, and $\overline{WE}$ going HIGH.
   t_{WP} is measured from the beginning of Write to the end of Write.
4. t_{CW} is measured from the later of $\overline{CE}$ going LOW or going HIGH to the end of Write.
5. If $\overline{CE}$ or $\overline{OE}$ is HIGH, or $\overline{WE}$ is LOW, D_{OUT} goes to a high impedance state.
6. During a write cycle, $\overline{OE}$ = V_{IH} or V_{IL}.
7. D_{OUT} is equal to the Input Data written during the same cycle.

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	25	0.03	AT38LV256-70RC	28R	Commercial (0° to 70°C)
120	25	0.03	AT38LV256-12RC	28R	Commercial (0° to 70°C)

Package Type	
28R	28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline (SOIC)

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	25	0.03	AT28LV256-70RC	28R	Commercial (0° to 70°C)
120	25	0.03	AT28LV256-12RC	28R	Commercial (0° to 70°C)

Package Type	
28R	28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline (SOIC)

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ATMEL

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CMOS EPLDs

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Features

- 20-pin Universal EPLD
- Virtually Zero Standby Power
- Functional Replacement for Common 20-Pin Programmable Devices
  - I_{OL} = 24 mA
- High Performance CMOS EPROM Cell Technology
  - Erasable
  - Reconfigurable
  - 100% Testable
- 25 ns and 35 ns Max Propagation Delay (Commercial)
- 30 ns and 40 ns Max Propagation Delay (Industrial)
- Up to 18 Inputs and 8 Input/Output Macrocells
- Programmable Output Polarity
- Power-Up Reset on all Registers
- Register Preload Capability
- Synchronous Preset/Asynchronous Reset
- Security Fuse to Protect Duplication of Proprietary Designs
- Design Support Provided using many Popular Software Development Packages for PLDs
- Available in 300-mil-wide DIP with Quartz Window, Plastic DIP (OTP), or PLCC (OTP)
- Second Source to Signetic's PLC18V8Z/I

Zero-Standby Power 20-Pin EPLD

7

Description

The AT18V8Z is a universal EPLD featuring high performance and virtually zero-standby power for power-sensitive applications. It is a reliable, user-configurable substitute for discrete TTL/CMOS logic. While compatible with TTL and HCT logic, the AT18V8Z can also replace HC logic over the V_{CC} range of 4.5 to 5.5 V.

The AT18V8Z is a two-level logic element comprised of ten inputs, 74 AND gates (product terms), and eight output Macrocells.

Each output features an "Output Macrocell" which can be individually configured as a dedicated input, a combinatorial output, or a registered output with internal feedback. As a result, the AT18V8Z is capable of emulating all common 20-pin programmable logic devices to reduce documentation, inventory, and manufacturing costs.

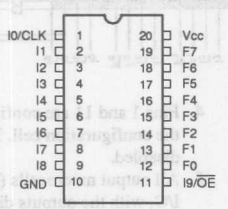
A power-up reset function and a Register Preload function have been incorporated into the AT18V8Z architecture to facilitate state machine design and testing.

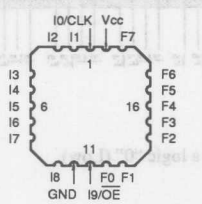
With a standby current of less than 100 µA and active power consumption of 1.5 mA/MHz, the AT18V8Z is ideally suited for power-sensitive applications in battery-operated/backed portable instruments and computers.

The AT18V8Z is also processed to industrial requirements for operation over an extended temperature range of -40°C to +85°C and supply voltage of 4.5 V to 5.5 V.

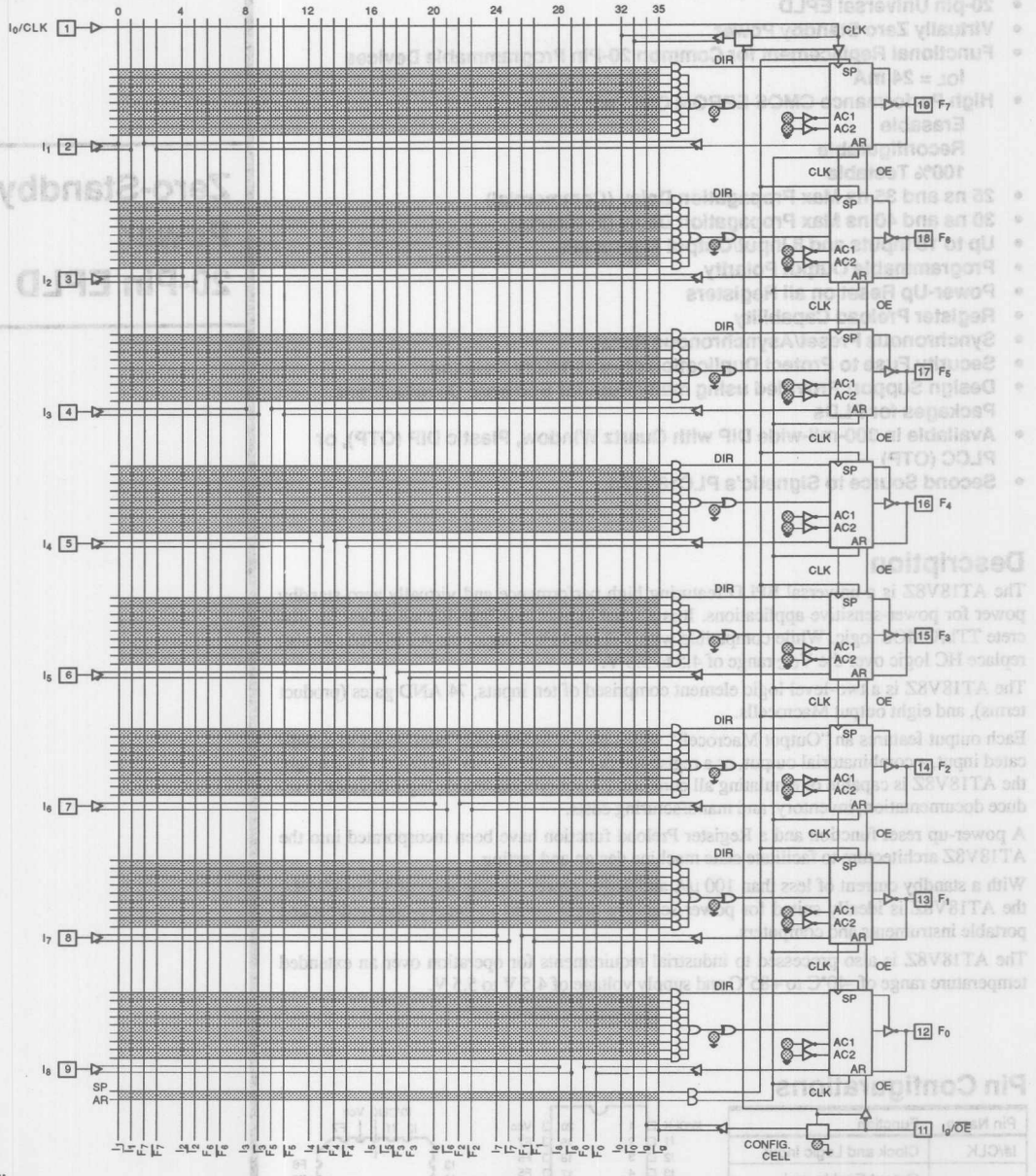
Pin Configurations

Pin Name	Function
I#/CLK	Clock and Logic Input
I#/OE	Output Enable and Logic Input
I#	Logic Inputs
F#	Bidirectional Buffers
*	No Internal Connection
Vcc	+5 V Supply





Logic Diagram



Notes:

In the unprogrammed or virgin state:

1. All cells are in a conductive state.
2. All AND gate locations are pulled to a logic "0" (Low).
3. Output polarity is inverting.

Denotes a programmable cell location.

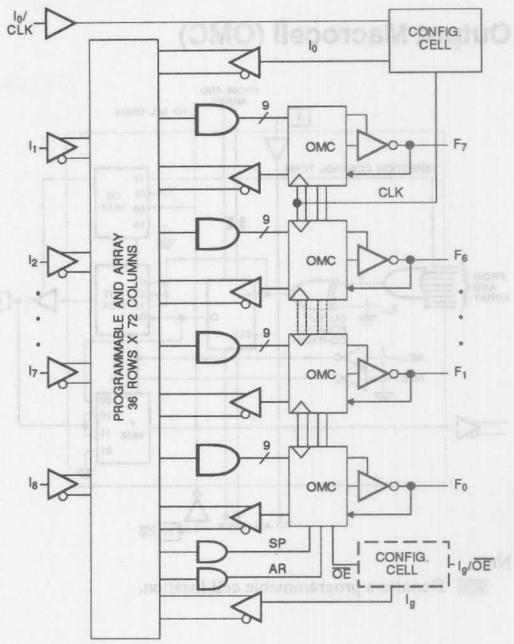
4. Pins 1 and 11 are configured as Inputs 0 and 9, respectively, via the configuration cell. The clock and $\overline{OE}$ functions are disabled.
5. All output macrocells (OMCs) are configured as bidirectional I/O, with the outputs disabled via the direction term.

Absolute Maximum Ratings*

Operating Temperature (Commercial)	0°C to +75°C
Operating Temperature (Industrial)	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Supply Voltage	-0.5 to +7 V_{DC}
Operating Supply Voltage (Commercial)	4.75 to 5.25 V_{DC}
Operating Supply Voltage (Industrial)	4.5 to 5.5 V_{DC}
Input Voltages (including N.C. Pins) with Respect to Ground	-0.5 V to V_{CC}+0.5 V_{DC}
Output Voltages with Respect to Ground-	0.5 V to V_{CC}+0.5 V_{DC}
Input Currents	-10 to +10 mA
Output Currents	+24 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Functional Diagram



7

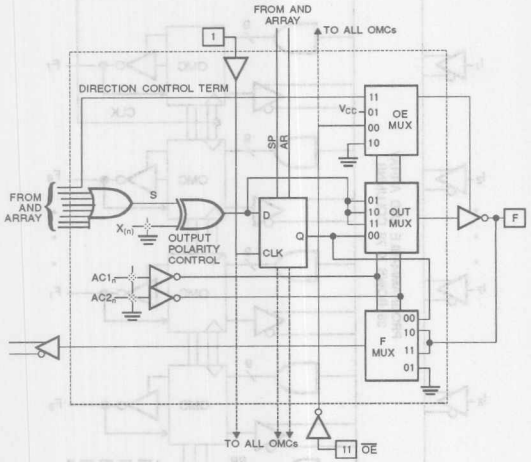
PAL Device to AT18V8Z Output Pin Configuration Cross Reference

PIN NO.	AT18V8Z	16L8 16H8 16P8 16P8	16R4 16RP4	16R6 16RP6	16R8 16RP8	16L2 16H2 16P2	14L4 14H4 14P4	12L6 12H6 12P6	10L8 10H8 10P8
1	I_0/CLK	I	CLK	CLK	CLK	I	I	I	I
19	F7	B	B	B	D	I	I	I	O
18	F6	B	B	D	D	I	I	O	O
17	F5	B	D	D	D	I	O	O	O
16	F4	B	D	D	D	O	O	O	O
15	F3	B	D	D	D	O	O	O	O
14	F2	B	D	D	D	I	O	O	O
13	F1	B	B	D	D	I	I	O	O
12	F0	B	B	B	D	I	I	I	O
11	$I_9/\overline{OE}$	I	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	I	I	I	I

The Atmel state-of-the-art floating-gate CMOS EPROM process yields bipolar equivalent performance at less than one-quarter the power consumption. The erasable nature of the EPROM process enables Atmel to functionally test the devices prior to shipment to the customer. Additionally, this allows Atmel to extensively stress test, as well as ensure the threshold voltage of each individual EPROM cell. 100% programming yield is subsequently guaranteed.

PAL may be a registered trademark of AMD Corp.

Output Macrocell (OMC)



Note:
▒ Denotes a programmable cell location.

Configuration Cell

A single configuration cell controls the functions of Pins 1 and 11. Refer to Functional Diagram. When the configuration cell is programmed, Pin 1 is a dedicated clock and Pin 11 is dedicated for output enable. When the configuration cell is unprogrammed, Pins 1 and 11 are both dedicated inputs. Note that the output enable for all registered OMCs is common—from Pin 11 only. Output enable control of the bidirectional I/O OMCs is provided from the AND array via the direction product term.

If any one OMC is configured as registered, the configuration cell will be automatically configured (via the design software) to ensure that the clock and output enable functions are enabled on Pins 1 and 11, respectively. If none of the OMCs are registered, the configuration cell will be programmed such that Pins 1 and 11 are dedicated inputs. The programming codes are as follows:

Pin 1 = CLK, Pin 11 = $\overline{OE}$	L
Pin 1 and Pin 11 = Input	H

The Output Macrocell (OMC)

The AT18V8Z series devices have eight individually programmable Output Macrocells. The 72 AND inputs (or product terms) from the programmable AND array are connected to the eight OMCs in groups of nine. Eight of the AND terms are dedicated to logic functions; the ninth is for asynchronous direction control, which enables/disables the respective bidirectional I/O pin. Two product terms are dedicated for the Synchronous Preset and Asynchronous Reset functions.

Each OMC can be independently programmed via 16 architecture control bits, $AC1_n$ and $AC2_n$ (one pair per macrocell). Similarly, each OMC has a programmable output polarity control bit (X_n). By configuring the pair of architecture control bits according to the configuration cell table, four different configurations may be implemented. Note that the configuration cell is automatically programmed based on the OMC configuration.

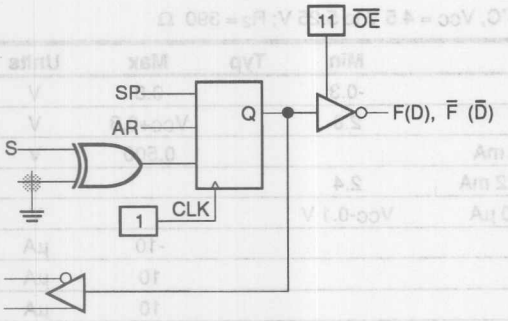
Design Security

The AT18V8Z series devices have a programmable security fuse that controls the access to the data programmed in the device.

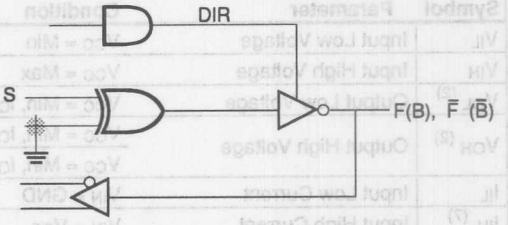
Function	Control Cell Configurations			Comments
	$AC1_n$	$AC2_n$	Config. Cell	
Registered Mode	Programmed	Programmed	Programmed	Dedicated clock from Pin 1. $\overline{OE}$ control for all registered OMCs from Pin 11 only.
Bidirectional I/O mode[1]	Unprogrammed	Unprogrammed	Unprogrammed	Pins 1 and 11 are dedicated inputs. 3-State control from AND array only.
Fixed input mode	Unprogrammed	Programmed	Unprogrammed	Pins 1 and 11 are dedicated inputs.
Fixed output mode	Programmed	Unprogrammed	Unprogrammed	Pins 1 and 11 are dedicated inputs. The feedback path (via F_{MUX}) is disabled.

Note:
1. This is the virgin state as shipped by the factory.

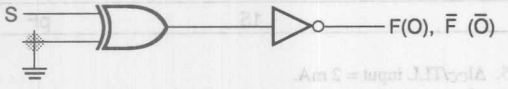
Architecture Control: AC1 and AC2



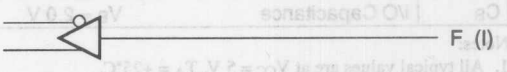
OMC Configuration	Code
Registered (D-type)	D



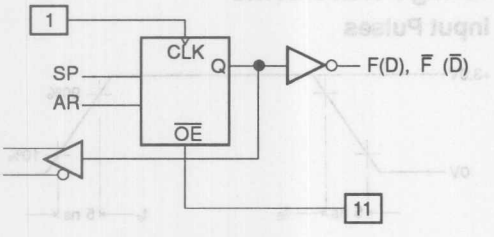
OMC Configuration	Code
Bidirectional I/O[1] (Combinatorial)	B



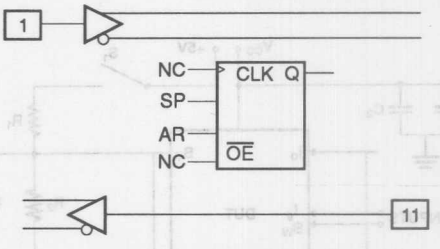
OMC Configuration	Code
Fixed Output	O



OMC Configuration	Code
Fixed Input	I



OMC Configuration	Code
Pin 1 = CLK Pin 11 = OE	L



OMC Configuration	Code
Pin 1 = Input Pin 11 = Input	H[6]

Notes:

A factory shipped unprogrammed device is configured such that:

1. This is the initial unprogrammed state. All cells are in a conductive state.
2. All AND gates are pulled to a logic "O" (Low).
3. Output polarity is inverting.
4. Pins 1 and 11 are configured as inputs 0 and 9. The clock and $\overline{OE}$ functions are disabled.
5. All Output Macrocells (OMCs) are configured as bidirectional I/O, with the outputs disabled via the direction term.
6. This configuration cannot be used if any OMCs are configured as registered (Code = D). The configuration cell will be automatically configured to ensure that the clock and output enable functions are enabled on Pins 1 and 11, respectively, if any one OMC is programmed as registered.

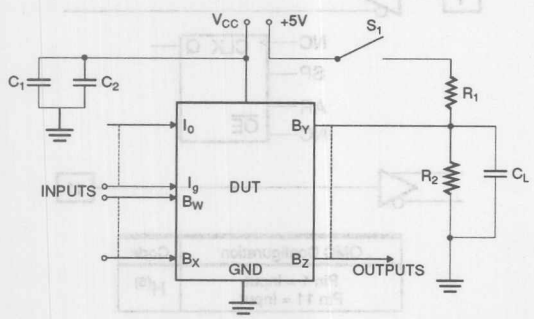
D.C. Characteristics

T_{AC} = 0°C to +75°C, V_{CC} = 4.75 V to 5.25 V; T_{AI} = -40°C to 85°C, V_{CC} = 4.5 V to 5.25 V; R_2 = 390 Ω

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IL}	Input Low Voltage	V_{CC} = Min	-0.3		0.8	V
V_{IH}	Input High Voltage	V_{CC} = Max	2.0		V_{CC}+0.3	V
V_{OL} (2)	Output Low Voltage	V_{CC} = Min, I_{OL} = 24 mA			0.500	V
V_{OH} (2)	Output High Voltage	V_{CC} = Min, I_{OH} = -3.2 mA	2.4			V
		V_{CC} = Min, I_{OH} = -20 µA	V_{CC}-0.1 V			V
I_{IL}	Input Low Current	V_{IN} = GND			-10	µA
I_{IH} (7)	Input High Current	V_{IN} = V_{CC}			10	µA
$I_{O(OFF)}$	Hi-Z State Output Current	V_{OUT} = V_{CC}			10	µA
		V_{OUT} = GND			-10	µA
I_{OS} (3)	Short Circuit Output Current	V_{OUT} = GND			-130	mA
I_{CC}	V_{CC} Standby Supply Current	V_{CC} = Max, V_{IN} = 0 or V_{CC} (8)			100	µA
$I_{CC/f}$ (4)	V_{CC} Active Supply Current	V_{CC} = Max (CMOS Inputs) (5,6)			1.5	mA/MHz
C_I	Input Capacitance	V_{CC} = 5 V, V_{IN} = 2.0 V		12		pF
C_B	I/O Capacitance	V_B = 2.0 V		15		pF

Notes:
1. All typical values are at V_{CC} = 5 V, T_A = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Duration of short-circuit should not exceed one second. Test one at a time.
4. Tested with TLL input levels: V_{IL} = 0.45 V, V_{IH} = 2.4 V. Measured with all outputs switching.
5. ΔI_{CC}/TLL input = 2 mA.
6. ΔI_{CC} vs. frequency (registered configuration) = 2 mA/MHz.
7. I_{IL} for Pin 1 (I_O/CLK) is ± 10 µA with V_{IN} = 0.4 V.
8. V_{IN} includes CLK and $\overline{OE}$ if applicable.

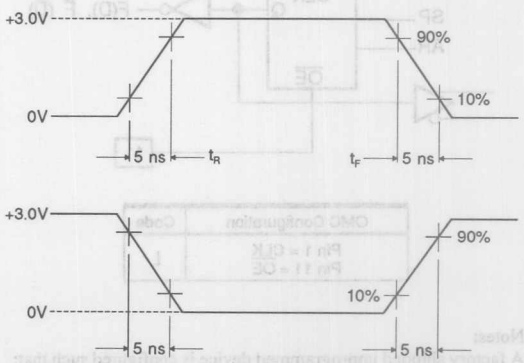
A.C. Test Conditions



Notes:
C_1 and C2 are to bypass V_{CC} to GND.
C_L = 50 pF
R_1 = 200 Ω
R_2 = 390 Ω

Voltage Waveforms

Input Pulses



Note: All circuit delays are measured at the +1.5 V level of inputs and outputs, unless otherwise specified.

A.C. Read Characteristics

T_{AC} = 0°C to +75°C, V_{CC} = 4.75 V to 5.25 V; T_{AI} = -40°C to 85°C, V_{CC} = 4.5 V to 5.25 V; R_2 = 390 Ω

				AT18V8Z								
				-25		-30		-35 (Comm.)		-35 (Ind.)		
Symbol	Parameter	From	To	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{CKP}	Clock Period (Minimum t_{IS} + t_{CKO})	CLK+	CLK+	33		40		47		57		ns
t_{CKH}	Clock Width High	CLK+	CLK-	15		20		20		25		ns
t_{CKL}	Clock Width Low	CLK-	CLK+	15		20		20		25		ns
t_{ARW}	Asynchronous Reset Pulse Width	I±, F±	I±, F±	25		30		35		40		ns
t_{IH}	Input or Feedback Data Hold Time	CLK+	Input±	0		0		0		0		ns
t_{IS}	Input of Feedback Data Setup Time	I±, F±	CLK+	18		2		25		30		ns
t_{PD}	Delay from Input to Active Output	I±, F±	F±		25		30		35		40	ns
t_{CKO}	Clock High to Output Valid Access Time	CLK+	F±		15		18		22		27	ns
t_{OE1}	Product Term Enable to Outputs Off	I±, F±	F±		25		30		35		40	ns
t_{OD1}	Pin 11 Output Disable to Outputs Off	I±, F±	F±		25		30		35		40	ns
t_{OD2}	Pin 11 Output Disable High to Outputs Off	OE-	F±		20		25		25		30	ns
t_{OE2}	Pin 11 Output Enable to Active Output	OE+	F±		20		25		25		30	ns
t_{ARD}	Asynchronous Reset Delay	I±, F±	F+		30		35		35		40	ns
t_{ARR}	Asynchronous Reset Recovery Time	I±, F±	CLK+	20		25		25		30		ns
t_{SPR}	Synchronous Preset Recovery Time	I±, F±	CLK+	20		25		25		30		ns
t_{PPR}	Power-Up Reset	V_{CC}+	F+		25		30		35		40	ns
f_{MAX}	Maximum Frequency	$1/(t_{IS} + t_{CKO})$			30		25		21		18	ns

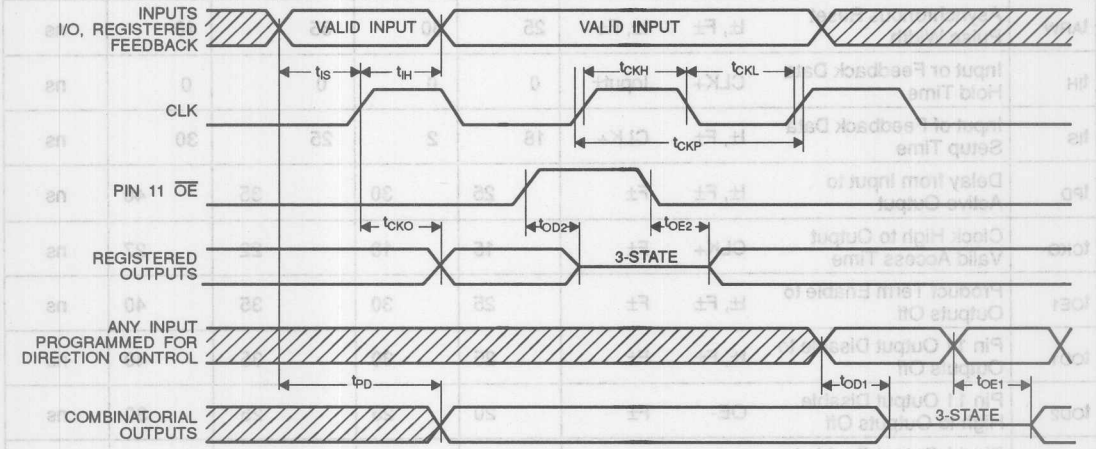
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Power Up Reset

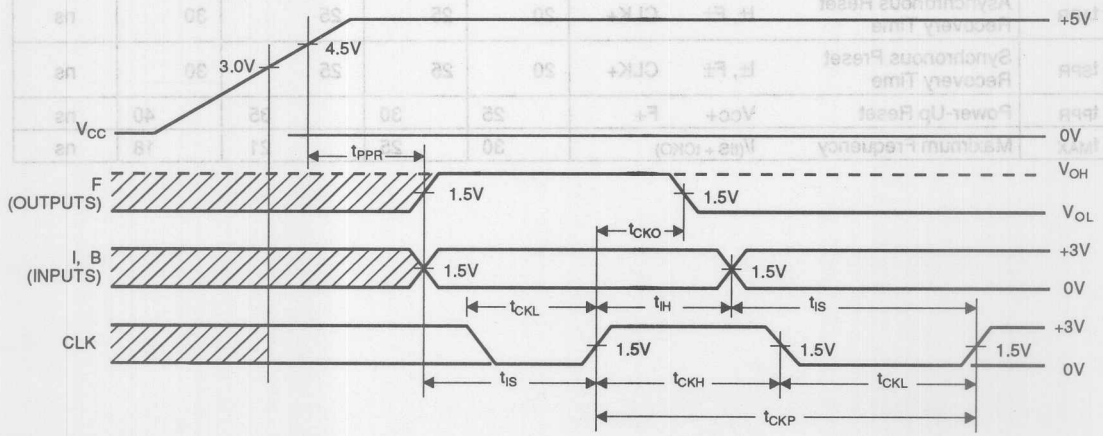
In order to facilitate state machine design and testing, a power-up reset function has been incorporated in the AT18V8Z. All internal registers will reset to Active-Low (logical "0") after a specified period of time (t_{PPR}).

Therefore, any OMC that has been configured as a registered output will always produce an Active-High on the associated output pin because of the inverted output buffer. The internal feedback (Q) of a registered OMC will also be set Low. The programmed polarity of OMC will not affect the Active-High output condition during a system power-up condition.

Switching Waveforms Timing Diagram

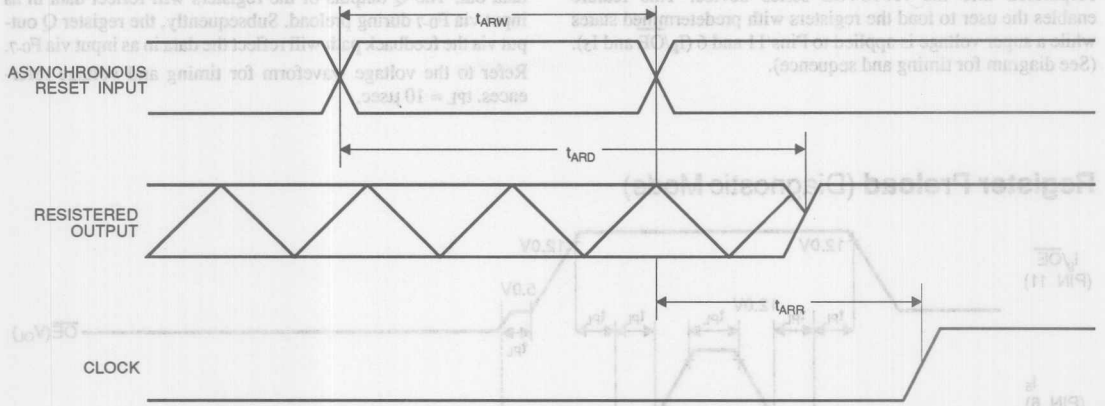


Power Up Reset Timing Diagram

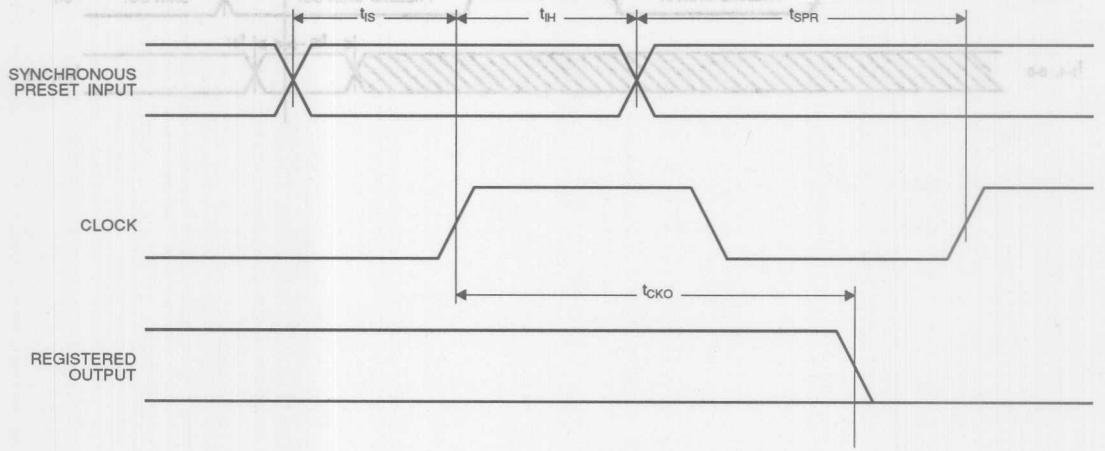


Note:
Diagram presupposes that the outputs (F) are enabled. The reset occurs regardless of the output condition (enabled or disabled).

Asynchronous Reset Timing Diagram



Synchronous Preset Timing Diagram



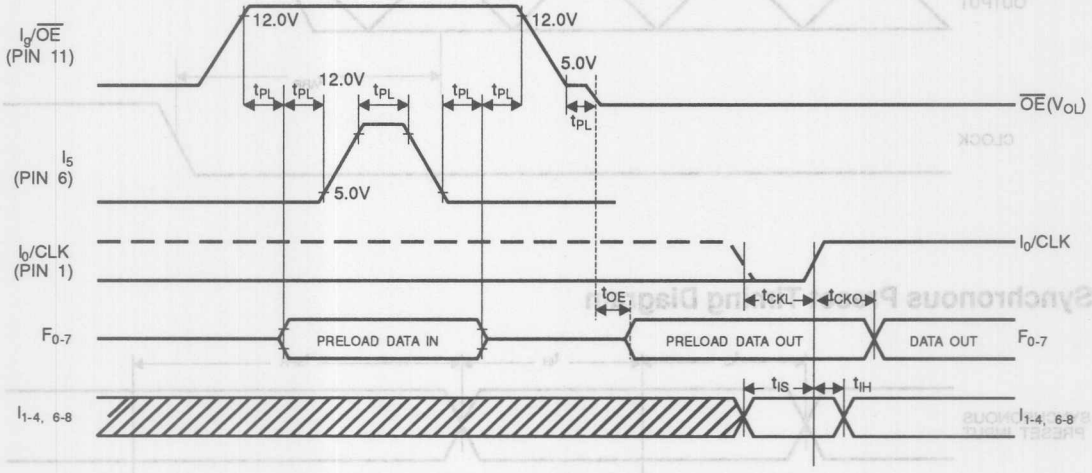
Register Preload Function (Diagnostic Mode Only)

In order to facilitate the testing of state machine/controller designs, a diagnostic mode register preload feature has been incorporated into the AT18V8Z series device. This feature enables the user to load the registers with predetermined states while a super voltage is applied to Pins 11 and 6 ($I_8/\overline{OE}$ and I_5). (See diagram for timing and sequence).

To read the data out, Pins 11 and 6 must be returned to normal TLL levels. The outputs, F_{0-7}, must be enabled in order to read data out. The Q outputs of the registers will reflect data in as input via F_{0-7} during preload. Subsequently, the register Q output via the feedback path will reflect the data in as input via F_{0-7}.

Refer to the voltage waveform for timing and voltage references. t_{PL} = 10 µsec.

Register Preload (Diagnostic Mode)



Logic Programming

The AT18V8Z series is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Signetics AMAZE, SLICE, and SNAP design software packages. ABEL™ and CUPL™ design packages also support the AT18V8Z architecture.

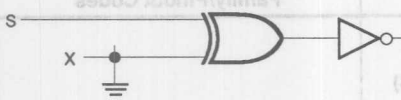
All packages allow Boolean and state equation entry formats. SNAP, ABEL, and CUPL also accept, as input, schematic capture format.

AT18V8Z logic designs can also be generated using the program table entry format, which is detailed on the following pages. This program table entry format is supported by AMAZE and SLICE only. Both AMAZE and SLICE design packages are available, free of charge, to qualified users.

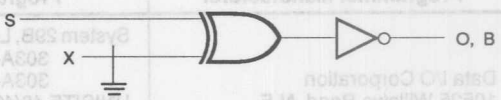
With Logic programming, the AND/OR/Ex-OR gate input connections necessary to implement the desired logic function are coded directly from logic equations using the Program Table. Similarly, various OMC configurations are implemented by programming the Architecture Control bits AC1 and AC2. Note that the configuration cell is automatically programmed based on the OMC configuration.

In this table, the logic state of variables I, P, and B associated with each Sum Term S is assigned a symbol which results in the proper fusing pattern of corresponding link pairs, defined as follows:

Output Polarity (O, B)

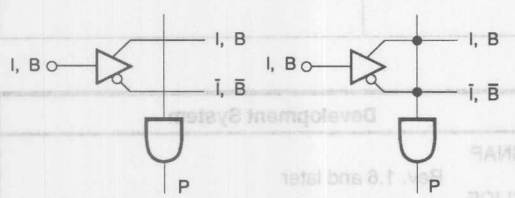


Active Level	Code
Inverting[1]	L



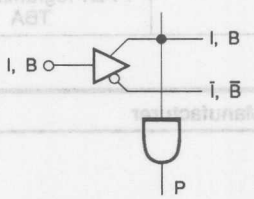
Active Level	Code
Non-inverting	H

"AND" Array (I, B)

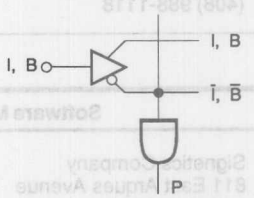


State	Code
Don't Care	–

State	Code
Inactive[1]	O



State	Code
I, B	H



State	Code
$\overline{I}$, $\overline{B}$	L

Note:
1. A factory-shipped unprogrammed device is configured such that all cells are in a conductive state.

ABEL and CUPL may be registered trademarks of others.

Erasure Characteristics (For Quartz Window Packages Only)

The erasure characteristics of the AT18V8Z Series devices are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lighting could erase a typical AT18V8Z in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the AT18V8Z is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure for the AT18V8Z is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15 $Wsec/cm^2$. The erasure time with this dosage is approximately 30 to 35 minutes using an ultraviolet lamp with a 12,000 $\mu W/cm^2$ power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a CMOS EPLD can be exposed to without damage is 7258 $Wsec/cm^2$. Exposure of these CMOS EPLDs to high intensity UV light for longer periods may cause permanent damage.

Programing

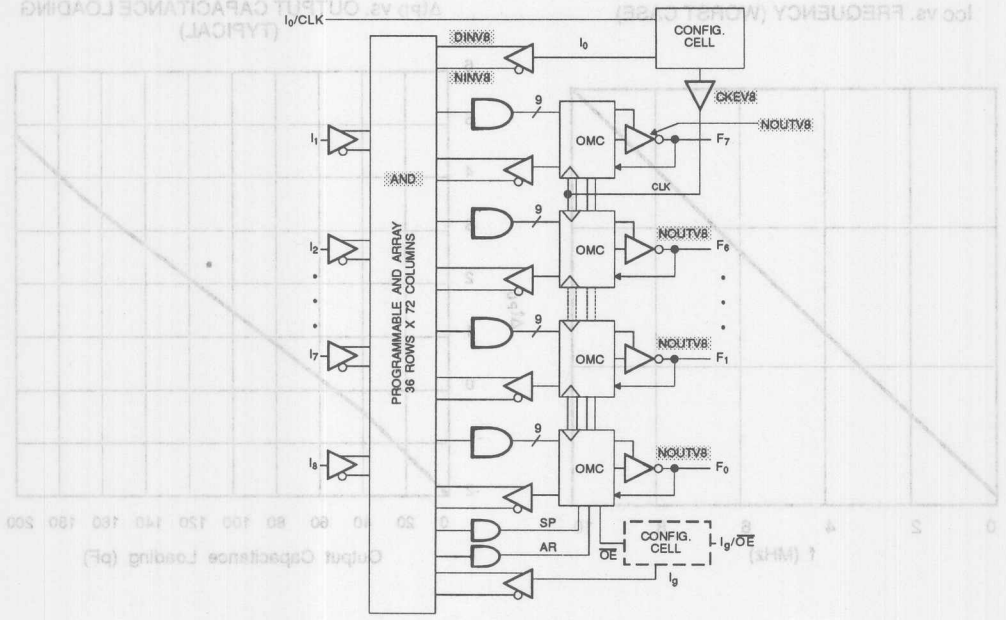
The AT18V8Z is programmable on conventional programmers for 20-pin PAL devices.

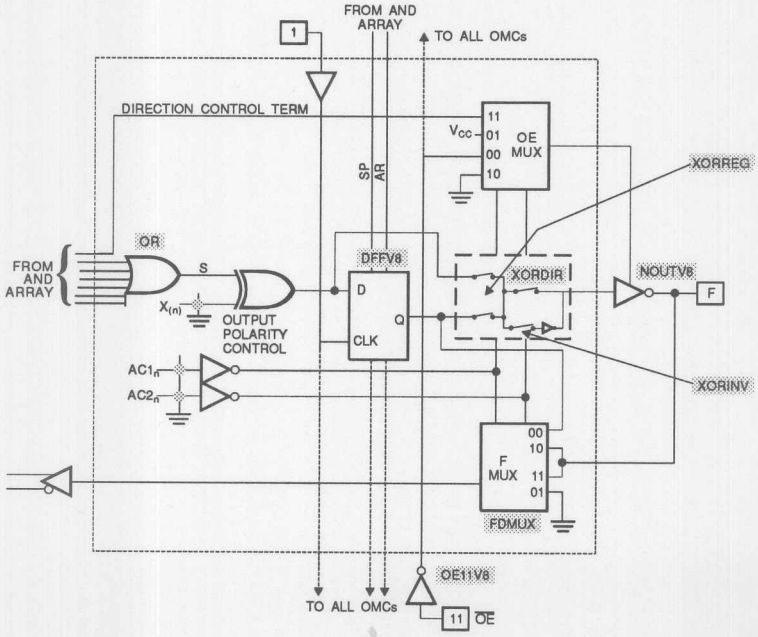
Refer to the following charts for qualified manufacturers of programmers and software tools:

Programmer Manufacturer	Programmer Model	Family/Pinout Codes
Data I/O Corporation 10525 Willows Road, N.E. P.O. Box 97046 Redmond, Washington 98073-9746 (800) 247-5700	System 29B, LogicPak™ 303A-011A; V09 (DIL) 303A-011B; VO4 (PLCC) UNISITE 40/48 V2.6 (DIL) Chipsite (PLCC)-V2.8 MODEL 60 360A001 (DIL) 360A006 (PLCC)	86/4F
Stag Microsystems, Inc. 1600 Wyatt Drive, Suite 3 Santa Clara, California 95054 (408) 988-1118	ZL30/30A Programmer Rev. 30A34 (DIL) 30A001 Adaptor (PLCC) PPZ Programmer TBA	12/205

Software Manufacturer	Development System
Signetics Company 811 East Arques Avenue P.O. Box 3409 Sunnyvale, California 94088-3409 (408) 991-2000	SNAP Rev. 1.6 and later SLICE Rev. 1.0 and later AMAZE Software Rev. 1.8 and later
Data I/O Corporation 10525 Willows Road, N.E. P.O. Box 97046 Redmond, Washington 98073-9746 (800) 247-5700	ABEL™ Software
Logical Devices, Inc. 1201 Northwest 65th Place Fort Lauderdale, Florida 33309 (800) 331-7766	CUPL™ Software

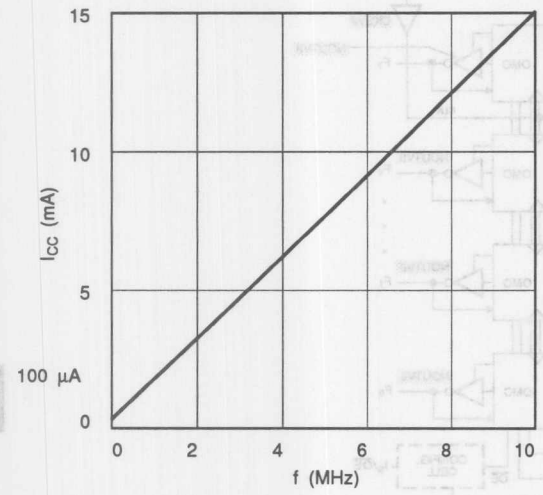
Snap Resource Summary Designations



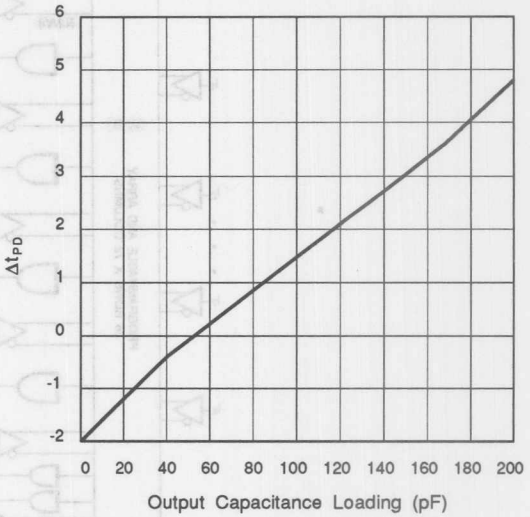


Note:
▒ Denotes a programmable cell location.

I_{CC} vs. FREQUENCY (WORST CASE)



Δt_{PD} vs. OUTPUT CAPACITANCE LOADING (TYPICAL)



Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
25	18	15	AT18V8Z-25DC AT18V8Z-25JC AT18V8Z-25PC	20DW3 20J 20P3	Commercial (0°C to 70°C)
30	22	18	AT18V8Z-30DI AT18V8Z-30JI AT18V8Z-30PI	20DW3 20J 20P3	Industrial (-40°C to 85°C)
35	25	22	AT18V8Z-35DC AT18V8Z-35JC AT18V8Z-35PC	20DW3 20J 20P3	Commercial (0°C to 70°C)
40	30	27	AT18V8Z-40DI AT18V8Z-40JI AT18V8Z-40PI	20DW3 20J 20P3	Industrial (-40°C to 85°C)

Package Type	
20DW3	20 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
20J	20 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
20P3	20 Lead, 0.300" Wide Plastic Dual Inline Package OTP (PDIP)

Ordering Information

t_{PD} (ns)	t_S (ns)	I_{CC} (mA)	Ordering Code	Package	Operation Range
25	18	15	AT18V82-25JC AT18V82-25LC AT18V82-25PC	20DW3 20J 20P3	Commercial (0°C to 70°C)
30	22	15	AT18V82-30DI AT18V82-30JI AT18V82-30PI	20DW3 20J 20P3	Industrial (-40°C to 85°C)
35	25	22	AT18V82-35DC AT18V82-35JC AT18V82-35PC	20DW3 20J 20P3	Commercial (0°C to 70°C)
40	30	27	AT18V82-40DI AT18V82-40JI AT18V82-40PI	20DW3 20J 20P3	Industrial (-40°C to 85°C)

Package Type	
20DW3	20 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
20J	20 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
20P3	20 Lead, 0.300" Wide Plastic Dual Inline Package OTP (PDIP)

Features

- **High Speed Programmable Logic Device**
  - **15 ns Max Propagation Delay**
  - **5 V ±10% Operation**
- **Low Power CMOS Operation**

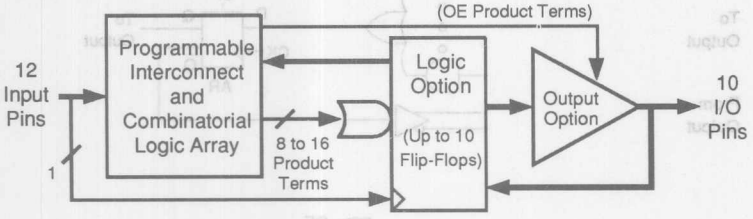
Speed	"L"	-15,-20	All
Temp	C/M	C/M	Others
Icc(mA)	12/15	90/100	55

- **CMOS and TTL Compatible Inputs and Outputs**
  - **10 µA Leakage Maximum**
- **Reprogrammable - Tested 100% for Programmability**
- **High Reliability CMOS Technology**
  - **2000 V ESD Protection**
  - **200 mA Latchup Immunity**
- **Full Military, Commercial and Industrial Temperature Ranges**
- **Dual-In-Line and Surface Mount Packages**

High Speed UV Erasable Programmable Logic Device

7

Logic Diagram



Description

The AT22V10 and AT22V10L are CMOS high performance Erasable Programmable Logic Devices (EPLDs). Speeds down to 15 ns and power dissipation as low as 12 mA are offered. All speed ranges are specified over the full 5 V ±10% range. All pins offer a low ±10 µA leakage.

The AT22V10L provides the optimum low power CMOS EPLD solution, with low DC power (8 mA typical) and full CMOS output levels. The AT22V10L significantly reduces total system power and enhances system reliability.

Full CMOS output levels help reduce power in many other system components.

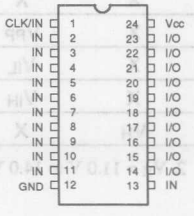
The AT22V10 and AT22V10L incorporate a variable product term architecture. Each output is allocated from eight to 16 product terms, which allows highly complex logic functions to be realized.

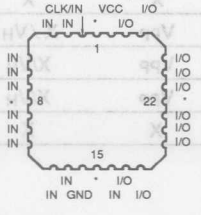
Two additional product terms are included to provide synchronous preset and asynchronous reset. These terms are common to all 10 registers. All registers are automatically cleared upon power up.

Register Preload simplifies testing. A Security Fuse prevents unauthorized copying of programmed fuse patterns.

Pin Configurations

Pin Name	Function
CLK/IN	Clock and Logic Input
IN	Logic Inputs
I/O	Bidirectional Buffers
*	No Internal Connection
VCC	+5 V Supply





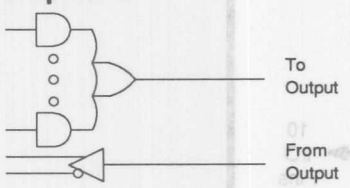
Absolute Maximum Ratings*

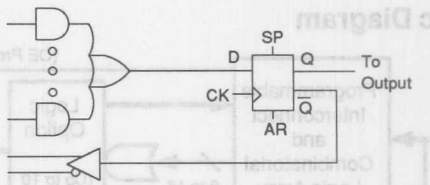
Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0 V to +14.0 V(1)
Programming Voltage with Respect to Ground	-2.0 V to +14.0 V(1)
Integrated UV Erase Dose	7258 W·sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

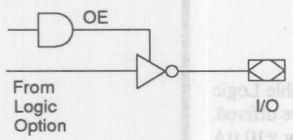
Note:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC}+0.75 V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

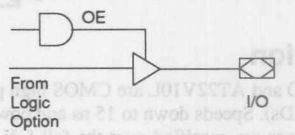
Logic Options





Output Options





D.C. and A.C. Operating Conditions

	Commercial AT22V10/L -15, -20, -25, -35	Industrial AT22V10/L -15, -20, -25, -35	Military AT22V10/L -15, -20, -25, -30
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C	-55°C - 125°C
V_{CC} Power Supply	5 V ± 10%	5 V ± 10%	5 V ± 10%

Operating Modes

	24-Pin DIP	1	5	8	13	I/Os	Vcc(24)
Mode	28-Pin JLCC	2	6	10	16	I/Os	Vcc(28)
"EPLD"		X(1)	X	X	X	I/O	5 V
Program		V_{PP}	X / V_H (2)	X	V_{PP}	D_{IN}	6 V
PGM Verify		V_{PP}	X/V_H	X	V_{IL}	D_{OUT}	6 V
PGM Inhibit		V_{PP}	X/V_H	X	V_{IH}	High Z	6 V
Preload		X	X	V_H	X	D_{IN}	5 V

Notes: 1. X can be V_{IL} or V_{IH}. 2. V_H = 11.0 V to 14.0 V

D.C. Characteristics

Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1 V to V_{CC}+1 V					10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1 V to V_{CC}+0.1 V					10	µA
I_{CC}	Power Supply Current	V_{CC} = MAX, V_{IN} = GND, Outputs Open	AT22V10-15,-20	Com.			90	mA
				Ind., Mil.			100	mA
			AT22V10-25,-35(2)				55	mA
			AT22V10L(2)	Com.		1.7	12	mA
				Ind., Mil.		2.0	15	mA
I_{CC2}	Clocked Power Supply Current	f = 1 MHz, V_{CC} = MAX, Outputs Open	AT22V10L(2)	Com.			15	mA
				Ind., Mil.			20	mA
I_{OS} (1)	Output Short Circuit Current	V_{OUT} = 0.5 V					-90	mA
V_{IL}	Input Low Voltage				-0.6		0.8	V
V_{IH}	Input High Voltage				2.0		V_{CC}+0.75	V
V_{OL}	Output Low Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = MIN	I_{OL} = 16 mA	Com.,Ind.			0.5	V
			I_{OL} = 12 mA	Mil.			0.5	V
			I_{OL} = 24 mA	Com.			0.8	V
V_{OH}	Output High Voltage	V_{IN}=V_{IH} or V_{IL}, V_{CC}=MIN	I_{OH} = -100 µA		V_{CC}-0.3			V
			I_{OH} = -4.0 mA		2.4			V

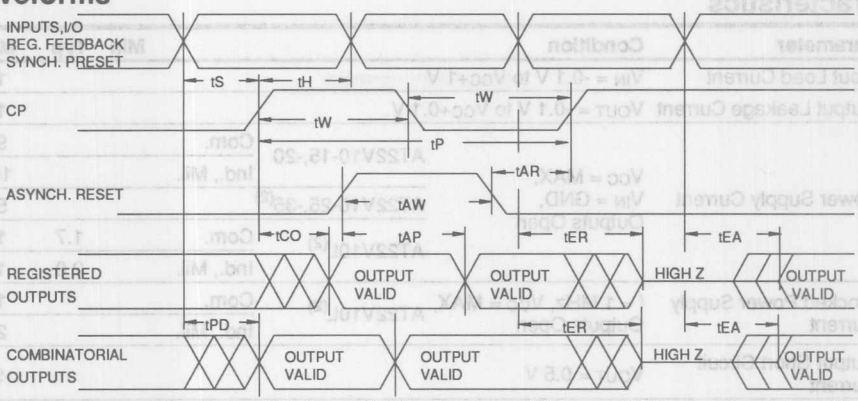
Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.

2. See I_{CC} vs. Frequency curves in the back of this data sheet.

A.C. Characteristics, Commercial and Industrial

		AT22V10-15			AT22V10/L-20			AT22V10/L-25			AT22V10/L-35			
Symbol	Parameter	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
t_{PD}	Input or Feedback to Non-Registered Output		10	15		12	20		15	25		20	35	ns
t_{EA}	Input to Output Enable		10	15			20		15	25		20	35	ns
t_{ER}	Input to Output Disable		10	15			20		15	25		20	35	ns
t_{CF}	Clock to Feedback	0	1	2.5	0	4	8	0	5	10	0	10	15	ns
t_{CO}	Clock to Output	0	7	10	0	8	12	0	10	15	0	12	20	ns
t_S	Input or Feedback Setup Time	10	8		12	8		15	12		20	15		ns
t_H	Hold Time	0			0			0			0			ns
t_P	Clock Period	12			20			24			30			ns
t_W	Clock Width	6			10			12			15			ns
F_{MAX}	External Feedback $1/(t_S+t_{CO})$			50.0			41.6			33.3			25.0	MHz
	Internal Feedback $1/(t_S + t_{CF})$			80.0			50.0			40.0			28.5	MHz
	No Feedback $1/(t_P)$			83.3			50.0			41.6			33.3	MHz
t_{AW}	Asynchronous Reset Width	15	8		20	9		25	10		30	15		ns
t_{AR}	Asynchronous Reset, Synchronous Preset, Recovery Time	15	8		20	12		25	15		30	18		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		12	20		15	22		18	25		20	30	ns

A.C. Waveforms [1]

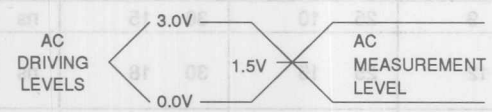


Note: 1. Timing measurement reference is 1.5 V. Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.

A.C. Characteristics, Military

		AT22V10-15			AT22V10/L-20			AT22V10/L-25			AT22V10/L-30			
Symbol	Parameter	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
t_{PD}	Input or Feedback to Non-Registered Output		10	15		12	20		15	25		20	30	ns
t_{EA}	Input to Output Enable		10	15			20		15	25		20	30	ns
t_{ER}	Input to Output Disable		10	15			20		15	25		20	30	ns
t_{CF}	Clock to Feedback	0	1	2.5	0	4	8	0	5	10	0	10	15	ns
t_{CO}	Clock to Output	0	7	10	0	8	15	0	10	15	0	12	20	ns
t_{SF}	Feedback Setup Time	10	8		12	10		15	12		18	15		ns
t_S	Input Setup Time	10	8		17	14		18	15		20	15		ns
t_H	Hold Time	0			0			0			0			ns
t_P	Clock Period	12			20			24			30			ns
t_W	Clock Width	6			10			12			15			ns
F_{MAX}	External Feedback $1/(t_S+t_{CO})$			50.0			31.2			30.3			25.0	MHz
	Internal Feedback $1/(t_S + t_{CF})$			80.0			50.0			40.0			30.0	MHz
	No Feedback $1/(t_P)$			83.3			50.0			41.6			33.3	MHz
t_{AW}	Asynchronous Reset Width	15	8		20	9		25	10		30	15		ns
t_{AR}	Asynchronous Reset Recovery Time	15	8		20	12		25	15		30	18		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		12	20		15	22		18	25		20	30	ns

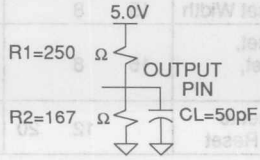
Input Test Waveforms and Measurement Levels



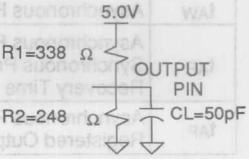
tR, tF < 5 ns (10% to 90%)

Output Test Loads:

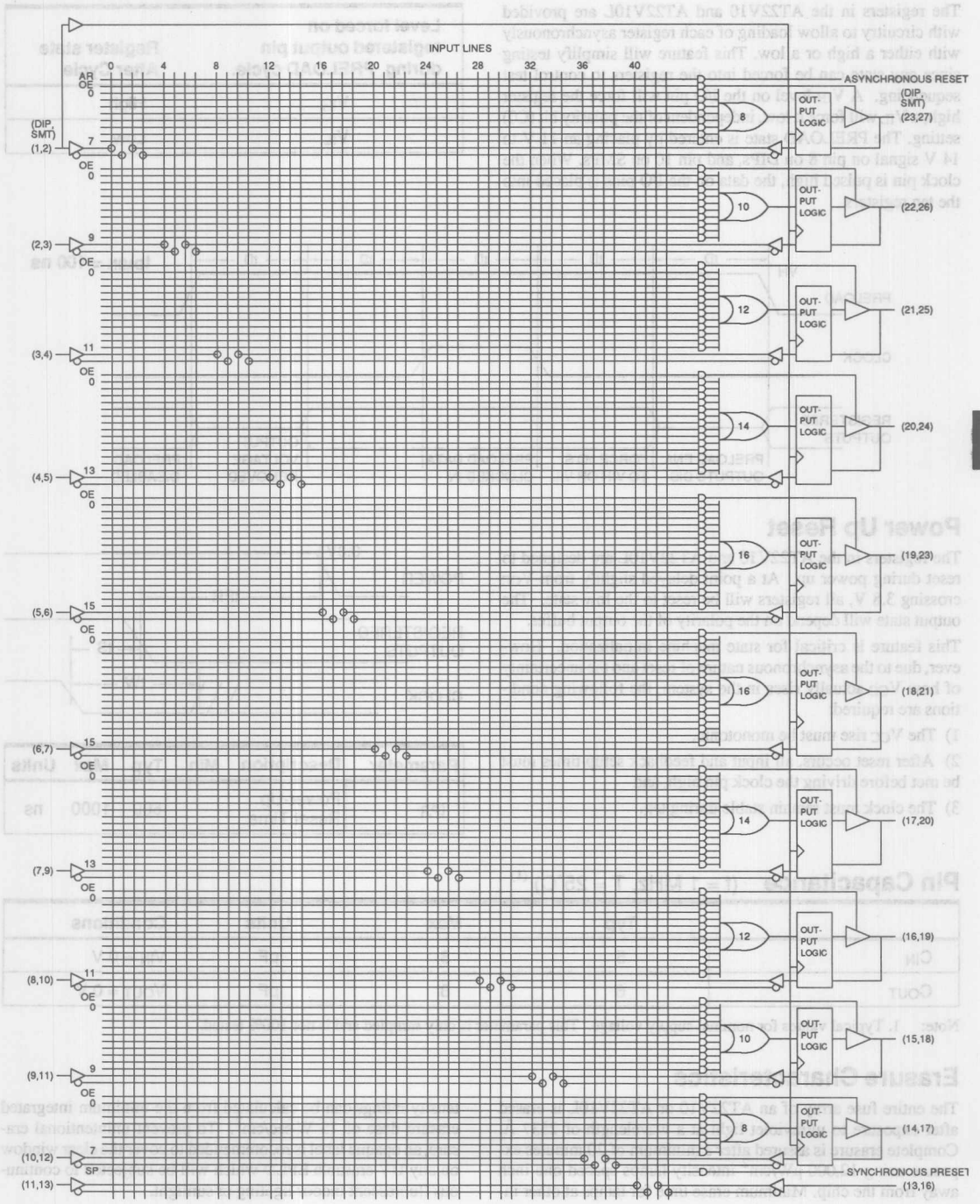
Commercial



Military



Functional Logic Diagram AT22V10/L

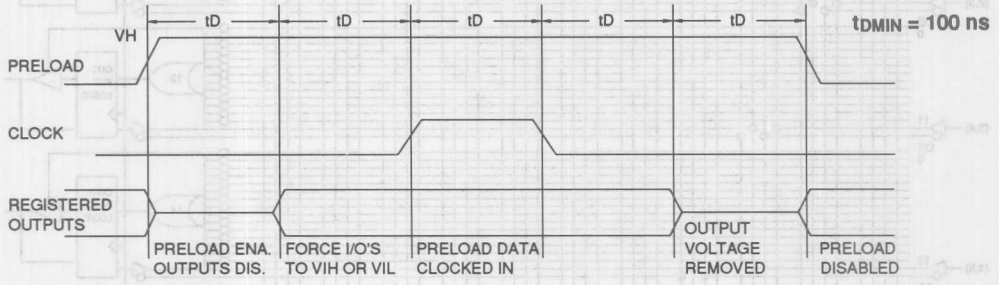


7

Preload of Registered Outputs

The registers in the AT22V10 and AT22V10L are provided with circuitry to allow loading of each register asynchronously with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A V_{IH} level on the I/O pin will force the register high; a V_{IL} will force it low, independent of the polarity bit (C0) setting. The PRELOAD state is entered by placing an 11 V to 14 V signal on pin 8 on DIPs, and pin 10 on SMPs. When the clock pin is pulsed high, the data on the I/O pins is placed into the ten registers.

Level forced on registered output pin during PRELOAD cycle.	Register state After Cycle
V_{IH}	High
V_{IL}	Low



Power Up Reset

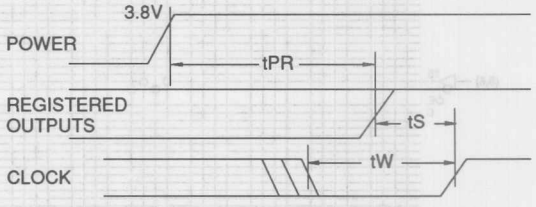
The registers in the AT22V10 and AT22V10L are designed to reset during power up. At a point delayed slightly from V_{CC} crossing 3.8 V, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1) The V_{CC} rise must be monotonic,

2) After reset occurs, all input and feedback setup times must be met before driving the clock pin high, and

3) The clock must remain stable during t_{PR}.



Parameter	Description	Min	Typ	Max	Units
t_{PR}	Power-Up Reset Time		600	1000	ns

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	5	8	pF	V_{IN} = 0 V
C_{OUT}	6	8	pF	V_{OUT} = 0 V

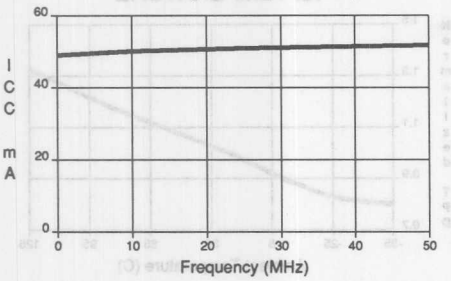
Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Erasure Characteristics

The entire fuse array of an AT22V10 or AT22V10L is erased after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 $W\text{-}sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPLD which will be subjected to continuous fluorescent indoor lighting or sunlight.

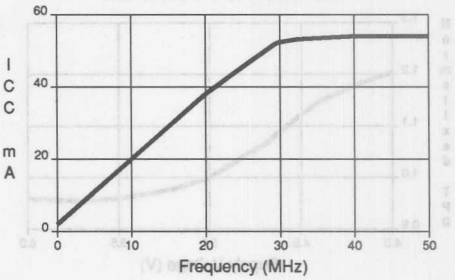
SUPPLY CURRENT vs. INPUT FREQUENCY

AT22V10 (TA = 25C, VCC = 5V)

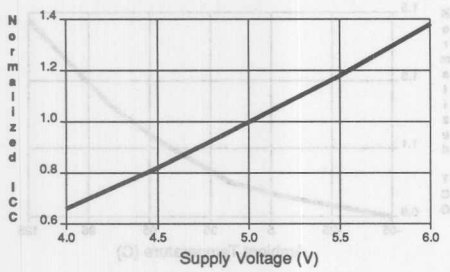


SUPPLY CURRENT vs. INPUT FREQUENCY

AT22V10L (TA = 25C, VCC = 5V)

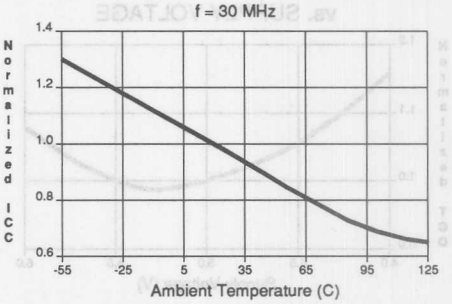


NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE

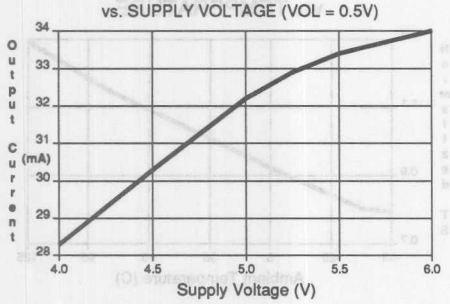


NORMALIZED ICC vs. AMBIENT TEMP.

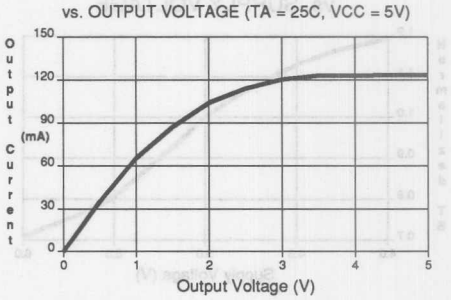
f = 30 MHz



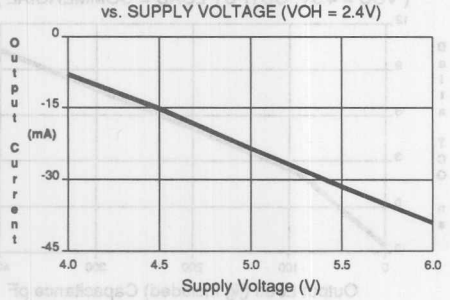
OUTPUT SINK CURRENT vs. SUPPLY VOLTAGE (VOL = 0.5V)



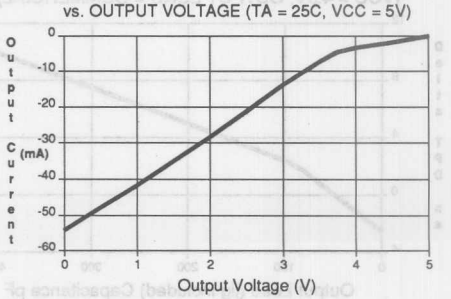
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE (TA = 25C, VCC = 5V)



OUTPUT SOURCE CURRENT vs. SUPPLY VOLTAGE (VOH = 2.4V)

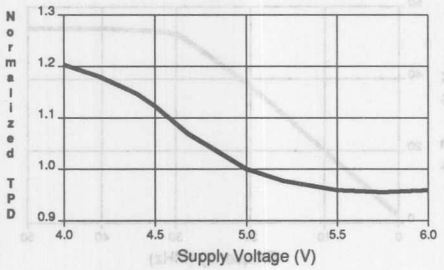


OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE (TA = 25C, VCC = 5V)

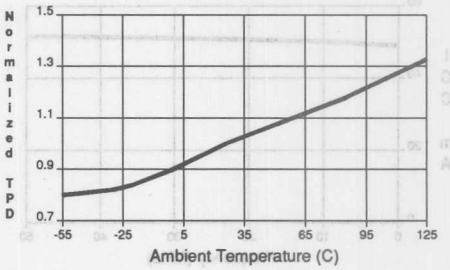


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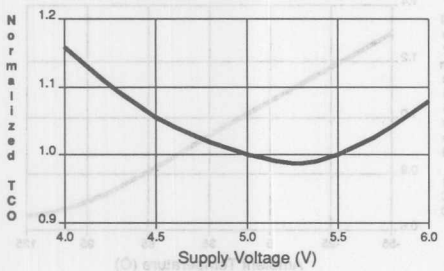
NORMALIZED TPD vs. SUPPLY VOLTAGE



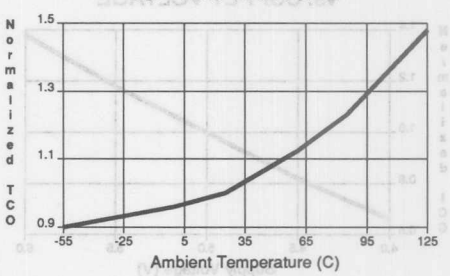
NORMALIZED TPD vs. TEMPERATURE



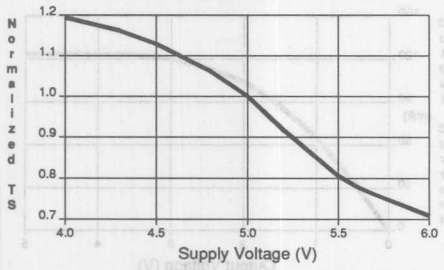
NORMALIZED TCO vs. SUPPLY VOLTAGE



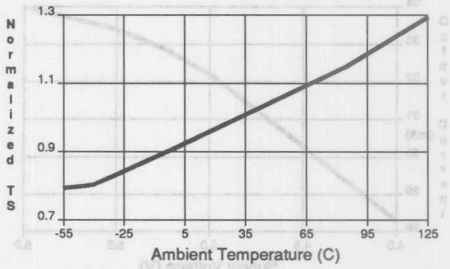
NORMALIZED TCO vs. TEMPERATURE



NORMALIZED TS vs. SUPPLY VOLTAGE

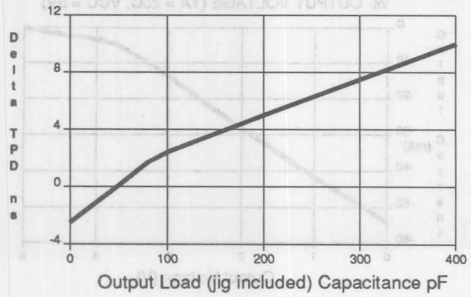


NORMALIZED TS vs. TEMPERATURE



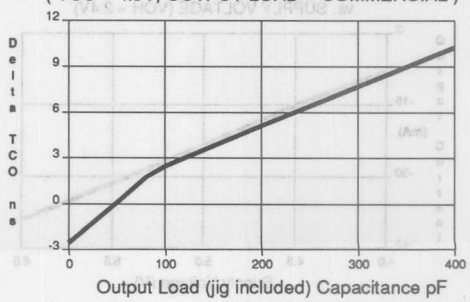
DELTA TPD vs. OUTPUT LOADING

(VCC = 4.5V, OUTPUT LOAD = COMMERCIAL)



DELTA TCO vs. OUTPUT LOADING

(VCC = 4.5V, OUTPUT LOAD = COMMERCIAL)



Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
15	10	10	AT22V10-15DC	24DW3	Commercial (0°C to 70°C)
			AT22V10-15FC	24C	
			AT22V10-15GC	24D3	
			AT22V10-15JC	28J	
			AT22V10-15KC	28KW	
			AT22V10-15LC	28LW	
			AT22V10-15NC	28L	
			AT22V10-15PC	24P3	
			AT22V10-15SC	24S	
			AT22V10-15YC	24CW	
			AT22V10-15DI	24DW3	Industrial (-40°C to 85°C)
			AT22V10-15FI	24C	
			AT22V10-15GI	24D3	
			AT22V10-15JI	28J	
			AT22V10-15KI	28KW	
			AT22V10-15LI	28LW	
			AT22V10-15NI	28L	
			AT22V10-15PI	24P3	
			AT22V10-15SI	24S	
			AT22V10-15YI	24CW	
			AT22V10-15DM	24DW3	Military (-55°C to 125°C)
			AT22V10-15FM	24C	
			AT22V10-15GM	24D3	
			AT22V10-15KM	28KW	
			AT22V10-15LM	28LW	
			AT22V10-15NM	28L	
			AT22V10-15YM	24CW	
			AT22V10-15DM/883	24DW3	Military/883C (-55°C to 125°C) Class B, Fully Compliant
			AT22V10-15FM/883	24C	
			AT22V10-15GM/883	24D3	
			AT22V10-15KM/883	28KW	
			AT22V10-15LM/883	28LW	
			AT22V10-15NM/883	28L	
			AT22V10-15YM/883	24CW	
20	12	15	AT22V10-20DC	24DW3	Commercial (0°C to 70°C)
			AT22V10-20FC	24C	
			AT22V10-20GC	24D3	
			AT22V10-20JC	28J	
			AT22V10-20KC	28KW	
			AT22V10-20LC	28LW	
			AT22V10-20NC	28L	
			AT22V10-20PC	24P3	
			AT22V10-20SC	24S	
			AT22V10-20YC	24CW	

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Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
20	12	15	AT22V10-20DI	24DW3	Industrial (-40°C to 85°C)
			AT22V10-20FI	24C	
			AT22V10-20GI	24D3	
			AT22V10-20JI	28J	
			AT22V10-20KI	28KW	
			AT22V10-20LI	28LW	
			AT22V10-20NI	28L	
			AT22V10-20PI	24P3	
			AT22V10-20SI	24S	
			AT22V10-20YI	24CW	
20	17	15	AT22V10-20DM	24DW3	Military (-55°C to 125°C)
			AT22V10-20FM	24C	
			AT22V10-20GM	24D3	
			AT22V10-20KM	28KW	
			AT22V10-20LM	28LW	
			AT22V10-20NM	28L	
			AT22V10-20YM	24CW	
			AT22V10-20DM/883	24DW3	Military/883C (-55°C to 125°C) Class B, Fully Compliant
			AT22V10-20FM/883	24C	
			AT22V10-20GM/883	24D3	
			AT22V10-20KM/883	28KW	
			AT22V10-20LM/883	28LW	
			AT22V10-20NM/883	28L	
			AT22V10-20YM/883	24CW	
25	15	15	AT22V10-25DC	24DW3	Commercial (0°C to 70°C)
			AT22V10-25FC	24C	
			AT22V10-25GC	24D3	
			AT22V10-25JC	28J	
			AT22V10-25KC	28KW	
			AT22V10-25LC	28LW	
			AT22V10-25NC	28L	
			AT22V10-25PC	24P3	
			AT22V10-25SC	24S	
			AT22V10-25YC	24CW	
			AT22V10-25DI	24DW3	Industrial (-40°C to 85°C)
			AT22V10-25FI	24C	
			AT22V10-25GI	24D3	
			AT22V10-25JI	28J	
			AT22V10-25KI	28KW	
			AT22V10-25LI	28LW	
			AT22V10-25NI	28L	
			AT22V10-25PI	24P3	
			AT22V10-25SI	24S	
			AT22V10-25YI	24CW	

Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
25	18	15	AT22V10-25DM	24DW3	Military (-55°C to 125°C)
			AT22V10-25FM	24C	
			AT22V10-25GM	24D3	
			AT22V10-25KM	28KW	
			AT22V10-25LM	28LW	
			AT22V10-25NM	28L	
			AT22V10-25YM	24CW	
			AT22V10-25DM/883	24DW3	Military/883C (-55°C to 125°C) Class B, Fully Compliant
			AT22V10-25FM/883	24C	
			AT22V10-25GM/883	24D3	
			AT22V10-25KM/883	28KW	
			AT22V10-25LM/883	28LW	
			AT22V10-25NM/883	28L	
			AT22V10-25YM/883	24CW	
30	20	20	AT22V10-30DM	24DW3	Military (-55°C to 125°C)
			AT22V10-30FM	24C	
			AT22V10-30GM	28D3	
			AT22V10-30KM	28KW	
			AT22V10-30LM	28LW	
			AT22V10-30NM	28L	
			AT22V10-30YM	24CW	
			AT22V10-30DM/883	24DW3	Military/883C (-55°C to 125°C) Class B, Fully Compliant
			AT22V10-30FM/883	24C	
			AT22V10-30GM/883	24D3	
			AT22V10-30KM/883	28KW	
			AT22V10-30LM/883	28LW	
			AT22V10-30NM/883	28L	
			AT22V10-30YM/883	24CW	
35	25	25	AT22V10-35DC	24DW3	Commercial (0°C to 70°C)
			AT22V10-35FC	24C	
			AT22V10-35GC	24D3	
			AT22V10-35JC	28J	
			AT22V10-35KC	28KW	
			AT22V10-35LC	28LW	
			AT22V10-35NC	28L	
			AT22V10-35PC	24P3	
			AT22V10-35SC	24S	
			AT22V10-35YC	24CW	
			AT22V10-35DI	24DW3	Industrial (-40°C to 85°C)
			AT22V10-35FI	24C	
			AT22V10-35GI	24D3	
			AT22V10-35JI	28J	
			AT22V10-35KI	28KW	
			AT22V10-35LI	28LW	
			AT22V10-35NI	28L	
			AT22V10-35PI	24P3	
			AT22V10-35SI	24S	
			AT22V10-35YI	24CW	

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Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
20	17	15	5962-87539 04 LX 5962-87539 04 3X	24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	18	15	5962-87539 01 KX 5962-87539 01 LX 5962-87539 01 3X	24CW 24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
30	20	20	5962-87539 02 KX 5962-87539 02 LX 5962-87539 02 3X	24CW 24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
40	30	25	5962-87539 03 KX 5962-87539 03 LX 5962-87539 03 3X	24CW 24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
15	10	10	5962-88670 05 LX 5962-88670 05 3X	24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
20	17	15	5962-88670 04 KX 5962-88670 04 LX 5962-88670 04 3X	24C 24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	18	15	5962-88670 01 KX 5962-88670 01 LX 5962-88670 01 3X	24C 24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
30	20	20	5962-88670 02 KX 5962-88670 02 LX 5962-88670 02 3X	24C 24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
40	30	25	5962-88670 03 KX 5962-88670 03 LX 5962-88670 03 3X	24C 24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant

Package Type	
24DW3	24 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
24C	24 Lead, Non-Windowed, Ceramic Flat Package (Cerpack)
24D3	24 Lead, 0.300" Wide, Non-Windowed (OTP), Ceramic Dual Inline Package (Cerdip)
28J	28 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
28KW	28 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
28LW	28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28L	28 Pad, Non-Windowed, Ceramic Leadless Chip Carrier OTP (LCC)
24P3	24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
24S	24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline OTP (SOIC)
24CW	24 Lead, Windowed, Ceramic Flat Package (Cerpack)

Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
20	12	15	AT22V10L-20DC	24DW3	Commercial (0°C to 70°C)
			AT22V10L-20FC	24C	
			AT22V10L-20GC	24D3	
			AT22V10L-20JC	28J	
			AT22V10L-20KC	28KW	
			AT22V10L-20LC	28LW	
			AT22V10L-20NC	28L	
			AT22V10L-20PC	24P3	
			AT22V10L-20SC	24S	
			AT22V10L-20YC	24CW	
			AT22V10L-20DI	24DW3	Industrial (-40°C to 85°C)
			AT22V10L-20FI	24C	
			AT22V10L-20GI	24D3	
			AT22V10L-20JI	28J	
			AT22V10L-20KI	28KW	
			AT22V10L-20LI	28LW	
			AT22V10L-20NI	28L	
			AT22V10L-20PI	24P3	
			AT22V10L-20SI	24S	
			AT22V10L-20YI	24CW	
20	17	15	AT22V10L-20DM	24DW3	Military (-55°C to 125°C)
			AT22V10L-20FM	24C	
			AT22V10L-20GM	24D3	
			AT22V10L-20KM	28KW	
			AT22V10L-20LM	28LW	
			AT22V10L-20NM	28L	
			AT22V10L-20YM	24CW	
			AT22V10L-20DM/883	24DW3	Military/883C (-55°C to 125°C) Class B, Fully Compliant
			AT22V10L-20FM/883	24C	
			AT22V10L-20GM/883	24D3	
			AT22V10L-20KM/883	28KW	
			AT22V10L-20LM/883	28LW	
			AT22V10L-20NM/883	28L	
			AT22V10L-20YM/883	24CW	
25	15	15	AT22V10L-25DC	24DW3	Commercial (0°C to 70°C)
			AT22V10L-25FC	24C	
			AT22V10L-25GC	24D3	
			AT22V10L-25JC	28J	
			AT22V10L-25KC	28KW	
			AT22V10L-25LC	28LW	
			AT22V10L-25NC	28L	
			AT22V10L-25PC	24P3	
			AT22V10L-25SC	24S	
			AT22V10L-25YC	24CW	

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Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
25	15	15	AT22V10L-25DI	24DW3	Industrial (-40°C to 85°C)
			AT22V10L-25FI	24C	
			AT22V10L-25GI	24D3	
			AT22V10L-25JI	28J	
			AT22V10L-25KI	28KW	
			AT22V10L-25LI	28LW	
			AT22V10L-25NI	28L	
			AT22V10L-25PI	24P3	
			AT22V10L-25SI	24S	
			AT22V10L-25YI	24CW	
25	18	15	AT22V10L-25DM	24DW3	Military (-55°C to 125°C)
			AT22V10L-25FM	24C	
			AT22V10L-25GM	24D3	
			AT22V10L-25KM	28KW	
			AT22V10L-25LM	28LW	
			AT22V10L-25NM	28L	
			AT22V10L-25YM	24CW	
			AT22V10L-25DM/883	24DW3	Military/883C (-55°C to 125°C) Class B, Fully Compliant
			AT22V10L-25FM/883	24C	
			AT22V10L-25GM/883	24D3	
			AT22V10L-25KM/883	28KW	
			AT22V10L-25LM/883	28LW	
			AT22V10L-25NM/883	28L	
			AT22V10L-25YM/883	24CW	
30	20	20	AT22V10L-30DM	24DW3	Military (-55°C to 125°C)
			AT22V10L-30FM	24C	
			AT22V10L-30GM	24D3	
			AT22V10L-30KM	28KW	
			AT22V10L-30LM	28LW	
			AT22V10L-30NM	28L	
			AT22V10L-30YM	24CW	
			AT22V10L-30DM/883	24DW3	Military/883C (-55°C to 125°C) Class B, Fully Compliant
			AT22V10L-30FM/883	24C	
			AT22V10L-30GM/883	24D3	
			AT22V10L-30KM/883	28KW	
			AT22V10L-30LM/883	28LW	
			AT22V10L-30NM/883	28L	
			AT22V10L-30YM/883	24CW	
35	25	25	AT22V10L-35DC	24DW3	Commercial (0°C to 70°C)
			AT22V10L-35FC	24C	
			AT22V10L-35GC	24D3	
			AT22V10L-35JC	28J	
			AT22V10L-35KC	28KW	
			AT22V10L-35LC	28LW	
			AT22V10L-35NC	28L	
			AT22V10L-35PC	24P3	
			AT22V10L-35SC	24S	
			AT22V10L-35YC	24CW	

Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
35	25	15	AT22V10L-35DI AT22V10L-35FI AT22V10L-35GI AT22V10L-35JI AT22V10L-35KI AT22V10L-35LI AT22V10L-35NI AT22V10L-35PI AT22V10L-35SI AT22V10L-35YI	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24S 24CW	Industrial (-40°C to 85°C)
20	17	15	5962-88724 04 KX 5962-88724 04 LX 5962-88724 04 3X	24CW 24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	18	15	5962-88724 01 KX 5962-88724 01 LX 5962-88724 01 3X	24CW 24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
30	20	20	5962-88724 02 KX 5962-88724 02 LX 5962-88724 02 3X	24CW 24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
40	30	25	5962-88724 03 KX 5962-88724 03 LX 5962-88724 03 3X	24CW 24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
20	17	15	5962-89755 04 KX 5962-89755 04 LX 5962-89755 04 3X	24C 24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	18	15	5962-89755 01 KX 5962-89755 01 LX 5962-89755 01 3X	24C 24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
30	20	20	5962-89755 02 KX 5962-89755 02 LX 5962-89755 02 3X	24C 24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
40	30	25	5962-89755 03 KX 5962-89755 03 LX 5962-89755 03 3X	24C 24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant

Package Type	
24DW3	24 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
24C	24 Lead, Non-Windowed, Ceramic Flat Package (Cerpack)
24D3	24 Lead, 0.300" Wide, Non-Windowed (OTP), Ceramic Dual Inline Package (Cerdip)
28J	28 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
28KW	28 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
28LW	28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28L	28 Pad, Non-Windowed, Ceramic Leadless Chip Carrier OTP (LCC)
24P3	24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
24S	24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline OTP (SOIC)
24CW	24 Lead, Windowed, Ceramic Flat Package (Cerpack)

tPD (ns)	tS (ns)	tOH (ns)	Ordering Code	Package	Operation Range
35	25	15	AT22V10L-35DJ AT22V10L-35FJ AT22V10L-35GJ AT22V10L-35JJ AT22V10L-35KJ AT22V10L-35LJ AT22V10L-35NJ AT22V10L-35PJ AT22V10L-35SJ AT22V10L-35VJ	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24S 24CW	Industrial (-40°C to 85°C)
20	17	15	5962-88724 04 KX 5962-88724 04 LX 5962-88724 04 3X	24CW 24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	15	15	5962-88724 01 KX 5962-88724 01 LX 5962-88724 01 3X	24CW 24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
20	20	20	5962-88724 02 KX 5962-88724 02 LX 5962-88724 02 3X	24CW 24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
40	30	25	5962-88724 03 KX 5962-88724 03 LX 5962-88724 03 3X	24CW 24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
20	17	15	5962-89755 04 KX 5962-89755 04 LX 5962-89755 04 3X	24C 24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	18	15	5962-89755 01 KX 5962-89755 01 LX 5962-89755 01 3X	24C 24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
20	20	20	5962-89755 02 KX 5962-89755 02 LX 5962-89755 02 3X	24C 24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
40	30	25	5962-89755 03 KX 5962-89755 03 LX 5962-89755 03 3X	24C 24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant

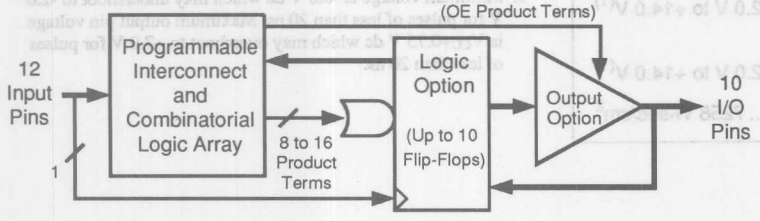
Package Type	
24DW3	24 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
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24S	24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline OTP (EIAJ)
24CW	24 Lead, Windowed, Ceramic Flat Package (Cerpack)

High Speed UV Erasable Programmable Logic Device

Features

- **High Performance Programmable Logic Device**
  - **7.5 ns Max Propagation Delay**
  - **Up to 166 MHz Operation**
  - **5 V ± 10% Operation**
- **Fully Compatible with Standard 22V10**
  - **Identical Functionality/Fuse-Map**
- **CMOS and TTL Compatible Inputs and Outputs**
  - **10 µA Leakage Maximum**
- **Reprogrammable - Tested 100% for Programmability**
- **High Reliability**
  - **Proven UV Erasable CMOS Technology**
  - **2000 V ESD Protection**
- **Full Military, Commercial and Industrial Temperature Ranges**
- **Dual-In-Line and Surface Mount Packages with Standard Pinouts**

Logic Diagram



Description

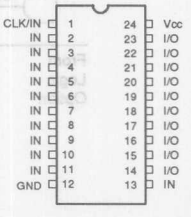
The AT22V10B is an ultra-high performance CMOS Erasable Programmable Logic Device (EPLD). Speeds down to 7.5 ns and operation up to 166 MHz are offered. All pins offer a low ± 10 µA leakage.

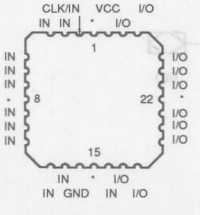
The AT22V10B logic functionality is fully compatible with the standard 22V10. The 12 dedicated inputs and ten configurable I/O pins allow implementation of logic requiring up to 22 input signals. The AT22V10B also provides individual output enable product terms for each of the ten I/Os.

Continued on next page.

Pin Configurations

Pin Name	Function
CLK/IN	Clock and Logic Input
IN	Logic Inputs
I/O	Bidirectional Buffers
*	No Internal Connection
VCC	+5 V Supply





Description (Continued)

The AT22V10B incorporates a variable product term architecture. Each output is allocated from eight to 16 product terms, which allows highly complex logic functions to be realized.

The AT22V10B includes two additional product terms to provide synchronous preset and asynchronous reset. These terms are common to all ten registers. All registers are automatically cleared upon power up.

Register Preload simplifies testing. A Security Fuse prevents unauthorized copying of programmed fuse patterns.

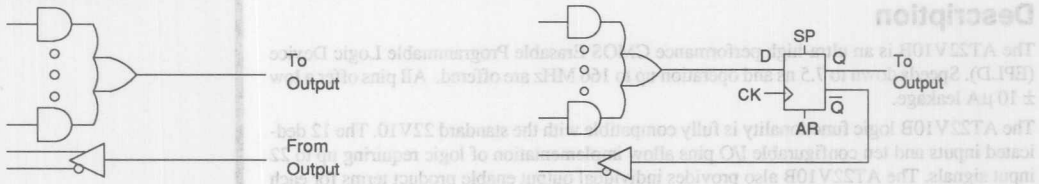
Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0 V to +14.0 V(1)
Programming Voltage with Respect to Ground	-2.0 V to +14.0 V(1)
Integrated UV Erase Dose	7258 W·sec/cm^2

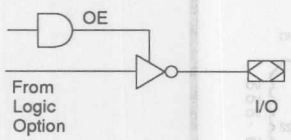
*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

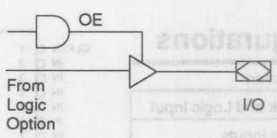
Note:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC}+0.75 V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

Logic Options



Output Options





D.C. and A.C. Operating Conditions

	Commercial AT22V10B -7	Commercial AT22V10B -10, -12	Industrial AT22V10B -10, -12	Military AT22V10B -10, -12
Operating Temperature (Case)	0°C - 70°C	0°C - 70°C	-40°C - 85°C	-55°C - 125°C
V_{CC} Power Supply	5 V ± 5%	5 V ± 10%	5 V ± 10%	5 V ± 10%

Operating Modes

Mode	24-Pin DIP / 28- Pin JLCC	1 / 2	5 / 6	8 / 10	13 / 16	I/O's	Vcc(24) / Vcc(28)
"EPLD"		X (1)	X	X	X	I/O	5V
Program		V_{PP}	X / V_H (2)	X	V_{PP}	D_{IN}	6V
PGM Verify		V_{PP}	X/V_H	X	V_{IL}	D_{OUT}	6V
PGM Inhibit		V_{PP}	X/V_H	X	V_{IH}	High Z	6V
Preload		X	X	V_H	X	D_{IN}	5V

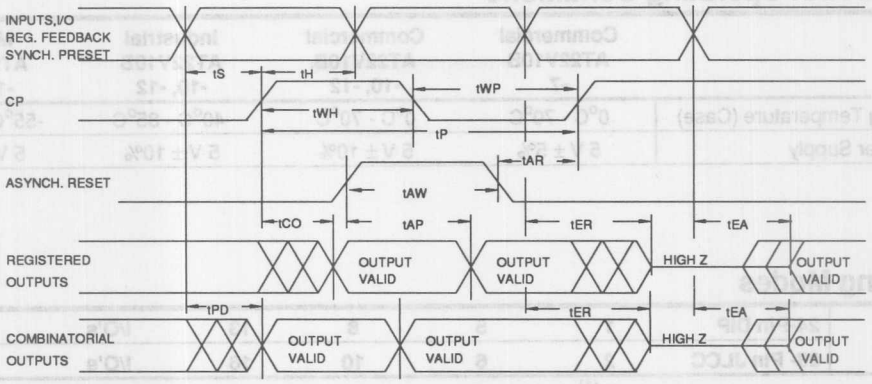
Notes: 1. X can be V_{IL} or V_{IH}. 2. V_H = 11.0 V to 14.0 V

D.C. Characteristics

Symbol	Parameter	Condition			Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1 V to V_{CC}+1 V				10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1 V to V_{CC}+0.1 V				10	µA
I_{CC}	Power Supply Current	V_{CC} = MAX, V_{IN} = GND, Outputs Open		Com.		140	mA
				Ind., Mil.		160	mA
I_{OS} (1)	Output Short Circuit Current	V_{OUT} = 0.5 V			-30	-120	mA
V_{IL}	Input Low Voltage				-0.6	0.8	V
V_{IH}	Input High Voltage				2.0	V_{CC}+0.75	V
V_{OL}	Output Low Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = MIN	I_{OL} = 16 mA	Com.,Ind.		0.5	V
			I_{OL} = 12 mA	Mil.		0.5	V
			I_{OL} = 24 mA	Com.		0.8	V
V_{OH}	Output High Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = MIN	I_{OH} = -4.0 mA		2.4		V

Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.

A.C. Waveforms [1]



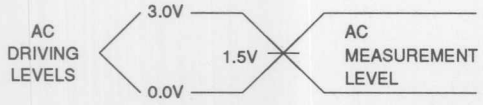
Note: 1. Timing measurement reference is 1.5 V. Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.

A.C. Characteristics

Symbol	Parameter	AT22V10B-7			AT22V10B-10			AT22V10B-12			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PD}	Input or Feedback to Non-Registered Output		5	7.5		6	10		7	12	ns
t_{EA}	Input to Output Enable		5	7.5		6	10		7	12	ns
t_{ER}	Input to Output Disable		5	7.5		6	10		7	12	ns
t_{CF} [1]	Clock to Feedback	0	1	2	0	1	2	0	1.5	2	ns
t_{CO}	Clock to Output	0	3.5	6.0	0	4	7	0	5	7.5	ns
t_S	Input or Feedback Setup Time	4	2.5		5	3		6	5		ns
t_H	Hold Time	0			0			0			ns
t_P	Clock Period	6			7			8			ns
t_{WL} [1]	Clock Width Low	3			3.5			4			ns
t_{WH}	Clock Width High	3			3.5			4			ns
F_{MAX}	External Feedback 1/(ts+tCO)			100			83			74	MHz
	Internal Feedback 1/(ts + tCF)			166			142			125	MHz
	No Feedback 1/(tp)			166			142			125	MHz
t_{AW}	Asynchronous Reset Width	6	3		7	4		8	5		ns
t_{AR}	Asynchronous Reset, Synchronous Preset, Recovery Time	7.5	4		8	5		8.5	5		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		7	13		8	14		9	15	ns

Note: 1. This parameter is only sampled and is not 100% tested.

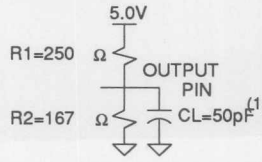
Input Test Waveforms and Measurement Levels



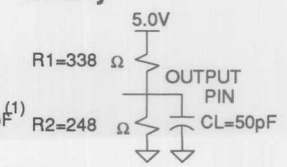
tR, tF < 2 ns (10% to 90%)

Output Test Loads:

Commercial

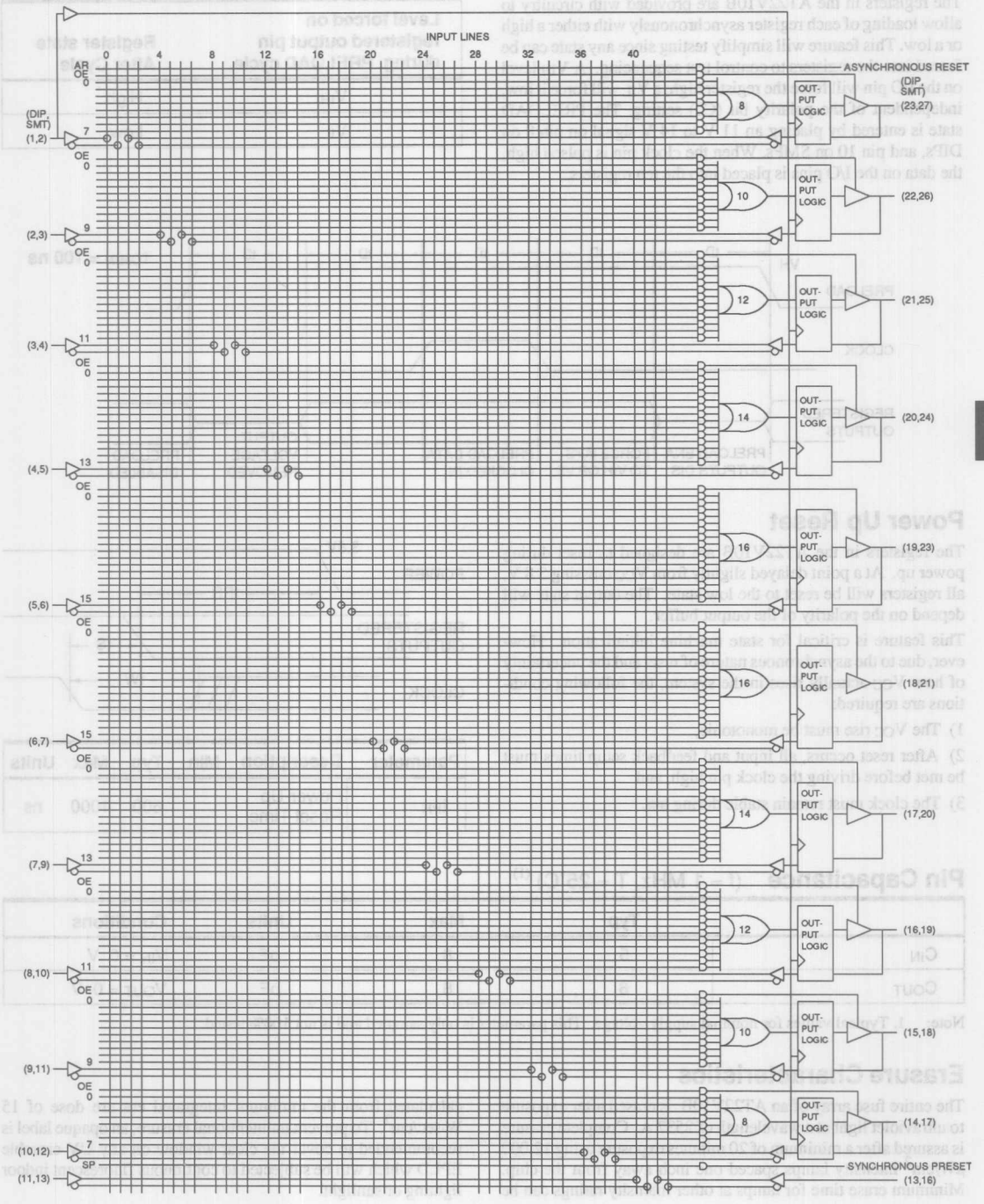


Military



Note: 1. CL = 30 pF for AT22V10B-7

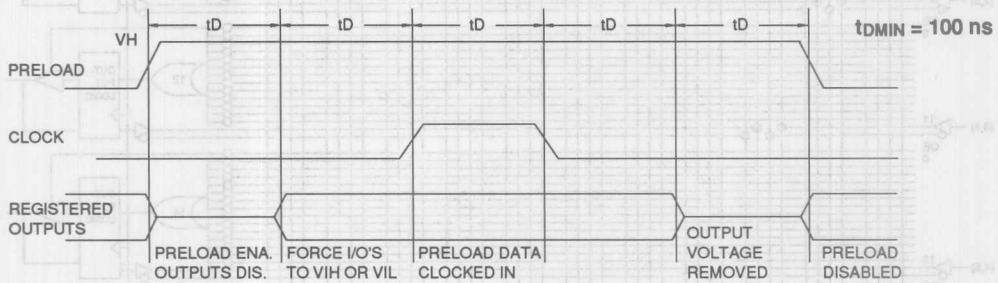
Functional Logic Diagram AT22V10B



Preload of Registered Outputs

The registers in the AT22V10B are provided with circuitry to allow loading of each register asynchronously with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A V_{IH} level on the I/O pin will force the register high; a V_{IL} will force it low, independent of the polarity bit (C0) setting. The PRELOAD state is entered by placing an 11 V to 14 V signal on pin 8 on DIPs, and pin 10 on SMPs. When the clock pin is pulsed high, the data on the I/O pins is placed into the ten registers.

Level forced on registered output pin during PRELOAD cycle.	Register state After Cycle
V_{IH}	High
V_{IL}	Low



Power Up Reset

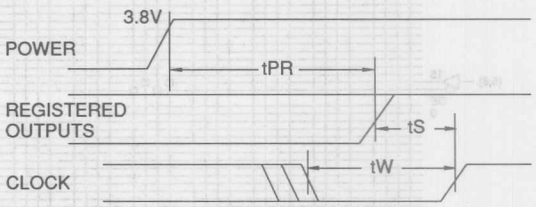
The registers in the AT22V10B are designed to reset during power up. At a point delayed slightly from V_{CC} crossing 3.8 V, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1) The V_{CC} rise must be monotonic,

2) After reset occurs, all input and feedback setup times must be met before driving the clock pin high, and

3) The clock must remain stable during t_{PR}.



Parameter	Description	Min	Typ	Max	Units
t_{PR}	Power-Up Reset Time		600	1000	ns

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	5	8	pF	V_{IN} = 0 V
C_{OUT}	6	8	pF	V_{OUT} = 0 V

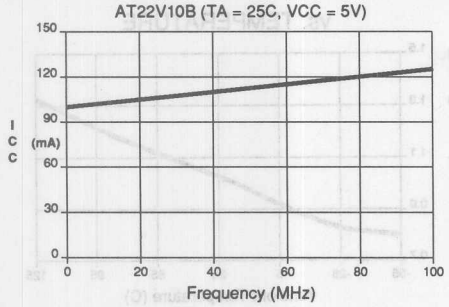
Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Erasure Characteristics

The entire fuse array of an AT22V10B is erased after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 $W \cdot sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPLD which will be subjected to continuous fluorescent indoor lighting or sunlight.

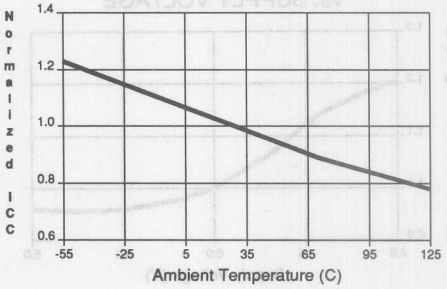
SUPPLY CURRENT vs. INPUT FREQUENCY

AT22V10B (TA = 25C, VCC = 5V)

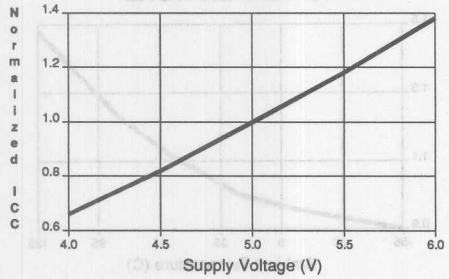


NORMALIZED ICC vs. AMBIENT TEMP.

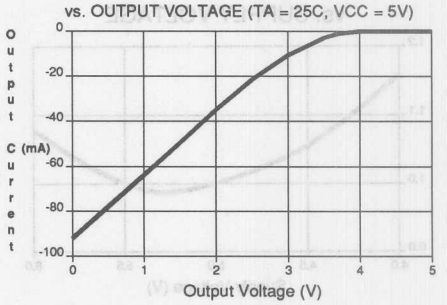
f = 50 MHz



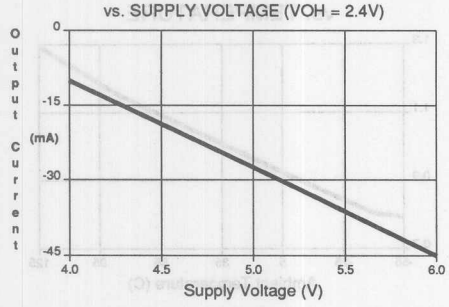
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



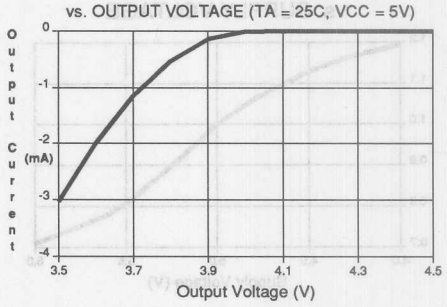
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE (TA = 25C, VCC = 5V)



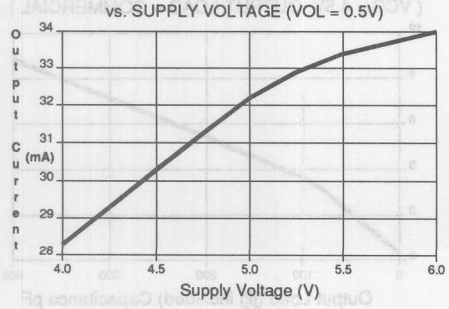
OUTPUT SOURCE CURRENT vs. SUPPLY VOLTAGE (VOH = 2.4V)



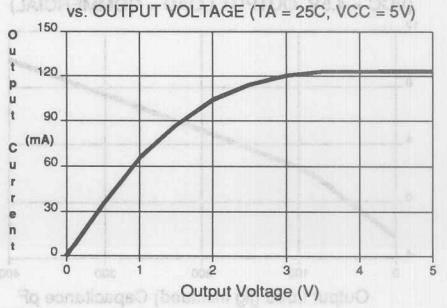
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE (TA = 25C, VCC = 5V)



OUTPUT SINK CURRENT vs. SUPPLY VOLTAGE (VOL = 0.5V)

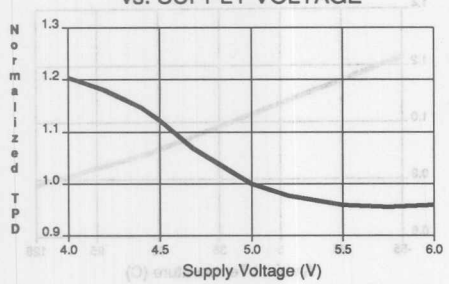


OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE (TA = 25C, VCC = 5V)

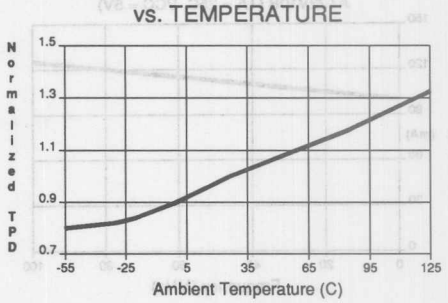


7

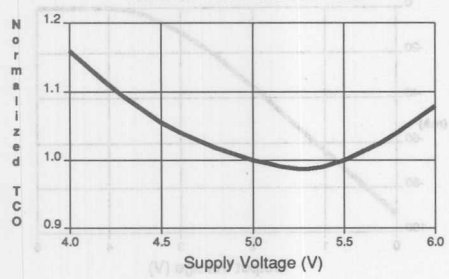
NORMALIZED TPD vs. SUPPLY VOLTAGE



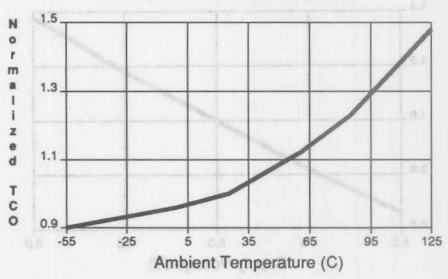
NORMALIZED TPD vs. TEMPERATURE



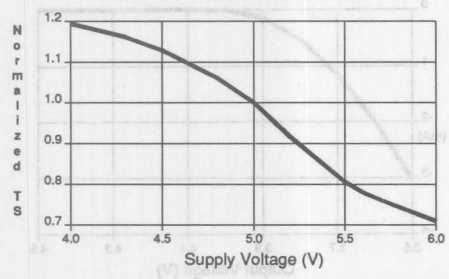
NORMALIZED TCO vs. SUPPLY VOLTAGE



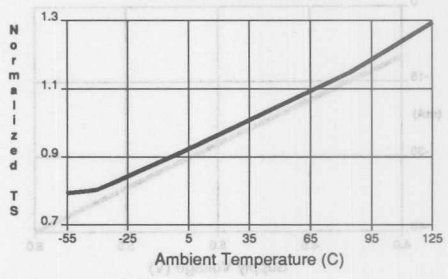
NORMALIZED TCO vs. TEMPERATURE



NORMALIZED TS vs. SUPPLY VOLTAGE

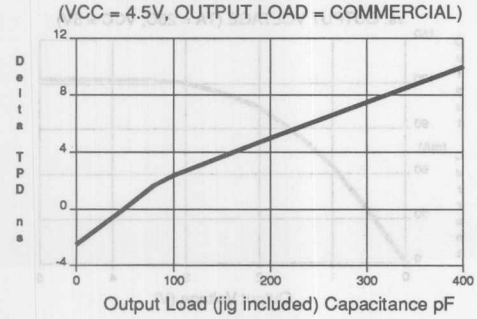


NORMALIZED TS vs. TEMPERATURE



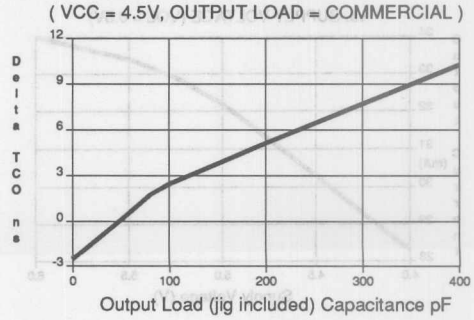
DELTA TPD vs. OUTPUT LOADING

(VCC = 4.5V, OUTPUT LOAD = COMMERCIAL)



DELTA TCO vs. OUTPUT LOADING

(VCC = 4.5V, OUTPUT LOAD = COMMERCIAL)



Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
7.5	4	6	AT22V10B-7DC	24DW3	Commercial (0°C to 70°C)
			AT22V10B-7GC	24D3	
			AT22V10B-7JC	28J	
			AT22V10B-7KC	28KW	
			AT22V10B-7LC	28LW	
			AT22V10B-7NC	28L	
			AT22V10B-7PC	24P3	
			AT22V10B-7SC	24S	
10	5	7	AT22V10B-10DC	24DW3	Commercial (0°C to 70°C)
			AT22V10B-10GC	24D3	
			AT22V10B-10JC	28J	
			AT22V10B-10KC	28KW	
			AT22V10B-10LC	28LW	
			AT22V10B-10NC	28L	
			AT22V10B-10PC	24P3	
			AT22V10B-10SC	24S	
			AT22V10B-10DI	24DW3	Industrial (-40°C to 85°C)
			AT22V10B-10GI	24D3	
			AT22V10B-10JI	28J	
			AT22V10B-10KI	28KW	
			AT22V10B-10LI	28LW	
			AT22V10B-10NI	28L	
			AT22V10B-10PI	24P3	
			AT22V10B-10SI	24S	
			AT22V10B-10DM	24DW3	Military (-55°C to 125°C)
			AT22V10B-10GM	24D3	
			AT22V10B-10KM	28KW	
			AT22V10B-10LM	28LW	
			AT22V10B-10NM	28L	
			AT22V10B-10DM/883	24DW3	Military/883C (-55°C to 125°C) Class B, Fully Compliant
			AT22V10B-10GM/883	24D3	
			AT22V10B-10KM/883	28KW	
			AT22V10B-10LM/883	28LW	
			AT22V10B-10NM/883	28L	
12	6	7.5	AT22V10B-12DC	24DW3	Commercial (0°C to 70°C)
			AT22V10B-12GC	24D3	
			AT22V10B-12JC	28J	
			AT22V10B-12KC	28KW	
			AT22V10B-12LC	28LW	
			AT22V10B-12NC	28L	
			AT22V10B-12PC	24P3	
			AT22V10B-12SC	24S	
			AT22V10B-12DI	24DW3	Industrial (-40°C to 85°C)
			AT22V10B-12GI	24D3	
			AT22V10B-12JI	28J	
			AT22V10B-12KI	28KW	
			AT22V10B-12LI	28LW	
			AT22V10B-12NI	28L	
			AT22V10B-12PI	24P3	
			AT22V10B-12SI	24S	

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Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
12	6	7.5	AT22V10B-12DM AT22V10B-12GM AT22V10B-12KM AT22V10B-12LM AT22V10B-12NM	24DW3 24D3 28KW 28LW 28L	Military (-55°C to 125°C)
			AT22V10B-12DM/883 AT22V10B-12GM/883 AT22V10B-12KM/883 AT22V10B-12LM/883 AT22V10B-12NM/883	24DW3 24D3 28KW 28LW 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant

Package Type	
24DW3	24 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
24D3	24 Lead, 0.300" Wide, Non-Windowed (OTP), Ceramic Dual Inline Package (Cerdip)
28J	28 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
28KW	28 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
28LW	28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28L	28 Pad, Non-Windowed, Ceramic Leadless Chip Carrier OTP (LCC)
24P3	24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
24S	24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline OTP (SOIC)

Features

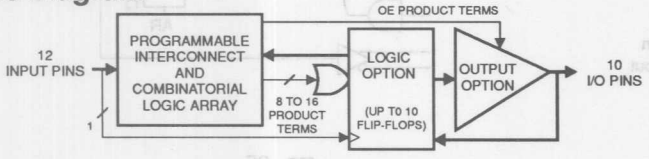
- **Low Voltage Programmable Logic Device**
  - **Wide Power Supply Range - 3.0 V to 5.5 V**
  - **Ideal for Battery Powered Systems**
- **High Speed Operation**
  - **20 ns max Propagation Delay at V_{CC} = 3.0 V**
- **Full Military, Commercial and Industrial Temperature Ranges**
- **Familiar 22V10 Logic Architecture**
- **Low Power 3-Volt CMOS Operation**

	AT22LV10L	AT22LV10
Temp	Com./Mil.	Com./Mil.
I_{CC} (mA)	4 / 5	35 / 45

V_{CC} = 3.6 V

- **CMOS and TTL Compatible Inputs and Outputs**
  - **10 µA Leakage Maximum**
- **Reprogrammable - Tested 100% for Programmability**
- **High Reliability CMOS Technology**
  - **2000 V ESD Protection**
  - **200 mA Latchup Immunity**
- **Dual-In-Line and Surface Mount Packages**

Logic Diagram



Description

The AT22LV10 and AT22LV10L are low voltage compatible CMOS high performance Erasable Programmable Logic Devices (EPLDs). Speeds down to 20 ns and power dissipation as low as 14.4 mW are offered. All speed ranges are specified over the 3.0 V to 5.5 V range. All pins offer a low ±10 µA leakage.

The AT22LV10L provides the optimum low power CMOS EPLD solution, with low DC power (1 mA typical at V_{CC} = 3.3 V) and full CMOS output levels. The AT22LV10L significantly reduces total system power, allowing battery powered operation.

Full CMOS output levels help reduce power in many other system components.

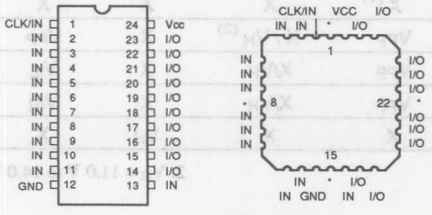
The AT22LV10 and AT22LV10L logic architectures are identical to the familiar 22V10. Each output is allocated from eight to 16 product terms, which allows highly complex logic functions to be realized.

Two additional product terms are included to provide synchronous preset and asynchronous reset. These terms are common to all ten registers. All registers are automatically cleared upon power up.

Register Preload simplifies testing. A Security Fuse prevents unauthorized copying of programmed fuse patterns.

Pin Configurations

Pin Name	Function
CLK/IN	Clock and Logic Input
IN	Logic Inputs
I/O	Bidirectional Buffers
*	No Internal Connection
VCC	3.0 V to 5.5 V Supply



Low Voltage UV Erasable Programmable Logic Device

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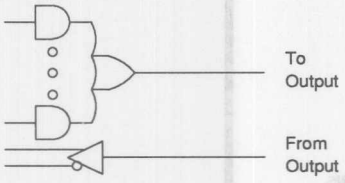
Absolute Maximum Ratings*

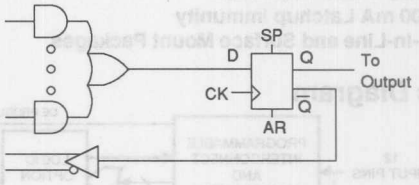
Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0 V to +14.0 V(1)
Programming Voltage with Respect to Ground	-2.0 V to +14.0 V(1)
Integrated UV Erase Dose	7258 W·sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

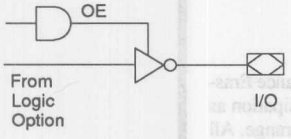
Note:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum pin voltage is V_{CC}+0.75 V dc which may overshoot to V_{CC} +2.0 V for pulses of less than 20 ns.

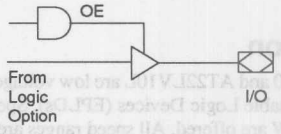
Logic Options





Output Options





D.C. and A.C. Operating Conditions

	Commercial AT22LV10/L -20, -25, -30	Industrial AT22LV10/L -20, -25, -30	Military AT22LV10/L -25, -30, -35
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C	-55°C - 125°C
V_{CC} Power Supply	3.0 V to 5.5 V	3.0 V to 5.5 V	3.0 V to 5.5 V

Operating Modes

	24-Pin DIP	1	5	8	13	I/Os	Vcc (24)
Mode	28-Pin JLCC	2	6	10	16	I/Os	Vcc (28)
"EPLD"		X(1)	X	X	X	I/O	3.0 V to 5.5 V
Program		V_{PP}	X / V_H (2)	X	V_{PP}	D_{IN}	6 V
PGM Verify		V_{PP}	X/V_H	X	V_{IL}	D_{OUT}	6 V
PGM Inhibit		V_{PP}	X/V_H	X	V_{IH}	High Z	6 V
Preload		X	X	V_H	X	D_{IN}	3.0 V to 5.5 V

Notes: 1. X can be V_{IL} or V_{IH}. 2. V_H = 11.0 V to 14.0 V

D.C. Characteristics

Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1 V to V_{CC}+1 V					10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1 V to V_{CC}+0.1 V					10	µA
I_{CC}	Power Supply Current	V_{CC} = 3.6 V / 5.5 V, V_{IN} = GND, Outputs Open	AT22LV10	Com.		20/50	35/90	mA
				Ind., Mil.		20/50	45/100	mA
			AT22LV10L(2)	Com.		1/2	4/12	mA
				Ind., Mil.		1/2	5/15	mA
I_{CC2}	Clocked Power Supply Current	f = 1 MHz, V_{CC} = 3.6 V / 5.5 V, Outputs Open	AT22LV10L(2)	Com.		3/5	7/15	mA
				Ind., Mil.		3/5	10/20	mA
I_{OS} (1)	Output Short Circuit Current	V_{OUT} = 0.5 V					-90	mA
V_{IL1}	Input Low Voltage	4.5 V ≤ V_{CC} ≤ 5.5 V			-0.6		0.8	V
V_{IL2}	Input Low Voltage	3.0 V ≤ V_{CC} < 4.5 V			-0.6		0.6	V
V_{IH}	Input High Voltage				2.0		V_{CC}+0.75	V
V_{OL}	Output Low Voltage V_{IN} = V_{IH} or V_{IL}	V_{CC} = 3.0 V	Com.,Ind./Mil.	I_{OL} = 8 mA / 6 mA			0.5	V
		V_{CC} = 4.5 V	Com.,Ind./Mil.	I_{OL} = 16 mA / 12 mA			0.5	V
		V_{CC} = 3.0 V	Com.,Ind./Mil.	I_{OL} = 6 mA / 4 mA			0.35	V
V_{OH}	Output High Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = 3.0 V / 4.5 V	I_{OH} = -100 µA		V_{CC}-0.3			V
			I_{OH} = -0.4 mA / -4.0 mA		2.4			V

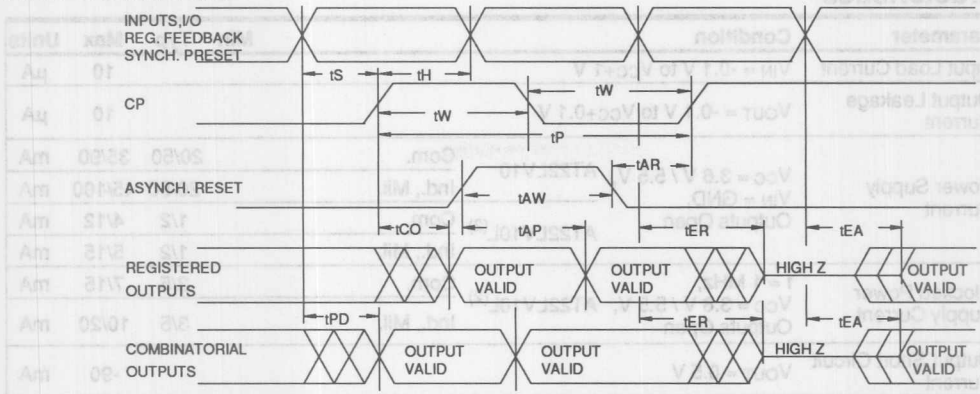
Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.

2. See I_{CC} vs. Frequency curves in the back of this data sheet.

A.C. Characteristics for the AT22LV10

		AT22LV10-20			AT22LV10-25			AT22LV10-30			
Symbol	Parameter	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
t_{PD}	Input or Feedback to Non-Registered Output		12	20		15	25		20	30	ns
t_{EA}	Input to Output Enable			20		15	25		20	30	ns
t_{ER}	Input to Output Disable			20		15	25		20	30	ns
t_{CF}	Clock to Feedback	0	4	9	0	5	9	0	6	10	ns
t_{CO}	Clock to Output	0	8	14	0	10	17	0	12	20	ns
t_S	Input or Feedback Setup Time	10	6		12	7		15	8		ns
t_H	Hold Time	0			0			0			ns
t_P	Clock Period	10			12			14			ns
t_W	Clock Width	5			6			7			ns
F_{MAX}	External Feedback 1/(t_S+t_{CO})			41.6			34.5			28.5	MHz
	Internal Feedback 1/(t_S + t_{CF})			52.6			47.6			40.0	MHz
	No Feedback 1/(t_P)			100.0			83.3			71.4	MHz
t_{AW}	Asynchronous Reset Width	20	12		25	15		30	18		ns
t_{AR}	Asynchronous Reset, Synchronous Preset, Recovery Time	20	12		25	15		30	18		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		15	25		18	28		20	30	ns

A.C. Waveforms[1]

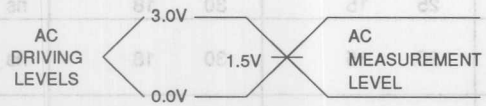


Note: 1. Timing measurement reference is 1.5 V. Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.

A.C. Characteristics for the AT22LV10L

Symbol	Parameter	AT22LV10L-25			AT22LV10L-30			AT22LV10L-35			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PD}	Input or Feedback to Non-Registered Output		15	25		20	30		25	35	ns
t_{EA}	Input to Output Enable		15	25		20	30		25	35	ns
t_{ER}	Input to Output Disable		15	25		20	30		25	35	ns
t_{CF}	Clock to Feedback	0	5	9	0	6	10		7	11	ns
t_{CO}	Clock to Output	0	10	14	0	12	17		15	20	ns
t_{SF}	Feedback Setup Time	12	7		15	10		18	12		ns
t_S	Input Setup Time	17	15		20	15		22	15		ns
t_H	Hold Time	0			0			0			ns
t_P	Clock Period	12			14			16			ns
t_W	Clock Width	6			7			8			ns
F_{MAX}	External Feedback $1/(t_S+t_{CO})$			32.2			27.0			23.8	MHz
	Internal Feedback $1/(t_{SF}+t_{CF})$			47.6			40.0			34.4	MHz
	No Feedback $1/(t_P)$			83.3			71.4			62.5	MHz
t_{AW}	Asynchronous Reset Width	25	15		30	18		35	20		ns
t_{AR}	Asynchronous Reset Recovery Time	25	15		30	18		35	20		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		18	28		20	30		22	35	ns

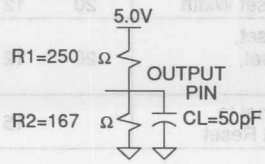
Input Test Waveforms and Measurement Levels



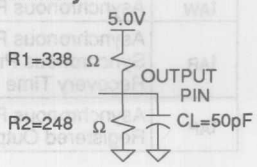
tR, tF < 5 ns (10% to 90%)

Output Test Loads:

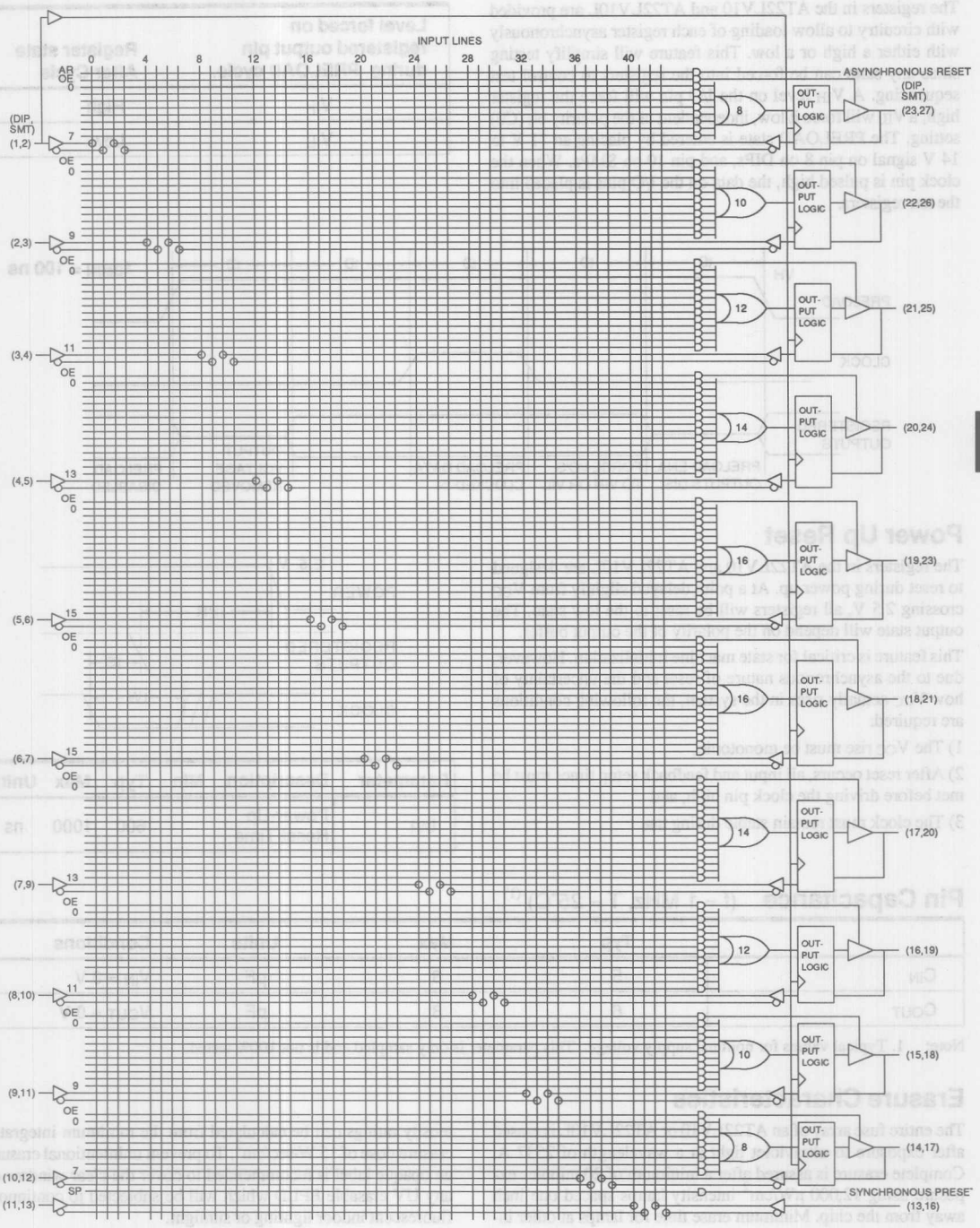
Commercial



Military



Functional Logic Diagram AT22LV10/L

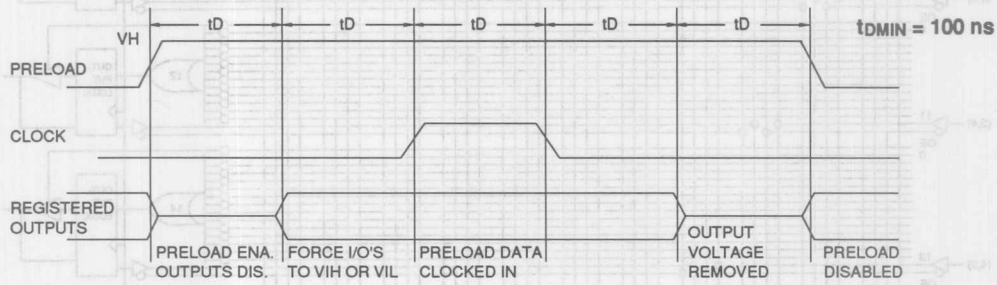


7

Preload of Registered Outputs

The registers in the AT22LV10 and AT22LV10L are provided with circuitry to allow loading of each register asynchronously with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A V_{IH} level on the I/O pin will force the register high; a V_{IL} will force it low, independent of the polarity bit (C0) setting. The PRELOAD state is entered by placing an 11 V to 14 V signal on pin 8 on DIPs, and pin 10 on SMPs. When the clock pin is pulsed high, the data on the I/O pins is placed into the ten registers.

Level forced on registered output pin during PRELOAD cycle.	Register state After Cycle
V_{IH}	High
V_{IL}	Low



Power Up Reset

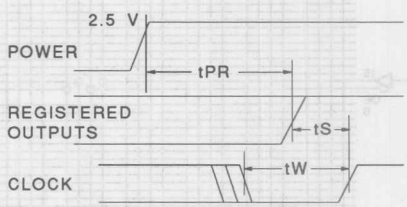
The registers in the AT22LV10 and AT22LV10L are designed to reset during power up. At a point delayed slightly from V_{CC} crossing 2.5 V, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1) The V_{CC} rise must be monotonic,

2) After reset occurs, all input and feedback setup times must be met before driving the clock pin high, and

3) The clock must remain stable during t_{PR}.



Parameter	Description	Min	Typ	Max	Units
t_{PR}	Power-Up Reset Time		600	1000	ns

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	5	8	pF	V_{IN} = 0 V
C_{OUT}	6	8	pF	V_{OUT} = 0 V

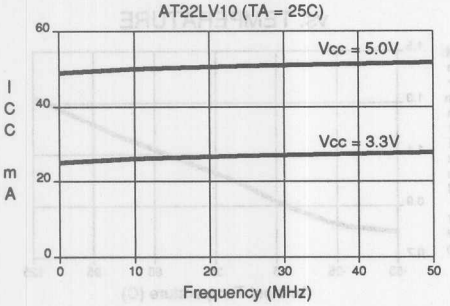
Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Erasure Characteristics

The entire fuse array of an AT22LV10 or AT22LV10L is erased after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 $W \cdot sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPLD which will be subjected to continuous fluorescent indoor lighting or sunlight.

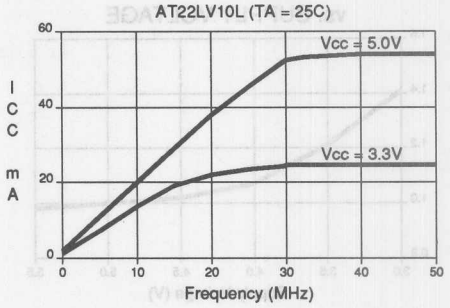
SUPPLY CURRENT vs. INPUT FREQUENCY

AT22LV10 (TA = 25C)

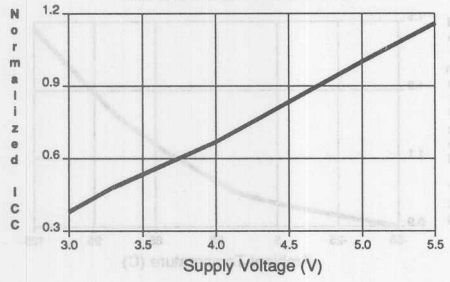


SUPPLY CURRENT vs. INPUT FREQUENCY

AT22LV10L (TA = 25C)

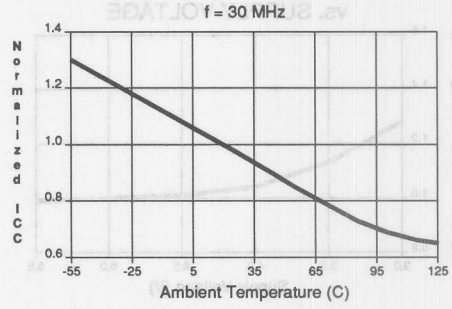


NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



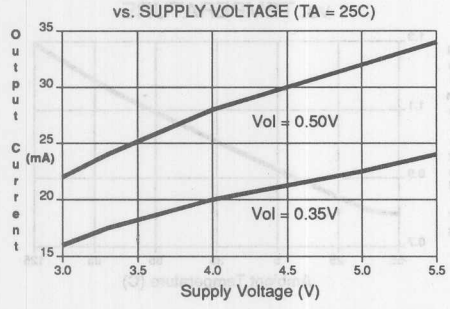
NORMALIZED ICC vs. AMBIENT TEMP.

f = 30 MHz



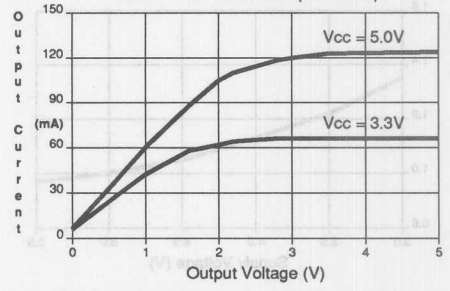
OUTPUT SINK CURRENT

vs. SUPPLY VOLTAGE (TA = 25C)



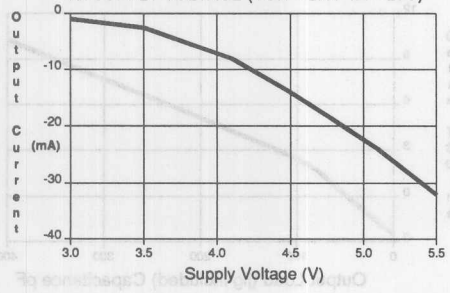
OUTPUT SINK CURRENT

vs. OUTPUT VOLTAGE (TA = 25C)



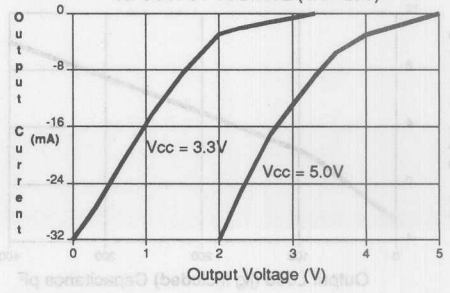
OUTPUT SOURCE CURRENT

vs. SUPPLY VOLTAGE (VOH = 2.4V TA = 25C)



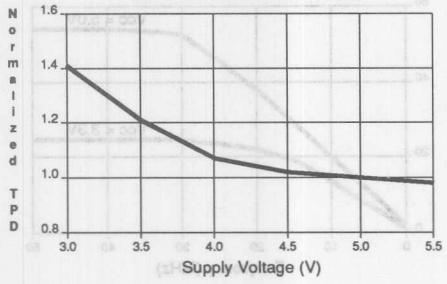
OUTPUT SOURCE CURRENT

vs. OUTPUT VOLTAGE (TA = 25C)

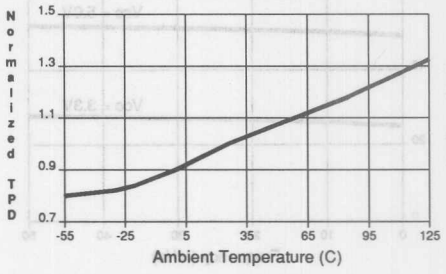


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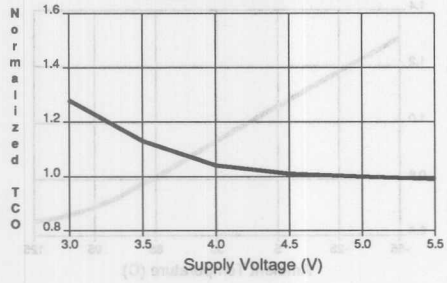
NORMALIZED TPD vs. SUPPLY VOLTAGE



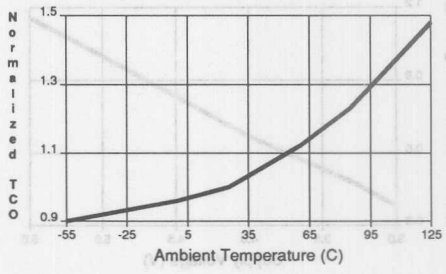
NORMALIZED TPD vs. TEMPERATURE



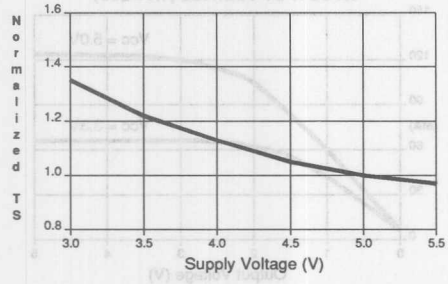
NORMALIZED TCO vs. SUPPLY VOLTAGE



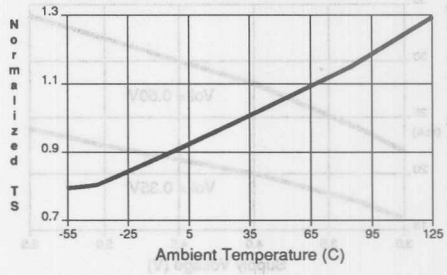
NORMALIZED TCO vs. TEMPERATURE



NORMALIZED TS vs. SUPPLY VOLTAGE

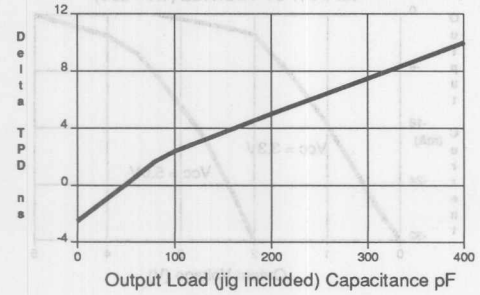


NORMALIZED TS vs. TEMPERATURE



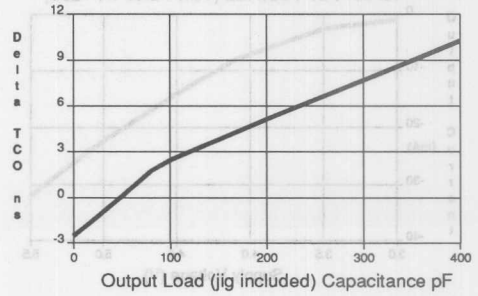
DELTA TPD vs. OUTPUT LOADING

(VCC = 4.5V, OUTPUT LOAD = COMMERCIAL)



DELTA TCO vs. OUTPUT LOADING

(VCC = 4.5V, OUTPUT LOAD = COMMERCIAL)



Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
20	10	14	AT22LV10-20DC	24DW3	Commercial (0°C to 70°C)
			AT22LV10-20FC	24C	
			AT22LV10-20GC	24D3	
			AT22LV10-20JC	28J	
			AT22LV10-20KC	28KW	
			AT22LV10-20LC	28LW	
			AT22LV10-20NC	28L	
			AT22LV10-20PC	24P3	
			AT22LV10-20SC	24S	
			AT22LV10-20YC	24CW	
			AT22LV10-20DI	24DW3	Industrial (-40°C to 85°C)
			AT22LV10-20FI	24C	
			AT22LV10-20GI	24D3	
			AT22LV10-20JI	28J	
			AT22LV10-20KI	28KW	
			AT22LV10-20LI	28LW	
			AT22LV10-20NI	28L	
			AT22LV10-20PI	24P3	
			AT22LV10-20SI	24S	
			AT22LV10-20YI	24CW	
			AT22LV10-20DM	24DW3	Military (-55°C to 125°C)
			AT22LV10-20FM	24C	
			AT22LV10-20GM	24D3	
			AT22LV10-20KM	28KW	
			AT22LV10-20LM	28LW	
			AT22LV10-20NM	28L	
			AT22LV10-20YM	24CW	
			AT22LV10-20DM/883	24DW3	Military/883D (-55°C to 125°C) Class B, Fully Compliant
			AT22LV10-20FM/883	24C	
			AT22LV10-20GM/883	24D3	
			AT22LV10-20KM/883	28KW	
			AT22LV10-20LM/883	28LW	
			AT22LV10-20NM/883	28L	
			AT22LV10-20YM/883	24CW	
25	12	17	AT22LV10-25DC	24DW3	Commercial (0°C to 70°C)
			AT22LV10-25FC	24C	
			AT22LV10-25GC	24D3	
			AT22LV10-25JC	28J	
			AT22LV10-25KC	28KW	
			AT22LV10-25LC	28LW	
			AT22LV10-25NC	28L	
			AT22LV10-25PC	24P3	
			AT22LV10-25SC	24S	
			AT22LV10-25YC	24CW	

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Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
25	12	17	AT22LV10-25DI	24DW3	Industrial (-40°C to 85°C)
			AT22LV10-25FI	24C	
			AT22LV10-25GI	24D3	
			AT22LV10-25JI	28J	
			AT22LV10-25KI	28KW	
			AT22LV10-25LI	28LW	
			AT22LV10-25NI	28L	
			AT22LV10-25PI	24P3	
			AT22LV10-25SI	24S	
			AT22LV10-25YI	24CW	
			AT22LV10-25DM	24DW3	Military (-55°C to 125°C)
			AT22LV10-25FM	24C	
			AT22LV10-25GM	24D3	
			AT22LV10-25KM	28KW	
			AT22LV10-25LM	28LW	
			AT22LV10-25NM	28L	
			AT22LV10-25YM	24CW	
			AT22LV10-25DM/883	24DW3	Military/883D (-55°C to 125°C) Class B, Fully Compliant
			AT22LV10-25FM/883	24C	
			AT22LV10-25GM/883	24D3	
			AT22LV10-25KM/883	28KW	
			AT22LV10-25LM/883	28LW	
			AT22LV10-25NM/883	28L	
			AT22LV10-25YM/883	24CW	
30	15	20	AT22LV10-30DC	24DW3	Commercial (0°C to 70°C)
			AT22LV10-30FC	24C	
			AT22LV10-30GC	24D3	
			AT22LV10-30JC	28J	
			AT22LV10-30KC	28KW	
			AT22LV10-30LC	28LW	
			AT22LV10-30NC	28L	
			AT22LV10-30PC	24P3	
			AT22LV10-30SC	24S	
			AT22LV10-30YC	24CW	
			AT22LV10-30DI	24DW3	Industrial (-40°C to 85°C)
			AT22LV10-30FI	24C	
			AT22LV10-3GI	24D3	
			AT22LV10-30JI	28J	
			AT22LV10-30KI	28KW	
			AT22LV10-30LI	28LW	
			AT22LV10-30NI	28L	
			AT22LV10-30PI	24P3	
			AT22LV10-30SI	24S	
			AT22LV10-30YI	24CW	

Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
30	15	20	AT22LV10-30DM AT22LV10-30FM AT22LV10-30GM AT22LV10-30KM AT22LV10-30LM AT22LV10-30NM AT22LV10-30YM	24DW3 24C 28D3 28KW 28LW 28L 24CW	Military (-55°C to 125°C)
			AT22LV10-30DM/883 AT22LV10-30FM/883 AT22LV10-30GM/883 AT22LV10-30KM/883 AT22LV10-30LM/883 AT22LV10-30NM/883 AT22LV10-30YM/883	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military/883D (-55°C to 125°C) Class B, Fully Compliant

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Package Type	
24DW3	24 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
24C	24 Lead, Non-Windowed, Ceramic Flat Package (Cerpack)
24D3	24 Lead, 0.300" Wide, Non-Windowed (OTP), Ceramic Dual Inline Package (Cerdip)
28J	28 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
28KW	28 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
28LW	28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28L	28 Pad, Non-Windowed, Ceramic Leadless Chip Carrier OTP (LCC)
24P3	24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
24S	24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline OTP (SOIC)
24CW	24 Lead, Windowed, Ceramic Flat Package (Cerpack)

Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
25	17	14	AT22LV10L-25DC	24DW3	Commercial (0°C to 70°C)
			AT22LV10L-25FC	24C	
			AT22LV10L-25GC	24D3	
			AT22LV10L-25JC	28J	
			AT22LV10L-25KC	28KW	
			AT22LV10L-25LC	28LW	
			AT22LV10L-25NC	28L	
			AT22LV10L-25PC	24P3	
			AT22LV10L-25SC	24S	
			AT22LV10L-25YC	24CW	
			AT22LV10L-25DI	24DW3	Industrial (-40°C to 85°C)
			AT22LV10L-25FI	24C	
			AT22LV10L-25GI	24D3	
			AT22LV10L-25JI	28J	
			AT22LV10L-25KI	28KW	
			AT22LV10L-25LI	28LW	
			AT22LV10L-25NI	28L	
			AT22LV10L-25PI	24P3	
			AT22LV10L-25SI	24S	
			AT22LV10L-25YI	24CW	
30	20	17	AT22LV10L-30DC	24DW3	Commercial (0°C to 70°C)
			AT22LV10L-30FC	24C	
			AT22LV10L-30GC	24D3	
			AT22LV10L-30JC	28J	
			AT22LV10L-30KC	28KW	
			AT22LV10L-30LC	28LW	
			AT22LV10L-30NC	28L	
			AT22LV10L-30PC	24P3	
			AT22LV10L-30SC	24S	
			AT22LV10L-30YC	24CW	
			AT22LV10L-30DI	24DW3	Industrial (-40°C to 85°C)
			AT22LV10L-30FI	24C	
			AT22LV10L-3GI	24D3	
			AT22LV10L-30JI	28J	
			AT22LV10L-30KI	28KW	
			AT22LV10L-30LI	28LW	
			AT22LV10L-30NI	28L	
			AT22LV10L-30PI	24P3	
			AT22LV10L-30SI	24S	
			AT22LV10L-30YI	24CW	
			AT22LV10L-30DM	24DW3	Military (-55°C to 125°C)
			AT22LV10L-30FM	24C	
			AT22LV10L-30GM	24D3	
			AT22LV10L-30KM	28KW	
			AT22LV10L-30LM	28LW	
			AT22LV10L-30NM	28L	
			AT22LV10L-30YM	24CW	

Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
30	20	17	AT22LV10L-30DM/883	24DW3	Military/883D (-55°C to 125°C) Class B, Fully Compliant
			AT22LV10L-30FM/883	24C	
			AT22LV10L-30GM/883	24D3	
			AT22LV10L-30KM/883	28KW	
			AT22LV10L-30LM/883	28LW	
			AT22LV10L-30NM/883	28L	
			AT22LV10L-30YM/883	24CW	
35	22	20	AT22LV10L-35DC	24DW3	Commercial (0°C to 70°C)
			AT22LV10L-35FC	24C	
			AT22LV10L-35GC	24D3	
			AT22LV10L-35JC	28J	
			AT22LV10L-35KC	28KW	
			AT22LV10L-35LC	28LW	
			AT22LV10L-35NC	28L	
			AT22LV10L-35PC	24P3	
			AT22LV10L-35SC	24S	
			AT22LV10L-35YC	24CW	
			AT22LV10L-35DI	24DW3	Industrial (-40°C to 85°C)
			AT22LV10L-35FI	24C	
			AT22LV10L-35GI	24D3	
			AT22LV10L-35JI	28J	
			AT22LV10L-35KI	28KW	
			AT22LV10L-35LI	28LW	
			AT22LV10L-35NI	28L	
			AT22LV10L-35PI	24P3	
			AT22LV10L-35SI	24S	
			AT22LV10L-35YI	24CW	
			AT22LV10L-35DM	24DW3	Military (-55°C to 125°C)
			AT22LV10L-35FM	24C	
			AT22LV10L-35GM	28D3	
			AT22LV10L-35KM	28KW	
			AT22LV10L-35LM	28LW	
			AT22LV10L-35NM	28L	
			AT22LV10L-35YM	24CW	
			AT22LV10L-35DM/883	24DW3	Military/883D (-55°C to 125°C) Class B, Fully Compliant
			AT22LV10L-35FM/883	24C	
			AT22LV10L-35GM/883	24D3	
			AT22LV10L-35KM/883	28KW	
			AT22LV10L-35LM/883	28LW	
			AT22LV10L-35NM/883	28L	
			AT22LV10L-35YM/883	24CW	

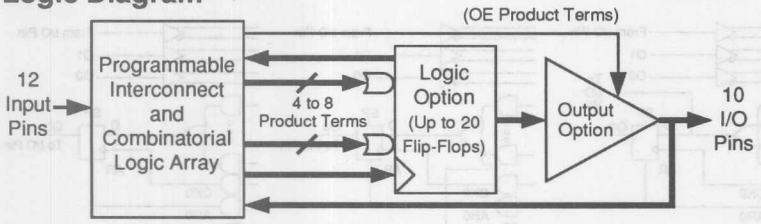
Package Type	
24DW3	24 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
24C	24 Lead, Non-Windowed, Ceramic Flat Package (Cerpack)
24D3	24 Lead, 0.300" Wide, Non-Windowed (OTP), Ceramic Dual Inline Package (Cerdip)
28J	28 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
28KW	28 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
28LW	28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28L	28 Pad, Non-Windowed, Ceramic Leadless Chip Carrier OTP (LCC)
24P3	24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
24S	24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline OTP (SOIC)
24CW	24 Lead, Windowed, Ceramic Flat Package (Cerpack)

High Density UV Erasable Programmable Logic Device

Features

- **Third Generation Programmable Logic Structure**
  - **High Density Replacement for Discrete Logic**
- **High Speed - Plus a New Low Power Version**
- **Increased Logic Flexibility**
  - **42 Inputs and 20 SUM terms**
- **Flexible Output Logic**
  - **20 Flip-Flops - 10 Extra**
  - **All Can Be Individually Buried or 10 Output Directly**
  - **Each has Individual Asynchronous Reset or Clock Terms**
- **Multiple Feedback Paths Provide for Buried State Machines and I/O Bus Compatibility**
- **Proven and Reliable High Speed CMOS EPROM Process**
  - **2000 V ESD Protection**
  - **200 mA Latchup Immunity**
- **Reprogrammable - Tested 100% for Programmability**
- **24-pin, 300-mil Dual-In-line and 28-Lead Surface Mount Packages**

Logic Diagram



Description

The ATV750/L is 100% more powerful than most other programmable logic devices in 24 pin packages. Increased Product terms, SUM Terms, and Flip-Flops translate into more usable gates.

Each of the ATV750's 22 logic pins can be used as an input. Ten of these can be used as input, output, or bi-directional I/O pins. All 20 Flip-Flops can be fed back into the array independently. This flexibility allows burying all of the SUM terms and Flip-Flops.

There are 171 Product Terms available. A variable format is used to assign between four and eight Product Terms per Sum Term. There are two Sum Terms per output, providing added flexibility. Much more logic can be replaced by this one 24-pin device.

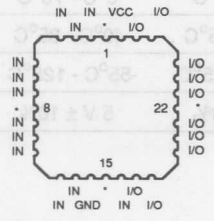
The ATV750/L has more flip-flops available than other EPLDs in this density range. Complex state machines are easily implemented.

Product terms are available providing Asynchronous Resets, Flip-Flop clocks, and Output Enables. One reset and one clock term are provided per Flip-Flop, with one Enable term per output. One product term provides a global synchronous Preset. Register Preload simplifies testing. The device has an internal power up clear function.

Pin Configurations

Pin Name	Function
IN	Logic Inputs
I/O	Bidirectional Buffers
*	No Internal Connection
VCC	+5V Supply





Absolute Maximum Ratings*

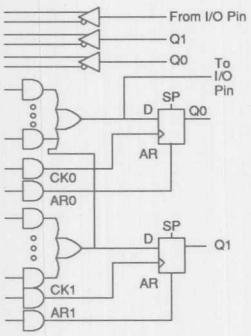
Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0 V to +14.0 V(1)
Programming Voltage with Respect to Ground	-2.0 V to +14.0 V(1)
Integrated UV Erase Dose	7258 W·sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

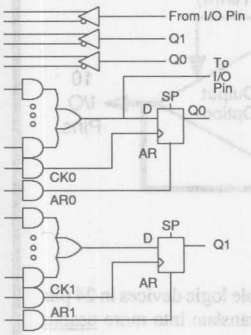
Note:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC}+0.75 V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

Logic Options

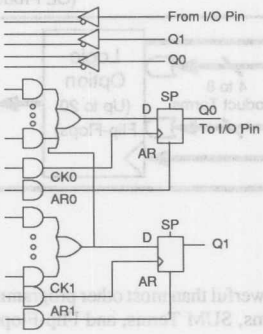
Combined Terms



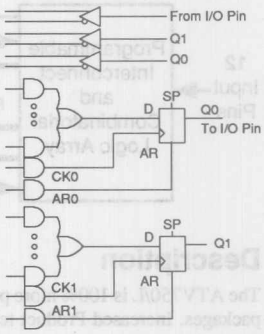
Separate Terms



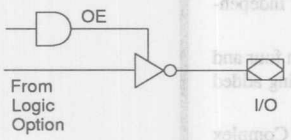
Combined Terms

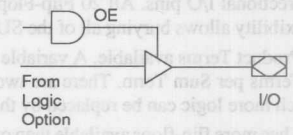


Separate Terms



Output Options





D.C. and A.C. Operating Conditions

		ATV750-20	ATV750/L-25	ATV750/L-30	ATV750/L-35	ATV750/L-40
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 10%	5 V ± 10%	5 V ± 10%	5 V ± 10%	5 V ± 10%

D.C. Characteristics

Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1 V to V_{CC}+1 V					10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1 V to V_{CC}+0.1 V					10	µA
I_{CC}	Power Supply Current	VCC = MAX, V_{IN} = GND, Outputs Open	ATV750	Com.			120	mA
				Ind.,Mil.			140	mA
			ATV750L	Com.		1.0	12	mA
				Ind.,Mil.		1.0	15	mA
I_{CC2} (2)	Clocked Power Supply Current	f = 1MHz, VCC = MAX, Outputs Open	ATV750L	Com.			15	mA
				Ind.,Mil.			20	mA
I_{OS} (1)	Output Short Circuit Current	V_{OUT} = 0.5 V					-90	mA
V_{IL}	Input Low Voltage				-0.6		0.8	V
V_{IH}	Input High Voltage				2.0		V_{CC}+0.75	V
V_{OL}	Output Low Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = MIN	I_{OL} = 12 mA Com.,Ind.				0.5	V
			I_{OL} = 8 mA Mil.				0.5	V
			I_{OL} = 24 mA, Com.				1.0	V
V_{OH}	Output High Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = MIN	I_{OH} = -100 µA		V_{CC}-0.3			V
			I_{OH} = -4.0 mA		2.4			V

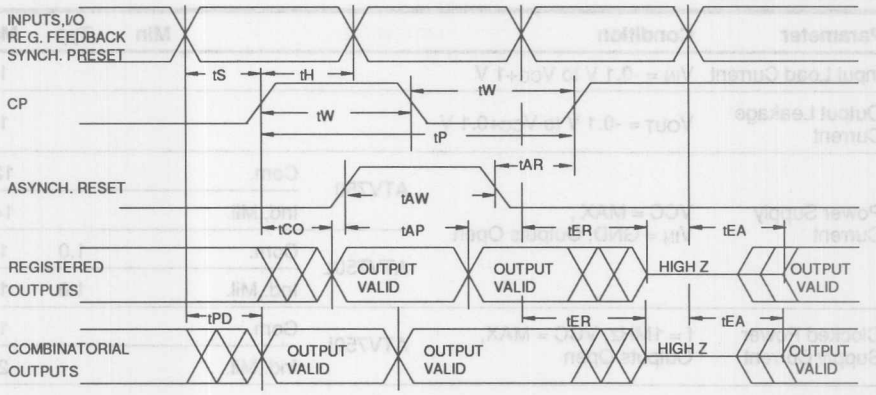
Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.
2. Outputs not loaded.

Operating Modes

	24-Pin DIP	1	5	8	11	13	I/Os	Vcc (24)
Mode	28-Pin JLCC	2	6	10	13	16	I/Os	Vcc (28)
"EPLD"		X (1)	X	X	X	X	I/O	5 V
Program		V_{PP}	X/V_H (2)	X	X/V_H	V_{PP}	D_{IN}	6 V
PGM Verify		V_{PP}	X/V_H	X	X/V_H	V_{IL}	D_{OUT}	5 V
PGM Inhibit		V_{PP}	X/V_H	X	X/V_H	V_{IH}	High Z	5-6 V
Preload #1		X	X	V_H	X	V_{IL}	D_{IN}	5 V
Preload #2		X	X	V_H	X	V_{IH}	D_{IN}	5 V

Notes: 1. X can be V_{IL} or V_{IH}.
2. V_H = 11.0 V to 14.0 V

A.C. Waveforms [1]



Note: 1. Timing measurement reference is 1.5 V. Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.

A.C. Characteristics

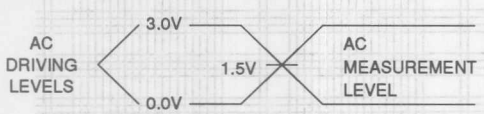
Symbol	Parameter	ATV750-30		ATV750-35		ATV750-40		Units
		Min	Max	Min	Max	Min	Max	
t_{PD}	Input or Feedback to Non-Registered Output		30		35		40	ns
t_{EA}	Input to Output Enable		30		35		40	ns
t_{ER}	Input to Output Disable		30		35		40	ns
t_{CO}	Clock to Output	5	25	10	30	10	35	ns
t_{CF}	Clock to Feedback	5	10	10	12	10	15	ns
t_S	Input Setup Time	15		18		20		ns
t_H	Hold Time	5		10		15		ns
t_P	Clock Period	25		30		35		ns
t_W	Clock Width	12		15		17		ns
F_{MAX}	Maximum Frequency		40		33		28	MHz
t_{AW}	Asynchronous Reset Width	30		35		40		ns
t_{AR}	Asynchronous Reset Recovery Time	30		35		40		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		30		35		40	ns
t_{SP}	Setup Time, Synchronous Preset	15		18		20		ns

A.C. Characteristics

Symbol	Parameter	ATV750-20		ATV750/L-25		ATV750L-30		Units
		Min	Max	Min	Max	Min	Max	
t_{PD}	Input or Feedback to Non-Registered Output		20		25		30	ns
t_{EA}	Input to Output Enable		20		25		30	ns
t_{ER}	Input to Output Disable		20		25		30	ns
t_{CO}	Clock to Output		20		22	5	25	ns
t_{CF}	Clock to Feedback	5	10	5	10	5	10	ns
t_S	Input Setup Time	10		12		15		ns
t_{SF}	Feedback Setup Time	5		7		15		ns
t_H	Hold Time	5		5		5		ns
t_P	Clock Period	18		22		25		ns
t_W	Clock Width	8		10		12		ns
F_{MAX}	Maximum Frequency		55		45		40	MHz
t_{AW}	Asynchronous Reset Width	15		20		30		ns
t_{AR}	Asynchronous Reset Recovery Time	15		20		30		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		20		25		30	ns
t_{SP}	Setup Time, Synchronous Preset	12		15		15		ns

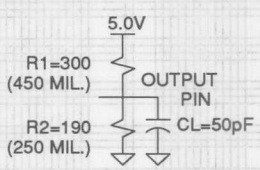
7

Input Test Waveforms and Measurement Levels

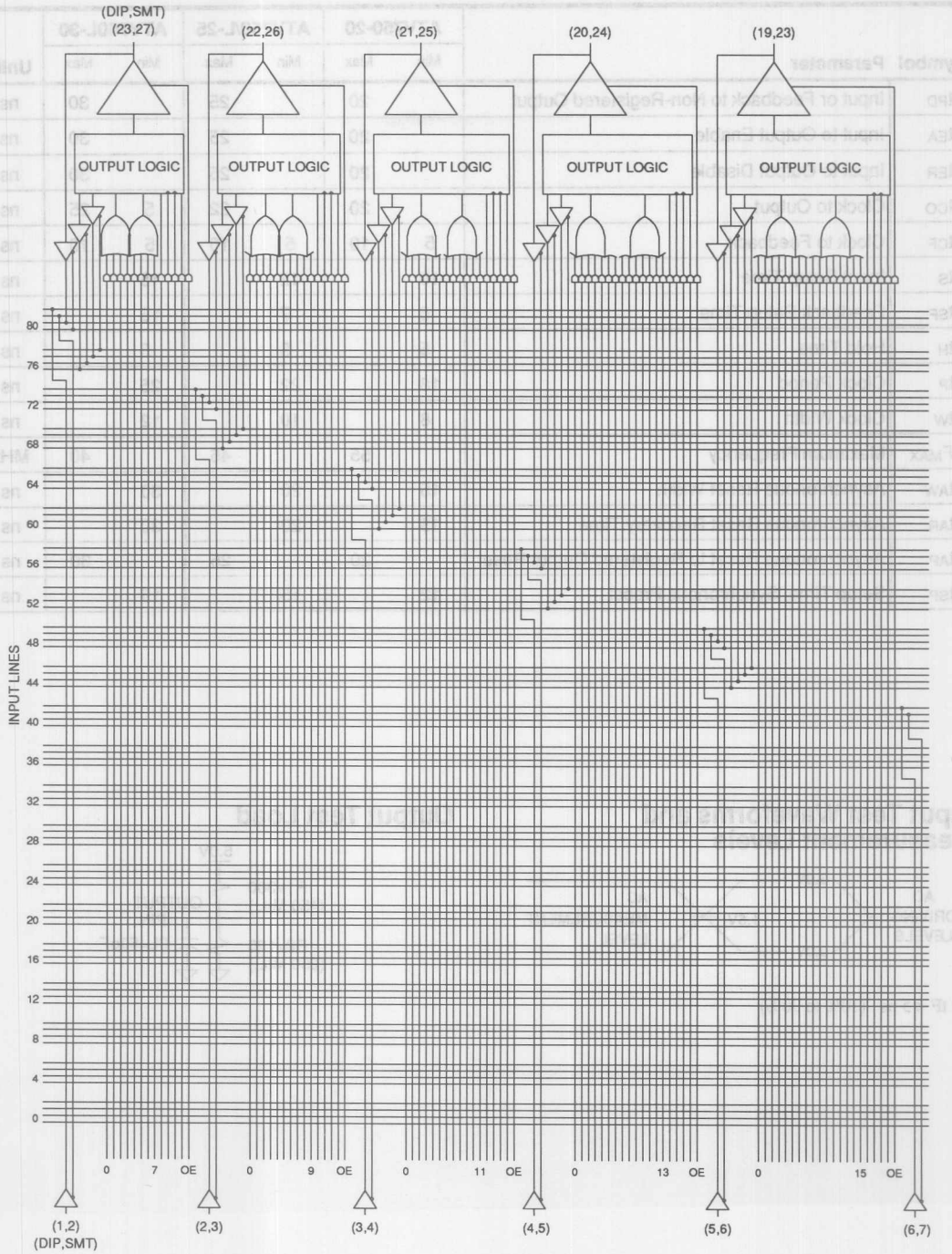


tR, tF < 5 ns (10% to 90%)

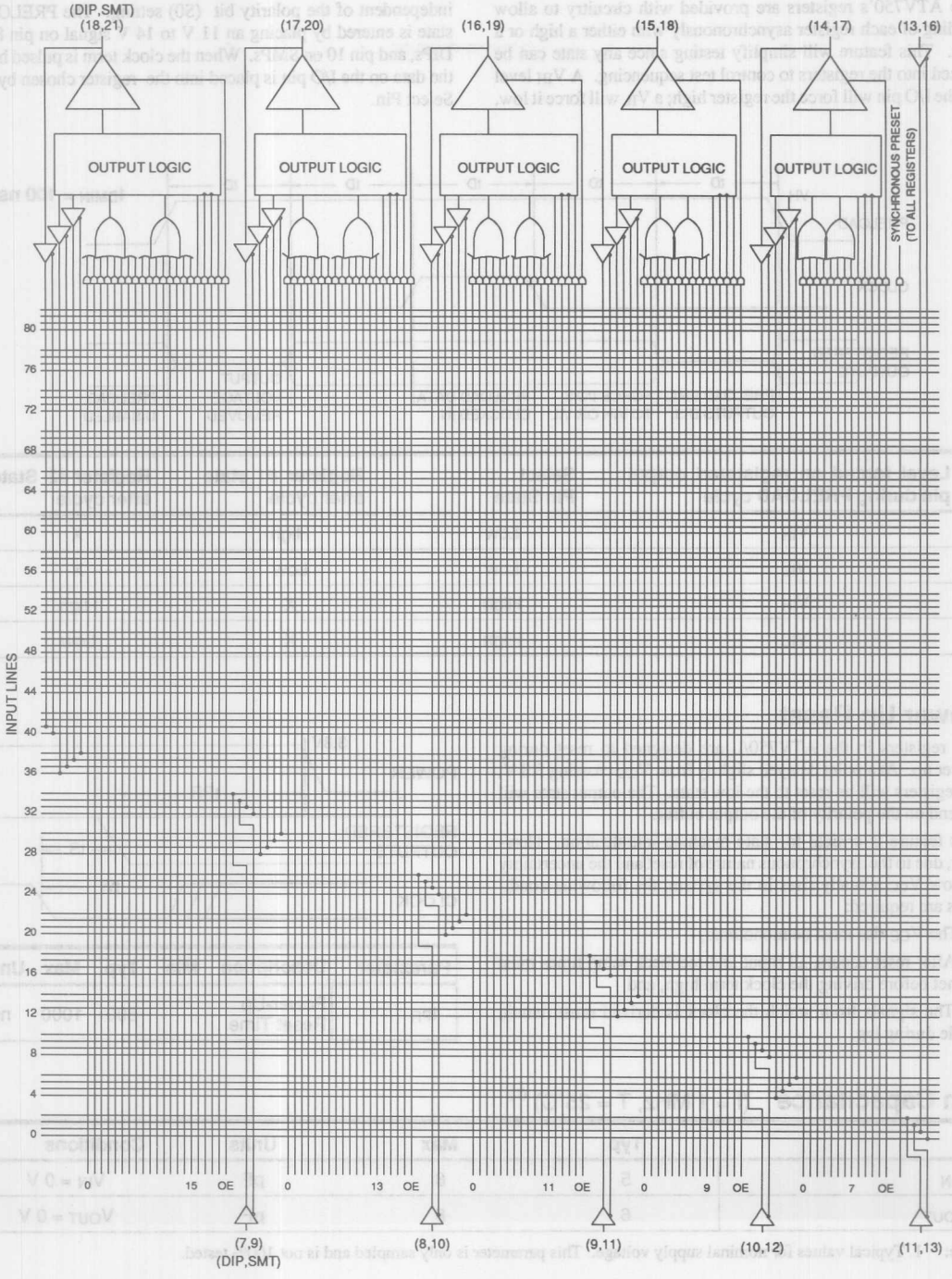
Output Test Load



Functional Logic Diagram ATV750, Upper Half



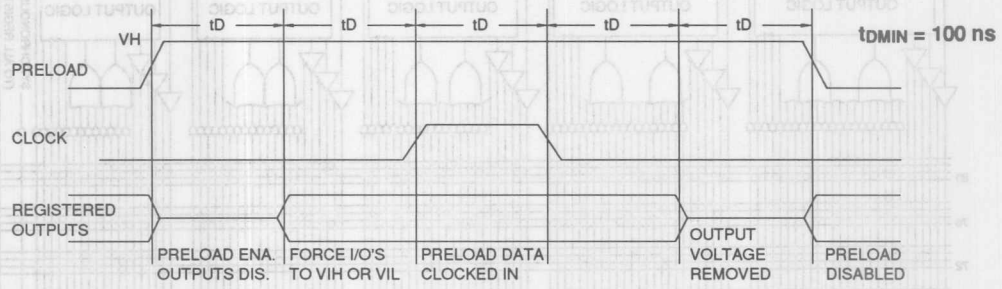
Functional Logic Diagram ATV750, Lower Half



7

Preload of Registered Outputs

The ATV750's registers are provided with circuitry to allow loading of each register asynchronously with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A V_{IH} level on the I/O pin will force the register high; a V_{IL} will force it low, independent of the polarity bit (S0) setting. The PRELOAD state is entered by placing an 11 V to 14 V signal on pin 8 on DIPs, and pin 10 on SMPs. When the clock term is pulsed high, the data on the I/O pin is placed into the register chosen by the Select Pin.



Level forced on registered output pin during PRELOAD cycle	Select Pin State	Register #1 state after cycle	Register #2 State after cycle
V_{IH}	Low	High	X
V_{IL}	Low	Low	X
V_{IH}	High	X	High
V_{IL}	High	X	Low

Power Up Reset

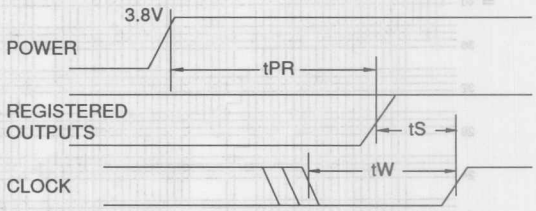
The registers in the ATV750/L are designed to reset during power up. At a point delayed slightly from V_{CC} crossing 3.8 V, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1) The V_{CC} rise must be monotonic,

2) After reset occurs, all input and feedback setup times must be met before driving the clock term high, and

3) The signals from which the clock is derived must remain stable during t_{PR}.



Parameter	Description	Min	Typ	Max	Units
t_{PR}	Power-Up Reset Time		600	1000	ns

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	5	8	pF	V_{IN} = 0 V
C_{OUT}	6	8	pF	V_{OUT} = 0 V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Using The ATV750's Many Advanced Features

The ATV750's flexibility puts more usable gates in 24 pins than other EPLDs. The ATV750/L starts with an architecture similar to the popular AT22V10, and adds several features:

- Asynchronous Clocks -
  Each of the Flip-Flops in the ATV750/L has a dedicated product term driving the clock. The user is no longer constrained to using one clock for all the registers. Buried state machines, counters, and registers can all coexist in one device, while running on separate clocks. The ATV750/L clock period matches that of similar synchronous devices.
- A Full Bank of 10 More Registers -
  The ATV750/L provides two Flip-Flops for each Output Macrocell - a total of 20. Each register has its own clock and reset product terms, as well as its own SUM term.
- Independent I/O Pin and Feedback Paths -
  Each I/O pin on the ATV750/L has a dedicated input path. Each of the 20 registers has individual feedback terms into the array. This feature, combined with individual product terms for each I/O's Output Enable, facilitates designs using bi-directional I/O buses.
- Combinable Sum Terms -
  Each Output Macrocell's two SUM terms can be combined in an OR gate before the Output or the Register. This provides up to 16 product terms per Output or Flip-Flop. This architecture increases the number of usable gates available.

Programming Software Support

Software which is capable of transforming Boolean equations, state machine descriptions and truth tables into JEDEC files for the ATV750/L is available from the following sources:

Data I/O / Futurenet Corp.	- ABEL 2.1, 3.0, and above
Logical Devices	- CUPL 2.15B, and above

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Synchronous Preset and Asynchronous Reset

One synchronous preset line is provided for all 20 registers in the ATV750/L. The appropriate input signals to cause the internal clocks to go to a high state must be received during a synchronous preset. Appropriate setup and hold times must be met, as shown in the switching waveform diagram.

An individual asynchronous reset line is provided for each of the 20 Flip-Flops. Both Master and Slave halves of the Flip-Flops are reset when the input signals received combine so as to force the internal resets high.

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATV750/L fuse patterns. Once programmed, the output buffers will remain in a high impedance state during verify.

The security fuse should be programmed last, as its effect is immediate.

Erasure Characteristics

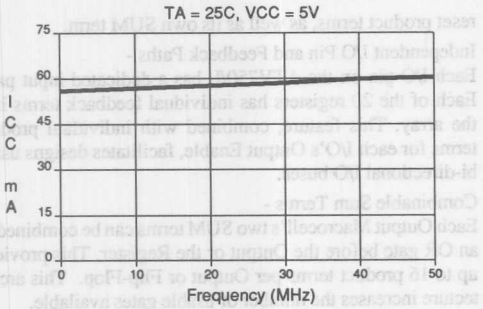
The entire memory array of an ATV750/L is erased after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 $W \cdot sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPLD which will be subjected to continuous fluorescent indoor lighting or sunlight.

Atmel CMOS EPLDs

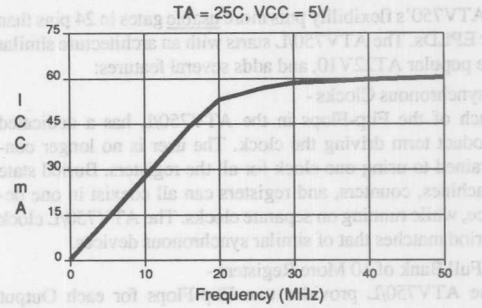
Atmel's Erasable Programmable Logic Devices utilize an advanced 1.5-micron CMOS EPROM technology. This technology's state of the art features are the optimum combination for EPLDs:

- CMOS technology provides high speed, low power, and high noise immunity.
- EPROM technology is the most cost effective method for producing EPLDs - surpassing bipolar fusible link technology in low cost, while providing the necessary reprogrammability.
- EPROM reprogrammability, which is 100% tested before shipment, provides inherently better programmability and reliability than one-time fusible PLDs.
- Atmel's EPROM process has proven extremely reliable in the volume production of a full line of advanced EPROM memory products, from 64K to one-megabit devices.

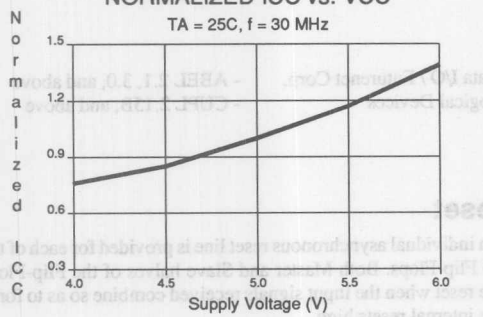
V750 ICC vs FREQUENCY



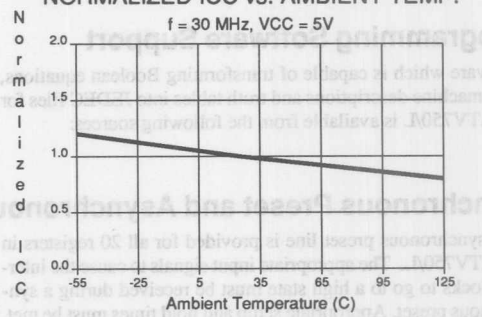
V750L ICC vs FREQUENCY



NORMALIZED ICC vs. VCC



NORMALIZED ICC vs. AMBIENT TEMP.



Ordering Information

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
20	18	55	ATV750-20DC	24DW3	Commercial (0°C to 70°C)
			ATV750-20FC	24C	
			ATV750-20GC	24D3	
			ATV750-20JC	28J	
			ATV750-20KC	28KW	
			ATV750-20LC	28LW	
			ATV750-20NC	28L	
			ATV750-20PC	24P3	
			ATV750-20SC	24S	
			ATV750-20YC	24CW	
			ATV750-20DI	24DW3	Industrial (-40°C to 85°C)
			ATV750-20FI	24C	
			ATV750-20GI	24D3	
			ATV750-20JI	28J	
			ATV750-20KI	28KW	
			ATV750-20LI	28LW	
			ATV750-20NI	28L	
			ATV750-20PI	24P3	
			ATV750-20SI	24S	
			ATV750-20YI	24CW	
			ATV750-20DM	24DW3	Military (-55°C to 125°C)
			ATV750-20FM	24C	
			ATV750-20GM	28D3	
			ATV750-20KM	28KW	
			ATV750-20LM	28LW	
			ATV750-20NM	28L	
			ATV750-20YM	24CW	
			ATV750-20DM/883	24DW3	Military/883C (-55°C to 125°C) Class B, Fully Compliant
			ATV750-20FM/883	24C	
			ATV750-20GM/883	24D3	
			ATV750-20KM/883	28KW	
			ATV750-20LM/883	28LW	
			ATV750-20NM/883	28L	
			ATV750-20YM/883	24CW	
25	22	45	ATV750-25DC	24DW3	Commercial (0°C to 70°C)
			ATV750-25FC	24C	
			ATV750-25GC	24D3	
			ATV750-25JC	28J	
			ATV750-25KC	28KW	
			ATV750-25LC	28LW	
			ATV750-25NC	28L	
			ATV750-25PC	24P3	
			ATV750-25SC	24S	
			ATV750-25YC	24CW	

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Ordering Information

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
25	22	45	ATV750-25DI	24DW3	Industrial (-40°C to 85°C)
			ATV750-25FI	24C	
			ATV750-25GI	24D3	
			ATV750-25JI	28J	
			ATV750-25KI	28KW	
			ATV750-25LI	28LW	
			ATV750-25NI	28L	
			ATV750-25PI	24P3	
			ATV750-25SI	24S	
			ATV750-25YI	24CW	
			ATV750-25DM	24DW3	Military (-55°C to 125°C)
			ATV750-25FM	24C	
			ATV750-25GM	24D3	
			ATV750-25KM	28KW	
			ATV750-25LM	28LW	
			ATV750-25NM	28L	
			ATV750-25YM	24CW	
			ATV750-25DM/883	24DW3	Military/883C (-55°C to 125°C) Class B, Fully Compliant
			ATV750-25FM/883	24C	
			ATV750-25GM/883	24D3	
			ATV750-25KM/883	28KW	
			ATV750-25LM/883	28LW	
			ATV750-25NM/883	28L	
			ATV750-25YM/883	24CW	
30	25	40	ATV750-30DC	24DW3	Commercial (0°C to 70°C)
			ATV750-30FC	24C	
			ATV750-30GC	24D3	
			ATV750-30JC	28J	
			ATV750-30KC	28KW	
			ATV750-30LC	28LW	
			ATV750-30NC	28L	
			ATV750-30PC	24P3	
			ATV750-30SC	24S	
			ATV750-30YC	24CW	
			ATV750-30DI	24DW3	Industrial (-40°C to 85°C)
			ATV750-30FI	24C	
			ATV750-30GI	24D3	
			ATV750-30JI	28J	
			ATV750-30KI	28KW	
			ATV750-30LI	28LW	
			ATV750-30NI	28L	
			ATV750-30PI	24P3	
			ATV750-30SI	24S	
			ATV750-30YI	24CW	

Ordering Information

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
30	25	40	ATV750-30DM	24DW3	Military (-55°C to 125°C)
			ATV750-30FM	24C	
			ATV750-30GM	24D3	
			ATV750-30KM	28KW	
			ATV750-30LM	28LW	
			ATV750-30NM	28L	
			ATV750-30YM	24CW	
			ATV750-30DM/883	24DW3	Military/883C (-55°C to 125°C) Class B, Fully Compliant
			ATV750-30FM/883	24C	
			ATV750-30GM/883	24D3	
			ATV750-30KM/883	28KW	
			ATV750-30LM/883	28LW	
			ATV750-30NM/883	28L	
			ATV750-30YM/883	24CW	
35	30	33	ATV750-35DC	24DW3	Commercial (0°C to 70°C)
			ATV750-35FC	24C	
			ATV750-35GC	24D3	
			ATV750-35JC	28J	
			ATV750-35KC	28KW	
			ATV750-35LC	28LW	
			ATV750-35NC	28L	
			ATV750-35PC	24P3	
			ATV750-35SC	24S	
			ATV750-35YC	24CW	
			ATV750-35DI	24DW3	Industrial (-40°C to 85°C)
			ATV750-35FI	24C	
			ATV750-35GI	24D3	
			ATV750-35JI	28J	
			ATV750-35KI	28KW	
			ATV750-35LI	28LW	
			ATV750-35NI	28L	
			ATV750-35PI	24P3	
			ATV750-35SI	24S	
			ATV750-35YI	24CW	
			ATV750-35DM	24DW3	Military (-55°C to 125°C)
			ATV750-35FM	24C	
			ATV750-35GM	24D3	
			ATV750-35KM	28KW	
			ATV750-35LM	28LW	
			ATV750-35NM	28L	
			ATV750-35YM	24CW	
			ATV750-35DM/883	24DW3	Military/883C (-55°C to 125°C) Class B, Fully Compliant
			ATV750-35FM/883	24C	
			ATV750-35GM/883	24D3	
			ATV750-35KM/883	28KW	
			ATV750-35LM/883	28LW	
			ATV750-35NM/883	28L	
			ATV750-35YM/883	24CW	

7

Ordering Information

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
40	35	28	ATV750-40DI ATV750-40FI ATV750-40GI ATV750-40JI ATV750-40KI ATV750-40LI ATV750-40NI	24DW3 24C 24D3 28J 28KW 28LW 28L	Industrial (-40°C to 85°C)
			ATV750-40PI ATV750-40SI ATV750-40YI	24P3 24S 24CW	
			ATV750-40DM ATV750-40FM ATV750-40GM ATV750-40KM	24DW3 24C 24D3 28KW	Military (-55°C to 125°C)
			ATV750-40LM ATV750-40NM ATV750-40YM	28LW 28L 24CW	
			ATV750-40DM/883 ATV750-40FM/883 ATV750-40GM/883 ATV750-40KM/883 ATV750-40LM/883 ATV750-40NM/883 ATV750-40YM/883	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
20	18	55	5962-88726 04 LX 5962-88726 04 3X	24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	22	45	5962-88726 03 LX 5962-88726 03 3X	24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
35	30	33	5962-88726 02 LX 5962-88726 02 3X	24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
40	35	28	5962-88726 01 LX 5962-88726 01 3X	24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant

Package Type	
24DW3	24 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
24C	24 Lead, Non-Windowed, Ceramic Flat Package (Cerpack)
24D3	24 Lead, 0.300" Wide, Non-Windowed (OTP) Ceramic Dual Inline Package (Cerdip)
28J	28 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
28KW	28 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
28LW	28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28L	28 Pad, Non-Windowed, Ceramic Leadless Chip Carrier OTP (LCC)
24P3	24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
24S	24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline OTP (SOIC)
24CW	24 Lead, Windowed, Ceramic Flat Package (Cerpack)

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Ordering Information

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
25	22	45	ATV750L-25DC	24DW3	Commercial (0°C to 70°C)
			ATV750L-25FC	24C	
			ATV750L-25GC	24D3	
			ATV750L-25JC	28J	
			ATV750L-25KC	28KW	
			ATV750L-25LC	28LW	
			ATV750L-25NC	28L	
			ATV750L-25PC	24P3	
			ATV750L-25SC	24S	
			ATV750L-25YC	24P3	
			ATV750L-25DI	24DW3	Industrial (-40°C to 85°C)
			ATV750L-25FI	24C	
			ATV750L-25GI	24D3	
			ATV750L-25JI	28J	
			ATV750L-25KI	28KW	
			ATV750L-25LI	28LW	
			ATV750L-25NI	28L	
			ATV750L-25PI	24P3	
			ATV750L-25SI	24S	
			ATV750L-25YI	24CW	
			ATV750L-25DM	24DW3	Military (-55°C to 125°C)
			ATV750L-25FM	24C	
			ATV750L-25GM	24D3	
			ATV750L-25KM	28KW	
			ATV750L-25LM	28LW	
			ATV750L-25NM	28L	
			ATV750L-25YM	24CW	
			ATV750L-25DM/883	24DW3	Military/883C (-55°C to 125°C) Class B, Fully Compliant
			ATV750L-25FM/883	24C	
			ATV750L-25GM/883	24D3	
			ATV750L-25KM/883	28KW	
			ATV750L-25LM/883	28LW	
			ATV750L-25NM/883	28L	
			ATV750L-25YM/883	24CW	
30	25	40	ATV750L-30DC	24DW3	Commercial (0°C to 70°C)
			ATV750L-30FC	24C	
			ATV750L-30GC	24D3	
			ATV750L-30JC	28J	
			ATV750L-30KC	28KW	
			ATV750L-30LC	28LW	
			ATV750L-30NC	28L	
			ATV750L-30PC	24P3	
			ATV750L-30SC	24S	
			ATV750L-30YC	24P3	

Ordering Information

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
30	25	40	ATV750L-30DI ATV750L-30FI ATV750L-30GI ATV750L-30JI ATV750L-30KI ATV750L-30LI ATV750L-30NI ATV750L-30PI ATV750L-30SI ATV750L-30YI	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24S 24CW	Industrial (-40°C to 85°C)
			ATV750L-30DM ATV750L-30FM ATV750L-30GM ATV750L-30KM ATV750L-30LM ATV750L-30NM ATV750L-30YM	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military (-55°C to 125°C)
			ATV750L-30DM/883 ATV750L-30FM/883 ATV750L-30GM/883 ATV750L-30KM/883 ATV750L-30LM/883 ATV750L-30NM/883 ATV750L-30YM/883	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	22	45	5962-88726 07 LX 5962-88726 07 3X	24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
30	25	40	5962-88726 07 LX 5962-88726 07 3X	24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant

Package Type	
24DW3	24 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
24C	24 Lead, Non-Windowed, Ceramic Flat Package (Cerpack)
24D3	24 Lead, 0.300" Wide, Non-Windowed (OTP) Ceramic Dual Inline Package (Cerdip)
28J	28 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
28KW	28 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
28LW	28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28L	28 Pad, Non-Windowed, Ceramic Leadless Chip Carrier OTP (LCC)
24P3	24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
24S	24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline OTP (SOIC)
24CW	24 Lead, Windowed, Ceramic Flat Package (Cerpack)

Ordering Information

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
30	25	40	ATV750L-30DI	24DW3	Industrial (-40°C to 85°C)
			ATV750L-30FI	24C	
			ATV750L-30DJ	24D3	
			ATV750L-30JI	28J	
			ATV750L-30KI	28KW	
			ATV750L-30LI	28LW	
			ATV750L-30NI	28L	
			ATV750L-30PI	24P3	
			ATV750L-30SI	24S	
			ATV750L-30YI	24CW	
			ATV750L-30DM	24DW3	Military (-55°C to 125°C)
			ATV750L-30FM	24C	
			ATV750L-30DM	24D3	
			ATV750L-30KM	28KW	
			ATV750L-30LM	28LW	
			ATV750L-30NM	28L	
			ATV750L-30YM	24CW	
			ATV750L-30DM/883	24DW3	Military/883C (-55°C to 125°C) Class B, Fully Compliant
			ATV750L-30FM/883	24C	
			ATV750L-30DM/883	24D3	
			ATV750L-30KM/883	28KW	
			ATV750L-30LM/883	28LW	
			ATV750L-30NM/883	28L	
			ATV750L-30YM/883	24CW	
25	22	45	5962-88726 07 LX	24DW3	Military/883C (-55°C to 125°C) Class B, Fully Compliant
			5962-88726 07 3X	28LW	
30	25	40	5962-88726 07 LX	24DW3	Military/883C (-55°C to 125°C) Class B, Fully Compliant
			5962-88726 07 3X	28LW	

Package Type	
24DW3	24 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
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Using the ATV750 with ABEL™ and CUPL™

High Density UV Erasable Programmable Logic Device

Application Brief

7

Typical applications for first and second generation PLDs include address decoding and counting. Here is an example using the ATV750, a third generation PLD, to implement a more complex counter. The following pages show example input listings for ABEL™ and CUPL™.

The first listing is for ABEL™ 3.0. The second listing is for CUPL™ 2.15b.

This design uses all twenty flip-flops of the ATV750 to build a 20-bit synchronous /asynchronous counter. With COUNT high and COUNT10, PRESET, RESET, Q1SEL, and OE low, a 1-MHz signal on the CLK pin will produce roughly a 1-Hz signal on pin 23.

The unique architecture of the macrocell gives the ATV750 its versatility and also increases gate utilization. Each of the twenty registers has its Q and $\overline{Q}$ feeding back to the array.

The Output Registers (Q0's) can be addressed directly (by the pin names in ABEL™; in CUPL™ define PINNODES 35 through 44). However, to access the Buried Registers (Q1's), the corresponding nodes have to be named (nodes 26 through 35 in ABEL™, PINNODEs 25 through 34 in CUPL™). They are called B14, B15,...B24 to show the correspondence with their Q0 counterparts. Any valid identifier can be used as a node name.

The ATV750 provides a global synchronous Preset which is accessible through the node definition or by extension. Each of the twenty flip-flops has its own clock, reset and sum term (not like a second generation PLD that allows only one clock and one reset for all registers). Use the '.CK' extension in conjunction with the named registers to define the equations for the clock inputs for all the registers. Use the '.RE' command following the named registers to define the reset terms.

The ATV750 gives the user a total of eight choices to configure each output. The operators ':=' and '=' inform ABEL™ the output is registered or combinatorial, respectively. In CUPL™, use of the .Q extension defines a registered output. Use the '!' operator to define an active low output; active high output is assumed by default. Another convenient method is to use the 'ISTYPE' statement (ABEL™ only) to define the outputs as high/low and registered/combinatorial. (Note: the ATV22V10 is defined the same way.)

The ATV750 has an advanced feature that lets the user combine or separate the sum terms in each macrocell. By default, the terms are combined. In CUPL™ and ABEL™, using the buried register automatically splits the sum terms.

Sets (ABEL™) or *fields* (CUPL™) are often defined for ease of referencing a group of signals or constants. In this particular example, *OUTS* is a collection of outputs used in the OE definition. *Out* is a reserved word in CUPL, and *Ouch* was used instead.

When PRESET and COUNT are asserted and the Clk pin goes high, all registers, even the asynchronously clocked ones, will go to the 'one' state. This is because as each flip-flop goes high, it forces the clock of the next flip-flop high, rippling the preset condition throughout the entire bank. To reset the output registers and the buried registers, simply have RESET high and vary !Q1SEL accordingly.

The O registers pair with the corresponding B registers to form ten two-bit synchronous counters. These are clocked by the preceding pair's output, thus forming a 20-bit counter. The last product term for the 'O' logic changes this device into a ten-bit counter with the output register mimicking the B registers. This provides observability, and a handy test mode. Test vectors take full

advantage of ABEL™'s and CUPL™'s ability to simulate the device before programming. This feature can save hours of testing and enable the user to make the necessary changes in seconds without ever leaving his or her PC. Therefore, it is highly recommended to take the time to write a comprehensive set of test vectors; this will reduce the time spent on the test bench.

ABEL™ and CUPL™ may be trademarks of others.

ABEL™ Example

```
module EX3
title '20 Bit Counter for Atmel's ATV750
EX375  device 'P750';
Clk                     pin   1;
COUNT,COUNT10,PRESET    pin   2, 3, 4;
RESET, Q1SEL , OE       pin   5, 11, 13;
O14,O15,O16,O17,O18     pin   14,15,16,17,18;
O19,O20,O21,O22,O23     pin   19,20,21,22,23;
B14,B15,B16,B17,B18     node  26,27,28,29,30;
B19,B20,B21,B22,B23     node  31,32,33,34,35;
"      Nodes      Description
"      26..35     Q1 for pins 14 to 23
"Sets
OUTS=[O23,O22,O21,O20,O19,O18,O17,O16,O15,O14];
H,L,Z,C,X     =   1,0,.Z.,.C.,.X.;
Equations
O14.RE        =   O14.Q & RESET & !Q1SEL;
B14.RE        =   B14 & RESET & Q1SEL;
O15.RE        =   O15.Q & RESET & !Q1SEL;
B15.RE        =   B15 & RESET & Q1SEL;
O16.RE        =   O16.Q & RESET & !Q1SEL;
B16.RE        =   B16 & RESET & Q1SEL;
O17.RE        =   O17.Q & RESET & !Q1SEL;
B17.RE        =   B17 & RESET & Q1SEL;
O18.RE        =   O18.Q & RESET & !Q1SEL;
B18.RE        =   B18 & RESET & Q1SEL;
O19.RE        =   O19.Q & RESET & !Q1SEL;
B19.RE        =   B19 & RESET & Q1SEL;
O20.RE        =   O20.Q & RESET & !Q1SEL;
B20.RE        =   B20 & RESET & Q1SEL;
O21.RE        =   O21.Q & RESET & !Q1SEL;
B21.RE        =   B21 & RESET & Q1SEL;
O22.RE        =   O22.Q & RESET & !Q1SEL;
B22.RE        =   B22 & RESET & Q1SEL;
O23.RE        =   O23.Q & RESET & !Q1SEL;
B23.RE        =   B23 & RESET & Q1SEL;
O14.C         =   Clk & COUNT;
B14.CK        =   Clk & COUNT; "Synchronous
O15.CK        =   O14.Q & COUNT;
B15.CK        =   O14.Q & COUNT; "Asynchronous
O16.CK        =   O15.Q & COUNT;
B16.CK        =   O15.Q & COUNT;
O17.CK        =   O16.Q & COUNT;
B17.CK        =   O16.Q & COUNT;
O18.CK        =   O17.Q & COUNT;
B18.CK        =   O17.Q & COUNT;
O19.CK        =   O18.Q & COUNT;
B19.CK        =   O18.Q & COUNT;
O20.CK        =   O19.Q & COUNT;
B20.CK        =   O19.Q & COUNT;
O21.CK        =   O20.Q & COUNT;
B21.CK        =   O20.Q & COUNT;
O22.CK        =   O21.Q & COUNT;
O23.CK        =   O22.Q & COUNT;
B23.CK        =   O22.Q & COUNT;
B14           :=  !B14;
!O14          :=  !O14.Q &  B14 & !COUNT10
#             O14.Q & !B14 & !COUNT10
#             !B14 & COUNT10;
B15           :=  !B15;
!O15          :=  !O15.Q & B15 & !COUNT10
#             O15.Q & !B15 & !COUNT10
#             !B15 & COUNT10;
B16           :=  !B16;
!O16          :=  !O16.Q & B16 & !COUNT10
#             O16.Q & !B16 & !COUNT10
#             !B16 & COUNT10;
B17           :=  !B17;
!O17          :=  !O17.Q & B17 & !COUNT10
#             O17.Q & !B17 & !COUNT10
#             !B17 & COUNT10;
B18           :=  !B18;
!O18          :=  !O18.Q & B18 & !COUNT10
#             O18.Q & !B18 & !COUNT10
#             !B18 & COUNT10;
B19           :=  !B19;
!O19          :=  !O19.Q &  B19 & !COUNT10
#             O19.Q & !B19 & !COUNT10
#             !B19 & COUNT10;
B20           :=  !B20;
!O20          :=  !O20.Q & B20 & !COUNT10
#             O20.Q & !B20 & !COUNT10
#             !B20 & COUNT10;
B21           :=  !B21;
!O21          :=  !O21.Q & B21 & !COUNT10
#             O21.Q & !B21 & !COUNT10
#             !B21 & COUNT10;
B22           :=  !B22;
!O22          :=  !O22.Q & B22 & !COUNT10
#             O22.Q & !B22 & !COUNT10
#             !B22 & COUNT10;
B23           :=  !B23;
!O23          :=  !O23.Q & B23 & !COUNT10
#             O23.Q & !B23 & !COUNT10
#             !B23 & COUNT10;
O23.PR        =   PRESET;
ENABLE OUTS   =   !OE;
End
```

CUPL™ Example

```
Name          EX75;
Company       Atmel;
Device        V750;
/*****************************************/
/** Allowable Target Device Types :V750    */
/*****************************************/
/**Inputs     **/
PIN [1..4]    =  [Clk,COUNT,COUNT10,PRESET];
PIN [5,11,13] =  RESET,Q1SEL,OE;
/**Outputs**/
PIN [14..23]  =  [Q14..Q23]; /* Pin Outputs*/
/*The easiest way to access the buried nodes
in CUPL*/
/*Refer to the I/O pins by their pin names,
and the */
/* Q0 and Q1 outputs by their pinnode names*/
PINNODE [25..34] =  [B14..B23]; /* Q1 nodes*/
field BEES  = [B23..B14]; /*Q1 field*/
field Ohi   = [O23..O19]; /*output hi field*/
field Olo   = [O18..O14]; /*output low field*/
field Ouch  = [O23..O14]; /*outputfield*/
/** Logic Equations **/
/*  The Asynch. Reset terms use the .AR
extension*/
Q14.AR        =  Q14 &  RESET & !Q1SEL;
B14.AR        =  B14 &  RESET & Q1SEL;
Q15.AR        =  Q15 &  RESET & !Q1SEL;
B15.AR        =  B15 &  RESET & Q1SEL;
Q16.AR        =  Q16 &  RESET & !Q1SEL;
B16.AR        =  B16 &  RESET & Q1SEL;
Q17.AR        =  Q17 &  RESET & !Q1SEL;
B17.AR        =  B17 &  RESET & Q1SEL;
Q18.AR        =  Q18 &  RESET & !Q1SEL;
B18.AR        =  B18 &  RESET & Q1SEL;
Q19.AR        =  Q19 &  RESET & !Q1SEL;
B19.AR        =  B19 &  RESET & Q1SEL;
Q20.AR        =  Q20 &  RESET & !Q1SEL;
B20.AR        =  B20 &  RESET & Q1SEL;
Q21.AR        =  Q21 &  RESET & !Q1SEL;
B21.AR        =  B21 &  RESET & Q1SEL;
Q22.AR        =  Q22 &  RESET & !Q1SEL;
B22.AR        =  B22 &  RESET & Q1SEL;
Q23.AR        =  Q23 &  RESET & !Q1SEL;
B23.AR        =  B23 &  RESET & Q1SEL;
/* The Clock lines are accessed with the .CK
extension*/
Q14.CK        =  Clk & COUNT;
B14.CK        =  Clk & COUNT; /* Synchronous */
Q15.CK        =  Q14 & COUNT;
B15.CK        =  Q14 & COUNT; /* Asynchronous*/
Q16.CK        =  Q15 & COUNT;
B16.CK        =  Q15 & COUNT;
Q17.CK        =  Q16 & COUNT;
B17.CK        =  Q16 & COUNT;
Q18.CK        =  Q17 & COUNT;
B18.CK        =  Q17 & COUNT;
Q19.CK        =  Q18 & COUNT;
B19.CK        =  Q18 & COUNT;
Q20.CK        =  Q19 & COUNT;
B20.CK        =  Q19 & COUNT;
Q21.CK        =  Q20 & COUNT;
B21.CK        =  Q20 & COUNT;
Q22.CK        =  Q21 & COUNT;
B22.CK        =  Q21 & COUNT;
Q23.CK        =  Q22 & COUNT;
B23.CK        =  Q22 & COUNT;
B14.D         =  !B14;
Q14.D         =  !Q14 &  B14 & !COUNT10
              #  Q14 & !B14 & !COUNT10
              #  !B14 & COUNT10;
/* Equations for both the B and the Q
automatically*/
/*tells CUPL to set the 'split' SUM term's
architecture bit.*/
B15.D         =  !B15;
Q15.D         =  !Q15 & B15 & !COUNT10
              #  Q15 & !B15 & !COUNT10
              #  !B15 & COUNT10;
B16.D         =  !B16;
Q16.D         =  !Q16 & B16 & !COUNT10
              #  Q16 & !B16 & !COUNT10
              #  !B16 & COUNT10;
B17.D         =  !B17;
Q17.D         =  !Q17 & B17 & !COUNT10
              #  Q17 & !B17 & !COUNT10
              #  !B17 & COUNT10;
B18.D         =  !B18;
Q18.D         =  !Q18 & B18 & !COUNT10
              #  Q18 & !B18 & !COUNT10
              #  !B18 & COUNT10;
B19.D         =  !B19;
Q19.D         =  !Q19 & B19 & !COUNT10
              #  Q19 & !B19 & !COUNT10
              #  !B19 & COUNT10;
B20.D         =  !B20;
Q20.D         =  !Q20 & B20 & !COUNT10
              #  Q20 & !B20 & !COUNT10
              #  !B20 & COUNT10;
B21.D         =  !B21;
Q21.D         =  !Q21 & B21 & !COUNT10
              #  Q21 & !B21 & !COUNT10
              #  !B21 & COUNT10;
B22.D         =  !B22;
Q22.D         =  !Q22 &  B22 & !COUNT10
              #  Q22 & !B22 & !COUNT10
              #  !B22 & COUNT10;
B23.D         =  !B23;
Q23.D         =  !Q23 & B23 & !COUNT10
              #  Q23 & !B23 & !COUNT10
              #  !B23 & COUNT10;
/*Only one synch preset equation is required*/
O23.SP        =  PRESET;
/*Use the .OE extension for the OE product
term*/
O14.oe        =  !OE ;    O19.oe=!OE ;
O15.oe        =  !OE ;    O20.oe=!OE ;
O16.oe        =  !OE ;    O21.oe=!OE ;
O17.oe        =  !OE ;    O22.oe=!OE ;
O18.oe        =  !OE ;    O23.oe=!OE ;
```

Features

- **Low Voltage Programmable Logic Device**
  - **Wide Power Supply Range - 3.0 V to 5.5 V**
  - **Ideal for Battery Powered Systems**
- **High Speed Operation**
  - **25 ns Max Propagation Delay at V_{CC} = 3.0 V**
- **Low Power, Three-Volt CMOS Operation**

	ATV750LVL	ATV750LV
Temp.	Com. / Mil.	Com. / Mil.
I_{CC} (mA)	4 / 7	40 / 50

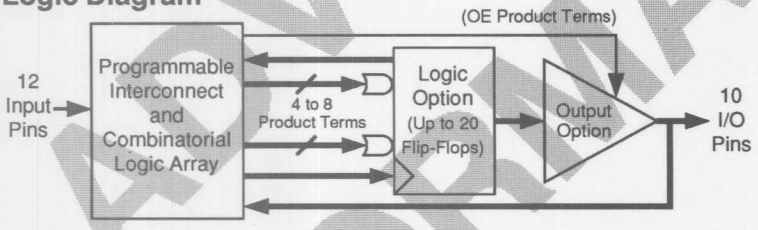
- **Flexible Output Logic**
  - **20 Flip-Flops - 10 Extra**
  - **All Can Be Individually Buried or 10 Connected to I/O Pins**
  - **Each has Individual Asynchronous Reset and Clock Terms**
- **Multiple Feedback Paths Provide for Buried State Machines and I/O Bus Compatibility**
- **Proven and Reliable High Speed CMOS EPROM Process**
  - **2000 V ESD Protection**
  - **200 mA Latchup Immunity**
- **Reprogrammable - Tested 100% for Programmability**
- **24-pin, 300-mil Dual-In-line and 28-Lead Surface Mount Packages**

Low Voltage UV Erasable Programmable Logic Device

Advance Information

7

Logic Diagram



Description

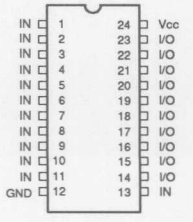
The ATV750LV and ATV750LVL are low voltage compatible CMOS high performance Erasable Programmable Logic Devices (EPLDs). Speeds down to 25 ns and power dissipation as low as 14.4 mW are offered. All speed ranges are specified over the 3.0 V to 5.5 V range. All pins offer a low ± 10 µA leakage.

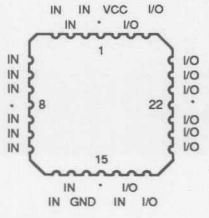
The ATV750LV/LVL provides the optimum power CMOS EPLD solution, with low D.C. power (1 mA typical at V_{CC} = 3.3 V) and full CMOS output levels. The ATV750LVL significantly reduces total system power, allowing battery powered operation.

(Continued on next page)

Pin Configurations

Pin Name	Function
IN	Logic Inputs
I/O	Bidirectional Buffers
*	No Internal Connection
VCC	+5V Supply





ADVANCE INFORMATION

Description (Continued)

The ATV750LV/LVL is 100% more powerful than most other programmable logic devices in 24-pin packages. Increased Product terms, SUM Terms, and Flip-Flops translate into more usable gates.

The ATV750LV/LVL has more flip-flops available than other EPLDs in this density range. Complex state machines are easily implemented.

Product terms are available providing Asynchronous Resets, Flip-Flop clocks, and Output Enables. One reset and one clock term are provided per Flip-Flop, with one Enable term per output. One product term provides a global synchronous Preset. Register Preload simplifies testing. The device has an internal power up clear function.

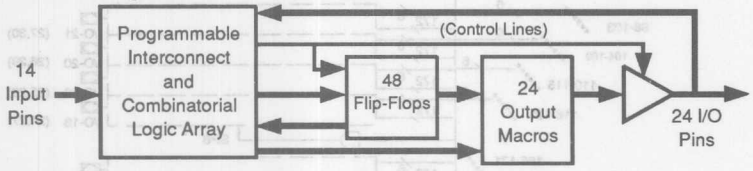
Features

- Third Generation Programmable Logic Structure
  - Easily Achieves Gate Utilization Factors of 80 Percent
- Increased Logic Flexibility
  - 86 Inputs and 72 Sum Terms
- Flexible Output Macrocell
  - 48 Flip-Flops - 2 per Macrocell
  - 3 Sum Terms - Can Be OR'ed and Shared
- High Speed
- Low Power - Less than 0.5 mA Typical (ATV2500L)
- Multiple Feedback Paths Provide for Buried State Machines and I/O Bus Compatibility
- Asynchronous Clocks and Resets
  - Multiple Synchronous Presets - One per Four or Eight Flip-Flops
- Proven and Reliable High Speed CMOS EPROM Process
  - 2000 V ESD Protection
  - 200 mA Latchup Immunity
- Reprogrammable - Tested 100% for Programmability
- 40-pin Dual-In-line and 44-Lead Surface Mount Packages

High Density UV Erasable Programmable Logic Device

7

Block Diagram



Description

The ATV2500H/L is the most powerful programmable logic device available in a 40 pin package. Increased Product terms, Sum Terms, and Flip-Flops translate into many more usable gates. High gate utilization is easily obtainable.

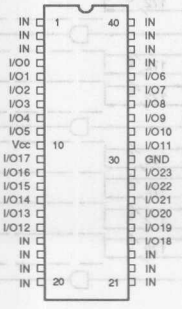
The ATV2500H/L is organized around a global bus. All pin and feedback terms are always available to every Logic Cell. Each of the 38 logic pins and their complements are array inputs, as well as the true and false outputs of each of the 48 Flip-Flops.

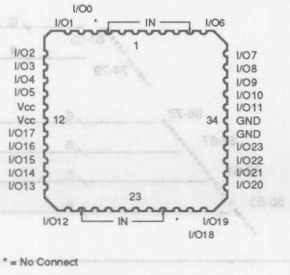
There are 416 Product Terms available. Four Product Terms are input to each Sum Term. The three Sum terms per Logic Cell can be combined to provide up to 12 Product Terms, Combinatorial and Registered. Independent of output configuration, the two Flip-Flops are always usable, and always have at least four Product Term inputs.

Product terms are available providing Asynchronous Resets, Flip-Flop clocks, and Output Enables. One reset and one clock term are provided per Flip-Flop, with one Enable term per output. Eight product terms provide local Synchronous Presets, divided up into banks of four and eight Flip-Flops. Register Preload and buried register observability simplify testing. The device has an internal power up clear function.

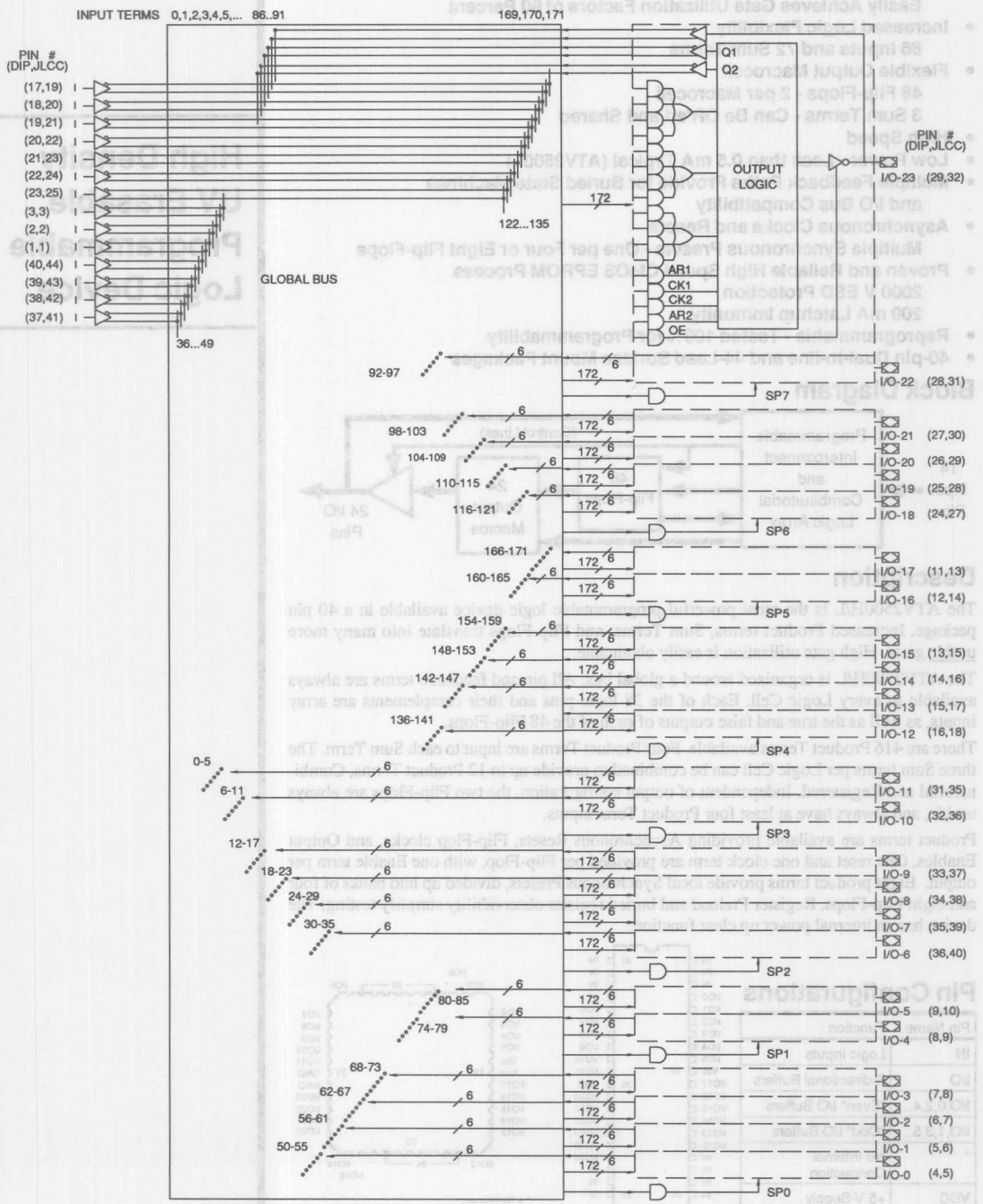
Pin Configurations

Pin Name	Function
IN	Logic Inputs
I/O	Bidirectional Buffers
I/O,0,2,4..	"Even" I/O Buffers
I/O,1,3,5..	"Odd" I/O Buffers
*	No Internal Connection
VCC	+5 V Supply





Functional Logic Diagram ATV2500H/L



Functional Logic Diagram Description

The ATV2500H/L Functional Logic Diagram describes the interconnections between the input, feedback pins and Logic Cells. All interconnections are routed through the Global Bus.

The ATV2500H/L is a straightforward and uniform EPLD. The 24 Macrocells are numbered 0 through 23. Each Macrocell contains 17 AND gates. All AND gates have 172 inputs. The five lower product terms provide AR1, CK1, CK2, AR2, and OE. These are: one asynchronous reset and clock per Flip-Flop, and an Output Enable. The top 12 product terms are grouped into three sum terms, which are used as shown in the Macrocell diagrams.

Eight Synchronous Preset terms are distributed in a 2/4 pattern. The first four Macrocells share Preset 0, the next two share Preset 1, and so on, ending with the last two Macrocells sharing Preset 7.

The 14 dedicated inputs and their complements use the numbered positions in the global bus as shown. Each Macrocell provides six inputs to the global bus: (left to right) Flip-Flop Q2 true and false, Flip-Flop Q1 true and false, and the pin true and false. The positions occupied by these signals in the Global Bus are the six numbers in the bus diagram next to each Macrocell.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0 V to +14.0 V(1)
Programming Voltage with Respect to Ground	-2.0 V to +14.0 V(1)
Integrated UV Erase Dose	7258 W-sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

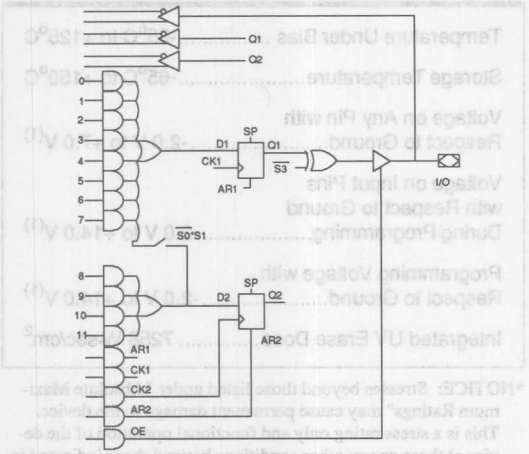
Note:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC}+0.75 V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

Operating Modes

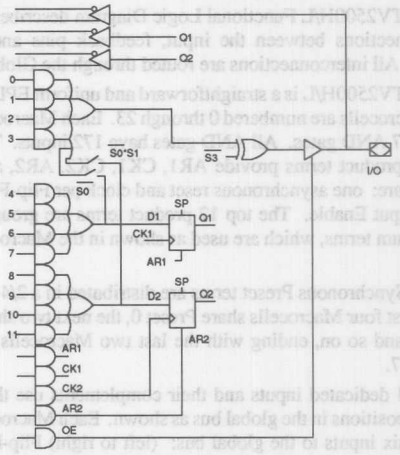
	40-Pin DIP	21	2	38	23	20	V_{CC}(10)	Odd	Even
Mode	44-Pin JLCC	23	2	42	25	22	V_{CC}(11,12)	I/Os	I/Os
"EPLD"		X(1)	X	X	X	X	5 V	I/O	I/O
Program		V_{PP}	X	X	X	V_H (2)	6 V	D_{IN}	N.C.
PGM Verify		V_{PP}	X	X	X	V_{IL}	6 V	D_{OUT}	V_{OH}
PGM Inhibit		V_{PP}	X	X	X	V_{IH}	6 V	High Z	High Z
Preload Q1		⎍	X	V_H	V_{IL}/V_{IH}	V_{IL}	5 V	D_{IN}(Even/Odd)	V_{IH}
Preload Q2		⎍	X	V_H	V_{IL}/V_{IH}	V_{IH}	5 V	D_{IN}(Even/Odd)	V_{IH}
Observe Q2		X	V_H	X	X	X	5 V	D_{OUT}	D_{OUT}

Notes: 1. X can be V_{IL} or V_{IH}.
2. V_H = 11.0 V to 14.0 V

Output Logic, Registered [1]



Output Logic, Combinatorial [1]



Note: 1. These diagrams shows equivalent logic functions, not necessarily the actual circuit implementation.

			Terms In		
S2	S1	S0	D1	D2	Output Configuration
0	0	0	8	4	Registered (Q1)
0	1	0	12	4[1]	Registered (Q1)

Note: 1. These 4 terms are shared with D1.

			Terms In		
S2	S1	S0	D1	D2	Output Configuration
1	0	0	4[1]	4	Combinatorial (8 Terms)
1	0	1	4	4	Combinatorial (4 Terms)
1	1	0	4[1]	4[1]	Combinatorial (12 Terms)

Note: 1. These 4 terms are shared with D1.

S3	Output Configuration
0	Active Low
1	Active High

S3	Output Configuration
0	Active Low
1	Active High

D.C. and A.C. Operating Conditions

		ATV2500H-25	ATV2500H/L-30	ATV2500H/L-35	ATV2500L-40	ATV2500L-45
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 10%	5 V ± 10%	5 V ± 10%	5 V ± 10%	5 V ± 10%

D.C. Characteristics

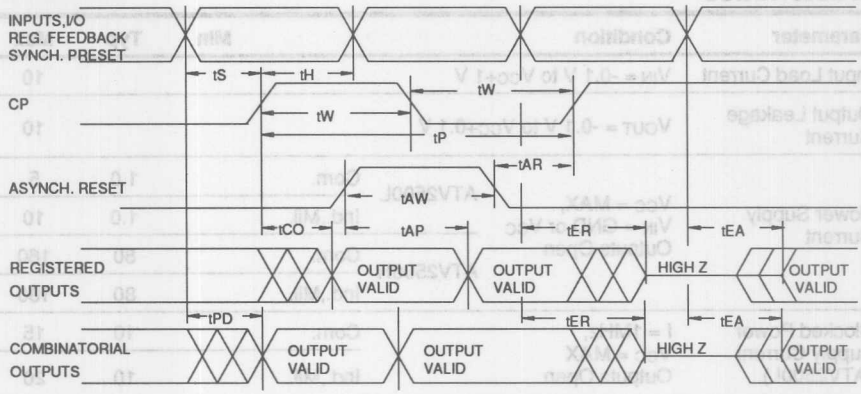
Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1 V to V_{CC}+1 V					10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1 V to V_{CC}+0.1 V					10	µA
I_{CC}	Power Supply Current	V_{CC} = MAX, V_{IN} = GND or V_{CC} Outputs Open	ATV2500L	Com.		1.0	5	mA
				Ind.,Mil.		1.0	10	mA
			ATV2500H	Com.		80	160	mA
				Ind.,Mil.		80	180	mA
I_{CC2}	Clocked Power Supply Current (ATV2500L)	f = 1MHz, V_{CC} = MAX Outputs Open		Com.		10	15	mA
				Ind.,Mil.		10	20	mA
I_{OS} [1]	Output Short Circuit Current	V_{OUT} = 0.5 V					-90	mA
V_{IL}	Input Low Voltage				-0.6		0.8	V
V_{IH}	Input High Voltage				2.0		V_{CC}+0.75	V
V_{OL}	Output Low Voltage	V_{IN} = V_{IH} or V_{IL}, I_{OL} = 8 mA Com,Ind; 6 mA Mil.					0.5	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA			V_{CC}-0.3			V
		I_{OH} = -4.0 mA			2.4			V

Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.This parameter is only sampled and is not 100% tested. See Absolute Maximum Ratings.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.



Note: 1. Timing measurement reference is 1.5 V. Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.

A.C. Characteristics for the ATV2500L

Symbol	Parameter	ATV2500L-30		ATV2500L-35		ATV2500L-40		ATV2500L-45		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input or Feedback to Non-Registered Output		30		35		40		45	ns
t_{EA}	Input to Output Enable		30		35		40		45	ns
t_{ER}	Input to Output Disable		30		35		40		45	ns
t_{CO}	Clock to Output	5	30	5	35	5	40	5	45	ns
t_{CF}	Clock to Feedback	10	20	15	20	15	22	15	25	ns
t_{SI1}	Input Setup Time, Output Register	20		22		25		30		ns
t_{SI2}	Input Setup Time, Buried Register(1)	5		5		5		5		ns
t_{SF}	Feedback Setup Time	10		15		18		20		ns
t_{H1}	Hold Time, Output Register	10		15		15		15		ns
t_{H2}	Hold Time, Buried Register(1)	5		5		5		5		ns
t_W	Clock Width	12		15		17		20		ns
t_P	Clock Period	30		35		40		45		ns
F_{MAX}	Maximum Frequency (1/t_P)		33		28		25		22	MHz
t_{AW}	Asynchronous Reset Width	18		20		22		25		ns
t_{AR}	Asynchronous Reset Recovery Time	18		20		22		25		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		30		35		40		45	ns

Note: 1. Buried registers include all 24 Q2 registers and any of the 24 Q1 registers in macrocells configured as combinatorial.

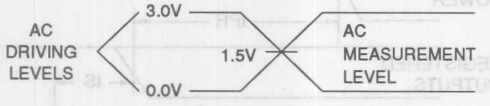
A.C. Characteristics for the ATV2500H

Symbol	Parameter	ATV2500H-25 Min	ATV2500H-25 Max	ATV2500H-30 Min	ATV2500H-30 Max	ATV2500H-35 Min	ATV2500H-35 Max	Units
t_{PD}	Input or Feedback to Non-Registered Output		25		30		35	ns
t_{EA}	Input to Output Enable		25		30		35	ns
t_{ER}	Input to Output Disable		25		30		35	ns
t_{CO}	Clock to Output	10	25	12	30	15	35	ns
t_{CF}	Clock to Feedback	10	18	12	20	15	20	ns
t_{SI1}	Input Setup Time, Output Register	10		12		15		ns
t_{SI2}	Input Setup Time, Buried Register(1)	5		5		5		ns
t_{SF}	Feedback Setup Time	7		10		15		ns
t_{H1}	Hold Time	5		5		5		ns
t_W	Clock Width	10		12		15		ns
t_P	Clock Period	25		30		35		ns
F_{MAX}	Maximum Frequency (1/tP)		40		33		28	MHz
t_{AW}	Asynchronous Reset Width	15		18		20		ns
t_{AR}	Asynchronous Reset Recovery Time	15		18		20		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		25		30		35	ns

Note: 1. Buried registers include all 24 Q2 registers and any of the 24 Q1 registers in macrocells configured as combinatorial.

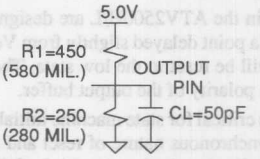
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Input Test Waveforms and Measurement Levels



tR, tF < 5 ns (10% to 90%)

Output Test Load

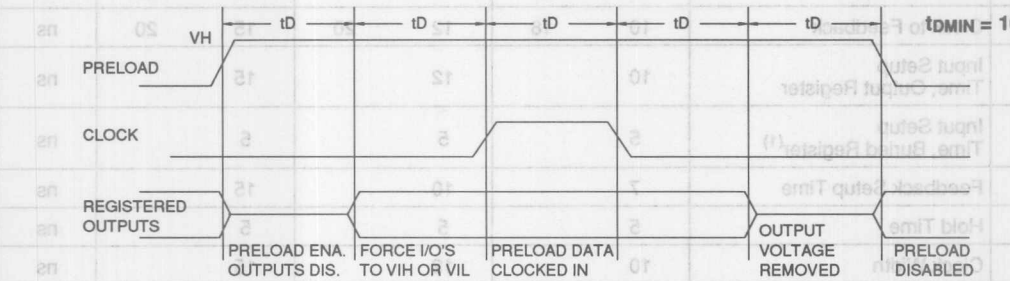


Preload and Observability of Registered Outputs

The ATV2500H/L's registers are provided with circuitry to allow loading of each register asynchronously with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A V_{IH} level on the Odd I/O pins will force the appropriate register high; a V_{IL} will force it low, independent of the polarity or other configuration bit settings.

The PRELOAD state is entered by placing an 11 V to 14 V signal on pin 38 on the DIP and pin 42 on the SMP. When the clock term is pulsed high, (pin 21 on the DIP, pin 23 on the SMP) the data on the I/O pins is placed into the 12 registers chosen by the Q Select and Even/Odd Select Pins.

Register 2 Observability Mode is entered by placing an 11 V to 14 V signal on pin 2 (DIP or SMP). In this mode, the contents of the Buried Register bank will appear on the associated outputs when the OE control signals are active.



Level forced on Odd I/O pin during PRELOAD cycle.	Q Select Pin State	Even/ Odd Select	Even Q1 state after cycle	Even Q2 state after cycle	Odd Q1 state after cycle	Odd Q2 state after cycle
V_{IH}	Low	Low	High	X	X	X
V_{IL}	Low	Low	Low	X	X	X
V_{IH}	High	Low	X	High	X	X
V_{IL}	High	Low	X	Low	X	X
V_{IH}	Low	High	X	X	High	X
V_{IL}	Low	High	X	X	Low	X
V_{IH}	High	High	X	X	X	High
V_{IL}	High	High	X	X	X	Low

Power Up Reset

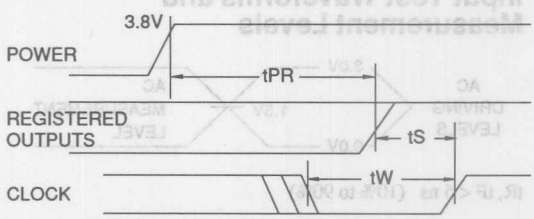
The registers in the ATV2500H/L are designed to reset during power up. At a point delayed slightly from V_{CC} crossing 3.8 V, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1) The V_{CC} rise must be monotonic,

2) After reset occurs, all input and feedback setup times must be met before driving the clock term high, and

3) The signals from which the clock is derived must remain stable during t_{PR}.



Parameter	Description	Min	Typ	Max	Units
t_{PR}	Power-Up Reset Time		600	1000	ns

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATV2500H/L fuse patterns. Once programmed, the outputs will read programmed during verify. The security fuse should be programmed last, as its effect is immediate.

The security fuse also inhibits Preload and Q2 observability.

Atmel CMOS EPLDs

Atmel's Erasable Programmable Logic Devices utilize an advanced 1.25-micron CMOS EPROM technology. This technology's state of the art features are the optimum combination for EPLDs:

- CMOS technology provides high speed, low power, and high noise immunity.
- EPROM technology is the most cost effective method for producing EPLDs - surpassing bipolar fusible link technology in low cost, while providing the necessary reprogrammability.
- EPROM reprogrammability, which is 100% tested before shipment, provides inherently better programmability and reliability than one-time fusible PLDs.
- Atmel's EPROM process has proven extremely reliable in the volume production of a full line of advanced EPROM memory products, from 64K to one-megabit devices.

Using The ATV2500's Many Advanced Features

The ATV2500H/L's flexibility puts more usable gates in 40 pins than other EPLDs. Some of the ATV2500H/L's key features are:

- Asynchronous Clocks -

Each of the Flip-Flops in the ATV2500H/L has a dedicated product term driving the clock. The user is no longer constrained to using one clock for all the registers. Buried state machines, counters, and registers can all coexist in one device, while running on separate clocks. The ATV2500H/L clock period matches that of similar synchronous devices.

- A Total of 48 Registers -

The ATV2500H/L provides two Flip-Flops for each Output Macrocell - a total of 48. Each register has its own clock and reset product terms, as well as its own SUM term.

- Independent I/O Pin and Feedback Paths -

Each I/O pin on the ATV2500/H has a dedicated input path. Each of the 48 registers has individual feedback terms into the array. This feature, combined with individual product terms for each I/O's Output Enable, facilitates designs using bi-directional I/O buses.

- Three Sum Terms per Macrocell -

The ATV2500H/L Macrocell can be configured with one Sum term feeding the output, and still have two Sum terms feeding the Flip-Flops. This is the simplest method for interfacing with an I/O bus, and no Flip-Flops need be sacrificed.

- Combinable Sum Terms -

Each Output Macrocell's three SUM terms can be combined in an OR gate before the Output or the Register. This provides up to 12 product terms per Output or Flip-Flop. When the Registered Output configuration is chosen, eight terms are automatically available to D1. The four terms feeding D2 can also be shared with D1, giving it a total of 12. In the combinatorial mode, four, eight, or 12 terms can feed the output, with the middle four still driving D1 and the bottom four still driving D2.

Programming Software Support

Software which is capable of transforming Boolean equations, state machine descriptions and truth tables into JEDEC files for the ATV2500H/L is currently available from the following sources:

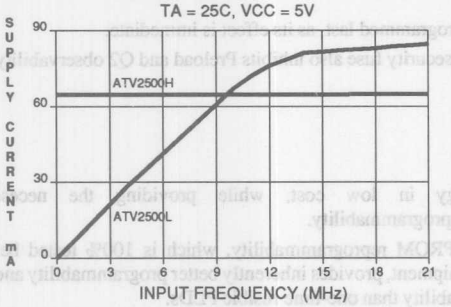
Data I/O / Futurenet Corp.	- ABEL™ 4.0 and above
Logical Devices	- CUPL 3.0 and above
Atmel Corp.	-Atmel-ABEL-4

Erasure Characteristics

The entire memory array of an ATV2500H/L is erased after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 $W \cdot sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPLD which will be subjected to continuous fluorescent indoor lighting or sunlight.

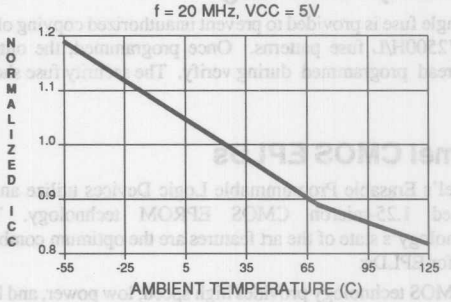
SUPPLY CURRENT vs. INPUT FREQUENCY

TA = 25C, VCC = 5V



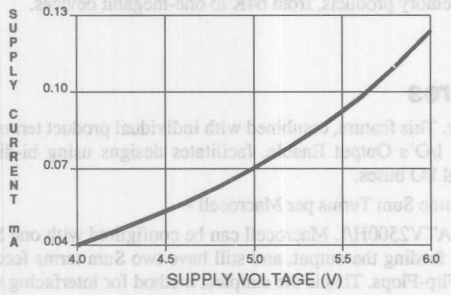
NORMALIZED ICC vs. AMBIENT TEMP.

f = 20 MHz, VCC = 5V



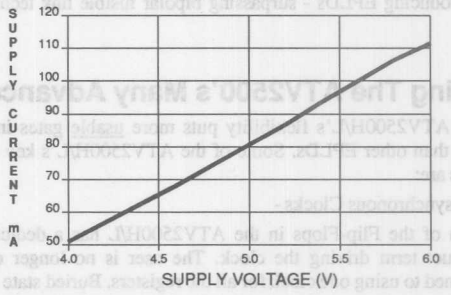
SUPPLY CURRENT vs. SUPPLY VOLTAGE

f = 0 HZ, TA = 25C



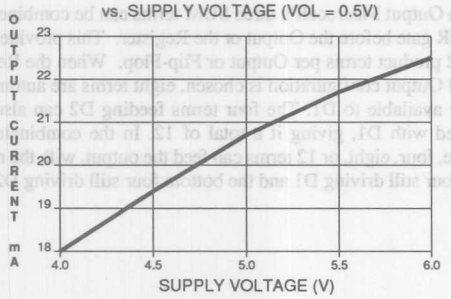
SUPPLY CURRENT vs. SUPPLY VOLTAGE

f = 20 MHz , TA = 25C



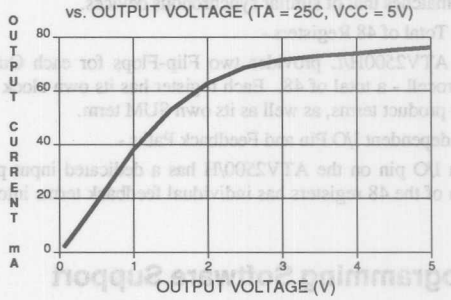
OUTPUT SINK CURRENT

vs. SUPPLY VOLTAGE (VOL = 0.5V)



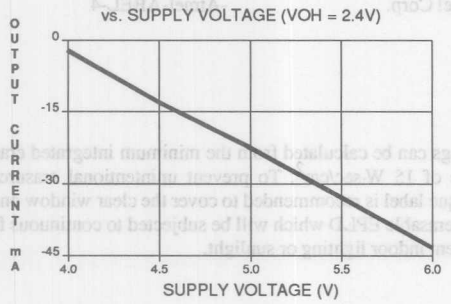
OUTPUT SINK CURRENT

vs. OUTPUT VOLTAGE (TA = 25C, VCC = 5V)



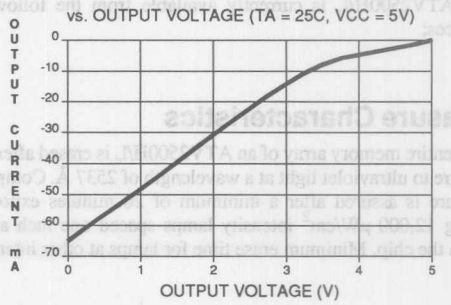
OUTPUT SOURCE CURRENT

vs. SUPPLY VOLTAGE (VOH = 2.4V)

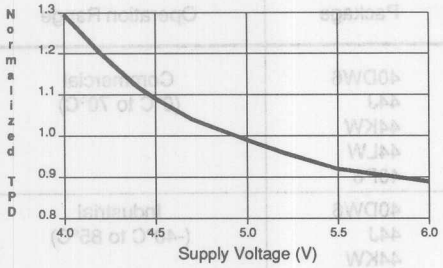


OUTPUT SOURCE CURRENT

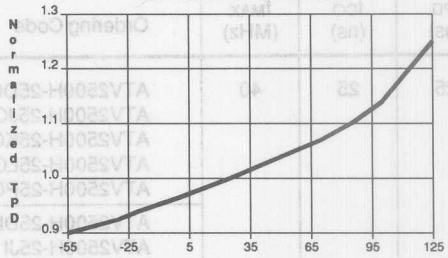
vs. OUTPUT VOLTAGE (TA = 25C, VCC = 5V)



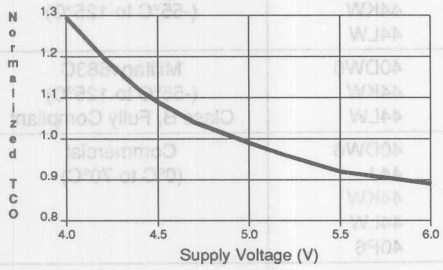
NORMALIZED TPD
vs. SUPPLY VOLTAGE



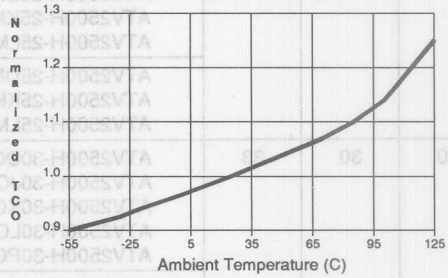
NORMALIZED TPD
vs. TEMPERATURE



NORMALIZED TCO
vs. SUPPLY VOLTAGE

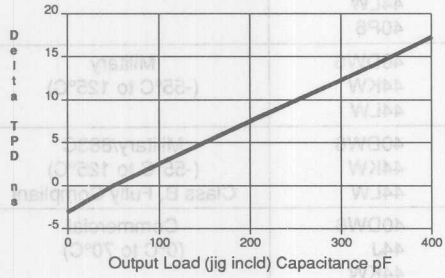


NORMALIZED TCO
vs. TEMPERATURE



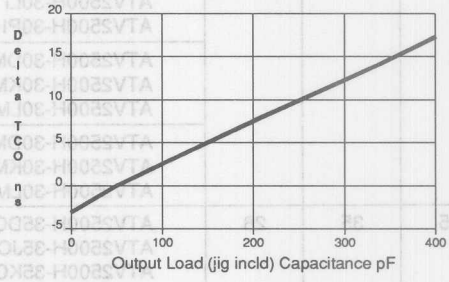
DELTA TPD vs. OUTPUT LOADING

TA = 25C, VCC = 5V



DELTA TCO vs. OUTPUT LOADING

TA = 25C, VCC = 5V



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Ordering Information

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
25	25	40	ATV2500H-25DC ATV2500H-25JC ATV2500H-25KC ATV2500H-25LC ATV2500H-25PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
			ATV2500H-25DI ATV2500H-25JI ATV2500H-25KI ATV2500H-25LI ATV2500H-25PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
			ATV2500H-25DM ATV2500H-25KM ATV2500H-25LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			ATV2500H-25DM/883 ATV2500H-25KM/883 ATV2500H-25LM/883	40DW6 44KW 44LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
30	30	33	ATV2500H-30DC ATV2500H-30JC ATV2500H-30KC ATV2500H-30LC ATV2500H-30PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
			ATV2500H-30DI ATV2500H-30JI ATV2500H-30KI ATV2500H-30LI ATV2500H-30PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
			ATV2500H-30DM ATV2500H-30KM ATV2500H-30LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			ATV2500H-30DM/883 ATV2500H-30KM/883 ATV2500H-30LM/883	40DW6 44KW 44LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
35	35	28	ATV2500H-35DC ATV2500H-35JC ATV2500H-35KC ATV2500H-35LC ATV2500H-35PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
			ATV2500H-35DI ATV2500H-35JI ATV2500H-35KI ATV2500H-35LI ATV2500H-35PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
			ATV2500H-35DM ATV2500H-35KM ATV2500H-35LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			ATV2500H-35DM/883 ATV2500H-35KM/883 ATV2500H-35LM/883	40DW6 44KW 44LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant

Ordering Information

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
25	25	40	5962-91545 02M QX 5962-91545 02M XX 5962-91545 02M YX	40DW6 44LW 44KW	Military/833C (-55°C to 125°C) Class B, Fully Compliant
30	30	33	5962-91545 01M QX 5962-91545 01M XX 5962-91545 01M YX	40DW6 44LW 44KW	Military/833C (-55°C to 125°C) Class B, Fully Compliant

Package Type	
40DW6	40 Lead, 0.600" Wide Windowed, Ceramic Dual Inline Package (Cerdip)
44J	44 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
44KW	44 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
44LW	44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
40P6	40 Lead, 0.600" Wide Plastic Dual Inline Package OTP (PDIP)

Ordering Information

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
30	30	33	ATV2500L-30DC ATV2500L-30JC ATV2500L-30KC ATV2500L-30LC ATV2500L-30PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
			ATV2500L-30DI ATV2500L-30JI ATV2500L-30KI ATV2500L-30LI ATV2500L-30PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
			ATV2500L-30DM ATV2500L-30KM ATV2500L-30LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			ATV2500L-30DM/883 ATV2500L-30KM/883 ATV2500L-30LM/883	40DW6 44KW 44LW	Military (-55°C to 125°C) Class B, Fully Compliant
35	35	28	ATV2500L-35DC ATV2500L-35JC ATV2500L-35KC ATV2500L-35LC ATV2500L-35PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
			ATV2500L-35DI ATV2500L-35JI ATV2500L-35KI ATV2500L-35LI ATV2500L-35PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
			ATV2500L-35DM ATV2500L-35KM ATV2500L-35LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			ATV2500L-35DM/883 ATV2500L-35KM/883 ATV2500L-35LM/883	40DW6 44KW 44LW	Military (-55°C to 125°C) Class B, Fully Compliant
40	40	25	ATV2500L-40DC ATV2500L-40JC ATV2500L-40KC ATV2500L-40LC ATV2500L-40PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
			ATV2500L-40DI ATV2500L-40JI ATV2500L-40KI ATV2500L-40LI ATV2500L-40PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
			ATV2500L-40DM ATV2500L-40KM ATV2500L-40LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			ATV2500L-40DM/883 ATV2500L-40KM/883 ATV2500L-40LM/883	40DW6 44KW 44LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant

Ordering Information

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
45	45	22	ATV2500L-45DI ATV2500L-45JI ATV2500L-45KI ATV2500L-45LI ATV2500L-45PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
			ATV2500L-45DM ATV2500L-45KM ATV2500L-45LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			ATV2500L-45DM/883 ATV2500L-45KM/883 ATV2500L-45LM/883	40DW6 44KW 44LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
30	30	33	5962-91545 03M QX 5962-91545 03M XX 5962-91545 03M YX	40DW6 44LW 44KW	Military/833C (-55°C to 125°C) Class B, Fully Compliant

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Package Type	
40DW6	40 Lead, 0.600" Wide Windowed, Ceramic Dual Inline Package (Cerdip)
44J	44 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
44KW	44 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
44LW	44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
40P6	40 Lead, 0.600" Wide Plastic Dual Inline Package OTP (PDIP)

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
45	45	22	ATV2500L-45DI ATV2500L-45JI ATV2500L-45KI ATV2500L-45LI ATV2500L-45PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
			ATV2500L-45DM ATV2500L-45KM ATV2500L-45LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			ATV2500L-45DM/883 ATV2500L-45KM/883 ATV2500L-45LM/883	40DW6 44KW 44LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
30	30	33	5962-91545 03M QX 5962-91545 03M XX 5962-91545 03M YX	40DW6 44LW 44KW	Military/883C (-55°C to 125°C) Class B, Fully Compliant

Package Type	
40DW6	40 Lead, 0.600" Wide Windowed, Ceramic Dual Inline Package (Cerdip)
44J	44 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
44KW	44 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
44LW	44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
40P6	40 Lead, 0.600" Wide Plastic Dual Inline Package OTP (PDIP)

Using the ATV2500 with ABEL™ and CUPL™

The following two examples show example headers to use when designing the ATV2500 with ABEL™ or CUPL™.

For ABEL™, the node numbers shown may be assigned any legal ABEL™ label. The fuse numbers for combining the product terms are included.

For CUPL™, the pinnodes shown may be assigned any legal CUPL™ label. Combining the product terms is handled automatically.

ABEL™ Example

```
module _NODE2500
title 'Addressing 48 Registers in V2500
NODE2500 device 'P2500';
      @message 'Use P2500PC device file.';
      @message 'for ABEL on a PC/Clone';
"Inputs
I1,I2,I3                              pin    1,2,3;
I17,I18,I19,I20,I21,I22,I23    pin    17,18,19,20,21,22,23;
I37,I38,I39,I40                pin    37,38,39,40;
"I/Os
O4,O5,O6,O7,O8,O9              pin    4,5,6,7,8,9;
O11,O12,O13,O14,O15,O16        pin    11,12,13,14,15,16;
O24,O25,O26,O27,O28,O29        pin    24,25,26,27,28,29;
O31,O32,O33,O34,O35,O36        pin    31,32,33,34,35,36;

"Q2 Registers
"Node Name          Node      Number        Pin Associated With:
B4,B5,B6            node      41,42,43;     " pin 4 to pin 6
B7,B8,B9            node      44,45,46;     " pin 7 to pin 9
B11,B12,B13         node      47,48,49;     " pin 11 to pin 13
B14,B15,B16         node      50,51,52;     " pin 14 to pin 16
B24,B25,B26         node      53,54,55;     " pin 24 to pin 26
B27,B28,B29         node      56,57,58;     " pin 27 to pin 29
B31,B32,B33         node      59,60,61;     " pin 31 to pin 33
B34,B35,B36         node      62,63,64;     " pin 34 to pin 36
"Q1 Registers
"Node Name          Node      Number        Pin Associated With:
Q4,Q5,Q6            node      217,218,219;  " pin 4 to pin 6
Q7,Q8,Q9            node      220,221,222;  " pin 7 to pin 9
Q11,Q12,Q13         node      223,224,225;  " pin 11 to pin 13
Q14,Q15,Q16         node      226,227,228;  " pin 14 to pin 16
Q24,Q25,Q26         node      229,230,231;  " pin 24 to pin 26
Q27,Q28,Q29         node      232,233,234;  " pin 27 to pin 29
Q31,Q32,Q33         node      235,236,237;  " pin 31 to pin 33
Q34,Q35,Q36         node      238,239,240;  " pin 34 to pin 36
```

CUPL™ Example

```
Name        NODE2500
Partno      00;
Date        11/21/88;
Revision    00;
Designer    J. Yu
Company     Atmel;
Assembly    None;
Location    None;
Device      V2500;
/*****************************************/
/** Allowable Target Device Types : V2500 **/
/*****************************************/
/**  Inputs  **/
/* This is a handy way to name a set of pins*/
PIN [1..3]      = [I1..I3];
PIN [17..23]    = [I17..I23];
PIN [37..40]    = [I37..I40];
/** I/Os        **
PIN [4..9]      = [O4..O9];
PIN [11..16]    = [O11..O16];
PIN [24..29]    = [O24..O29];
PIN [31..36]    = [O31..O36];
/** Declarations and Intermediate Variable
Definitions */
/* Q2 nodes                    Pin assoc. with:*/
PINNODE [41..46] = [B4..B9];   /*PIN 4 to 9*/
PINNODE [47..52] = [B11..B16]; /*PIN 11 to 16*/
PINNODE [53..58] = [B24..B29]; /*PIN 24 to 29*/
PINNODE [59..64] = [B31..B36]; /*PIN 31 to 36*/
/* Q1 nodes                    Pin assoc. with:*/
PINNODE [65..70] = [Q4..Q9];   /*PIN 4 to 9*/
PINNODE [71..76] = [Q11..Q16]; /*PIN 11 to 16*/
PINNODE [77..82] = [Q24..Q29]; /*PIN 24 to 29*/
PINNODE [83..88] = [Q31..Q36]; /*PIN 31 to 36*/
etc.
```

ABEL™ and CUPL™ may be trademarks of others.

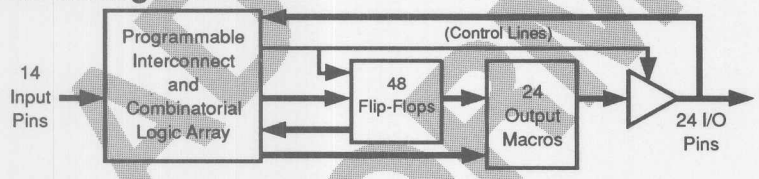
Features

- **Low Voltage Programmable Logic Device**
  - **Wide Power Supply Range - 3.0 V to 5.5 V**
  - **Ideal for Battery Powered Systems**
- **High Speed Operation**
  - **25 ns Max Propagation Delay at Vcc = 3. 0 V**
- **Third Generation Programmable Logic Structure**
  - **Easily Achieves Gate Utilization Factors of 80 Percent**
- **Increased Logic Flexibility**
  - **86 Inputs and 72 Sum Terms**
- **Flexible Output Macrocell**
  - **48 Flip-Flops - 2 per Macrocell**
  - **3 Sum Terms - Can Be OR'ed and Shared**
- **Low Power, Three-Volt CMOS Operation**

	ATV2500LVL	ATV2500LV
Temp.	Com. / Mil.	Com. / Mil.
Icc (mA)	3/ 7	60 / 80

- **Multiple Feedback Paths Provide for Buried State Machines and I/O Bus Compatibility**
- **Asynchronous Clocks and Resets**
- **Proven and Reliable High Speed CMOS EPROM Process**
  - **2000 V ESD Protection**
  - **200 mA Latchup Immunity**
- **Reprogrammable - Tested 100% for Programmability**
- **40-pin Dual-In-line and 44-Lead Surface Mount Packages**

Block Diagram



Description

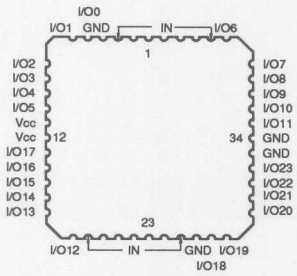
The ATV2500LV/LVL is the most powerful programmable logic device available in a 40 pin package. Increased Product terms, Sum Terms, and Flip-Flops translate into many more usable gates. High gate utilization is easily obtainable.

The ATV2500LV/LVL is organized around a global bus. All pin and feedback terms are always available to every Logic Cell. Each of the 38 logic pins and their complements are array inputs, as well as the true and false outputs of each of the 48 Flip-Flops.

(Continued on next page)

Pin Configurations

Pin Name	Function
IN	Logic Inputs
I/O	Bidirectional Buffers
I/O,0,2,4..	"Even" I/O Buffers
I/O,1,3,5..	"Odd" I/O Buffers
VCC	+5 V Supply



Low Voltage UV Erasable Programmable Logic Device

Advance Information

7

ADVANCE INFORMATION

Description (Continued)

The ATV2500LV and AT2500LVL are low voltage compatible CMOS high performance Erasable Programmable Logic Devices (EPLDs). Speeds down to 25 ns and power dissipation as low as 10.8 mW are offered. All speed ranges are specified over the 3.0 V to 5.5 V range. All pins offer a low ± 10 µA leakage.

The ATV2500LVL provides the optimum low power CMOS EPLD solution, with low D.C. power (1 mA typical at V_{CC} = 3.3 V) and full CMOS output levels. The ATV2500LVL significantly reduces total system power, allowing battery powered operation.

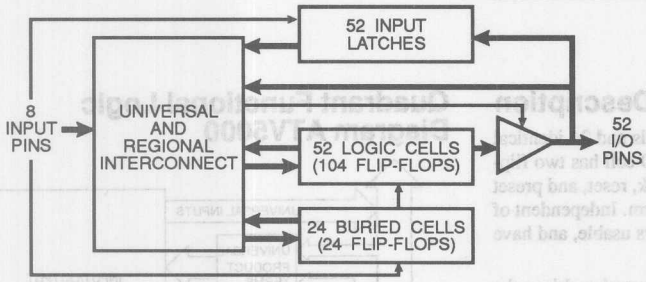
Product terms are available providing Asynchronous Resets, Flip-Flop clocks, and Output Enables. One reset and one clock term are provided per Flip-Flop, with one Enable term per output. Eight product terms provide local Synchronous Presets, divided up into banks of four and eight Flip-Flops. Register Preload and buried register observability simplify testing. The device has an internal power up clear function.

High Density UV Erasable Programmable Logic Device

Features

- **Advanced Programmable Logic Device - High Gate Utilization**
- **Flexible Interconnect Architecture - Universal Routing**
- **Flexible Logic Cells - 128 Flip-Flops and 52 Latches**
- **Multiple Flip-Flop Types - Synchronous or Asynchronous Registers**
- **High Speed - 50 MHz Operation**
- **Complete Third Party Software Support**
  No Placement, Routing or Layout Software Required
- **Proven and Reliable High Speed CMOS EPROM Process**
  2000 V ESD Protection
  200 mA Latchup Immunity
- **Reprogrammable - Tested 100% for Programmability**
- **Commercial, Industrial and Military Temperature Grades**

Block Diagram



Description

The Atmel V5000 is an easy to use, high density programmable logic device. Its simple, regular architecture translates into increased utilization and high performance.

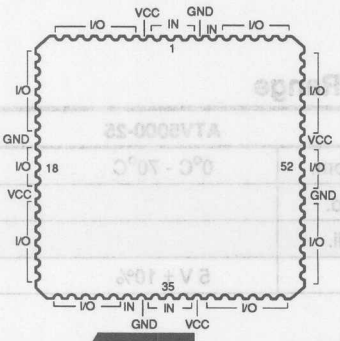
The ATV5000 has one programmable combinatorial logic array. This guarantees easy interconnection of and uniform performance from all nodes. "Sum terms", which are easy to use groupings of AND-OR gates, provide combinatorial logic blocks. Sum terms can be wire-OR'd together to integrate larger logic blocks. To expand the levels of logic, buried sum terms feed back into the logic array. The 52 I/O pins can each be driven by a register or a sum term. Each I/O pin has an individually enabled input latch.

All 128 registers are configurable as D- or T-types without using extra logic gates. Individual sum terms, asynchronous presets, resets and clocks give each flip-flop added flexibility. A direct "clock from pin" option guarantees synchronization and fast clock to output performance.

Standard, off-the-shelf third-party software tools and programmers support the ATV5000. This minimizes start-up investment and improves product support.

Chip Carrier Pin Configuration

Pin Name	Function
IN	Logic and Clock Inputs
Pins 2,32,36,66	Input/Register Clocks 1-4
Pins 1,34,35,68	Input/Latch Clocks 1-4
I/O	Bidirectional Buffers
VCC	+5 V Supply



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V[1]
Voltage on Input Pins with Respect to Ground During Programming	-2.0 V to +14.0 V[1]
Programming Voltage with Respect to Ground	-2.0 V to +14.0 V[1]
Integrated UV Erase Dose	7258 W·sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:

1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC}+0.75 V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

Functional Logic Diagram Description

There are 52 identical Input/Ouput logic cells and 24 identical buried logic cells in the ATV5000. Each I/O cell has two flip-flops, up to three sum terms, individual clock, reset, and preset terms per flip-flop, and one output enable term. Independent of output configuration, all flip-flops are always usable, and have at least four Product Term inputs each.

Each I/O pin (52 total) signal or its latched version drives the logic array. There is one latch clock per quadrant.

The ATV5000 has four identical quadrants (see Figure 2). The Universal Bus routes true and false signals from each of the 52 I/O pins to all four quadrants. Regional buses route each quadrant's flip-flop Q and $\overline{Q}$ locally. The eight input-only pins are available in all four regional buses.

Each logic cell has a number of "regional" and "universal" product terms (see Figure 1). The I/O Logic Cells contain three sum terms, two flip-flops, and an I/O buffer.

The Buried Logic Cells each contain one Flip-flop. In addition, in each buried logic cell the sum term can drive the regional bus. This allows for logic expansion.

Serial register preload and observability simplify testing. All registers automatically clear at power up.

Quadrant Functional Logic Diagram ATV5000

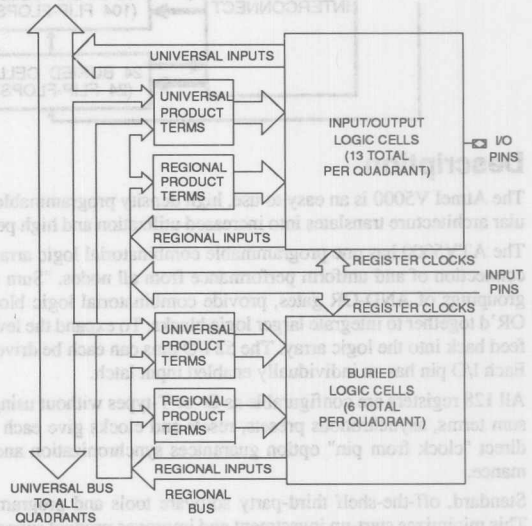


Figure 1

D.C. and A.C. Operating Range

		ATV5000-25	ATV5000/L-30	ATV5000/L-35
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.		-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 10%	5 V ± 10%	5 V ± 10%

ATV5000 Block Diagram

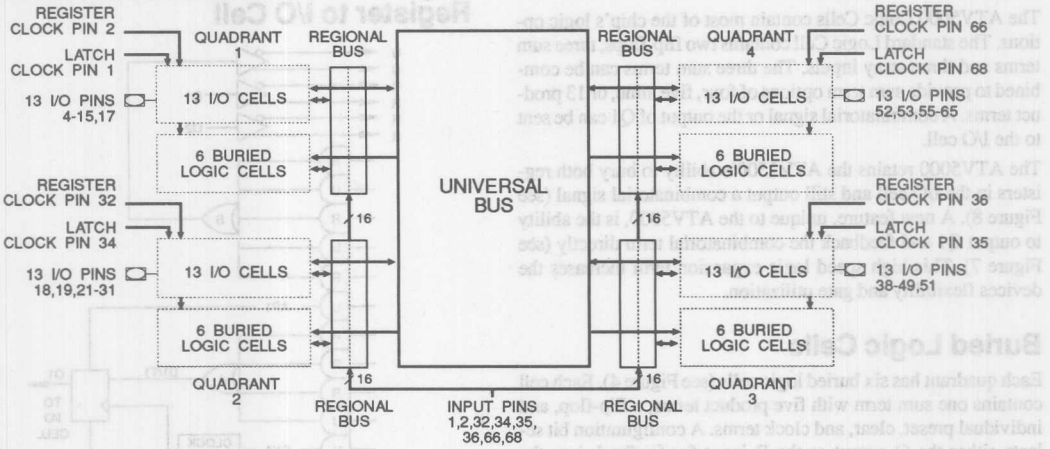


Figure 2

Quadrant Logic Diagram and Description

The ATV5000 has: four identical quadrants, 52 identical input/output logic cells, and 24 identical buried logic cells. The Universal Bus routes true and false signals from each of the 52 I/O pins to all four quadrants. Regional buses route each quadrant's flip-flop Q and $\overline{Q}$ locally. The eight input-only pins are available in every Regional Bus.

Each logic cell has a number of "regional" and "universal" product terms (see Figure 3). The I/O Logic Cells (Figures 7, 8, 9) contain three sum terms, two flip-flops, and an I/O buffer. Sum term B has five product terms - two universal and three regional. Sum terms A and C each have four product terms - one universal and three regional. Flip-flop Q1 has global Asynchronous Preset, Reset, and Clock product terms. Flip-flop Q2 has universal Asynchronous Reset and Clock terms and a regional Asynchronous Preset term. There is one universal product term for the I/O pin Output Enable.

The Buried Logic Cells (Figure 4) each contain one flip-flop. The sum term has one universal product term and four regional product terms for a total of five. The flip-flop has universal Asynchronous Preset, Reset, and Clock terms. In addition, in each buried logic cell the sum term can be fed back into the regional bus instead of the flip-flop. This allows for logic expansion.

Regional product terms have as inputs all quadrant flip-flop outputs (or buried flip flop inputs) and the eight dedicated input pins. Universal product terms have the same inputs plus the 52 I/O pins and their complements.

Quadrant Clock Pin Assignments

Quadrant Number	Register Clock Pin	Latch Clock Pin
1	2	1
2	32	34
3	36	35
4	66	68

Quadrant Structure

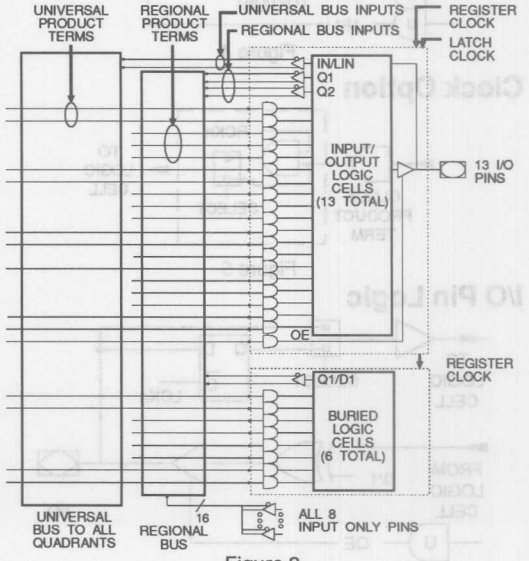


Figure 3

Logic Cell Options

The ATV5000 Logic Cells contain most of the chip's logic options. The standard Logic Cell contains two flip-flops, three sum terms and three array inputs. The three sum terms can be combined to provide sum term options of four, five, nine, or 13 product terms. A combinatorial signal or the output of Q1 can be sent to the I/O cell.

The ATV5000 retains the ATV2500's ability to bury both registers in the I/O cell and still output a combinatorial signal (see Figure 8). A new feature, unique to the ATV5000, is the ability to output Q1 and feedback the combinatorial term directly (see Figure 7). This high speed logic expansion term increases the devices flexibility and gate utilization.

Buried Logic Cells

Each quadrant has six buried logic cells (see Figure 4). Each cell contains one sum term with five product terms, a flip-flop, and individual preset, clear, and clock terms. A configuration bit selects either the Q output or the D input for feedback into the regional bus.

Buried Logic Cells

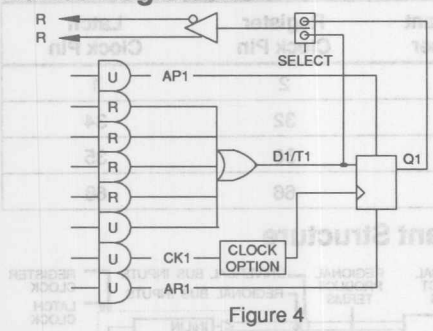


Figure 4

Clock Option

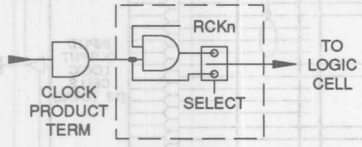


Figure 5

I/O Pin Logic

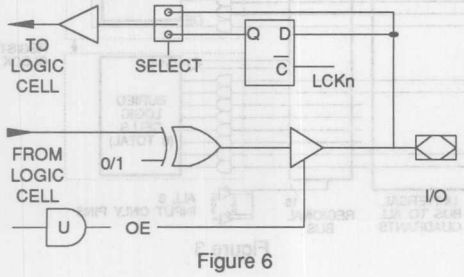


Figure 6

Logic Cell with Buried Sum Term and Register to I/O Cell

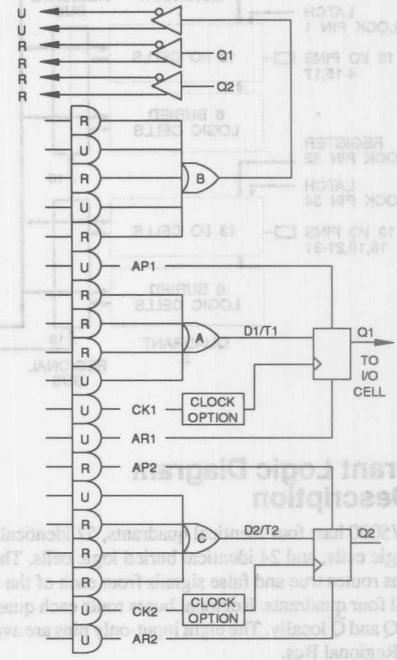


Figure 7

Flip-Flop Clock Options

Each register may be connected to its regional clock to provide fast clock to output timing (see Figure 5). In this "synchronous" mode, the clock is one of four input pins, a unique clock pin for each chip quadrant. One product term defines each flip-flop's clock in the "asynchronous" mode.

In the "synchronous" mode, the regional clock is ANDed with the product term. This provides the fast timing of a synchronous clock with the local control of the product term.

I/O Pin Latches

Each I/O pin of the ATV5000 has an input latch which can be individually enabled or disabled (see Figure 6). Each chip quadrant has a unique latch clock. When the latch is inactive, pin input flows directly into the array. When activated, the latch is flow-through when the clock signal is low, and data is captured on the clock's rising edge.

Flip-Flop Types

Each flip-flop in the ATV5000 may be configured as either a T- or D-type flip-flop. A T-type flip-flop can also easily be configured into a JK or SR flip-flop.

Logic Cell, Two Buried Registers, Combinatorial to I/O Cell

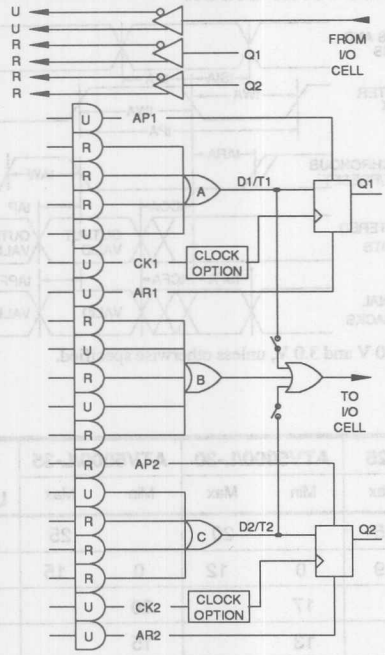


Figure 8

Logic Cell with Combinable Sum Terms, Register to I/O Cell

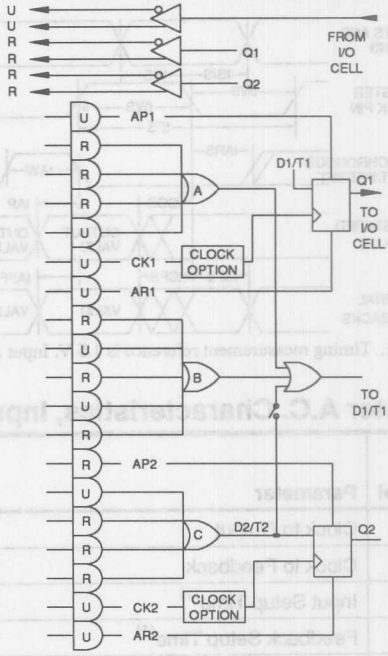


Figure 9

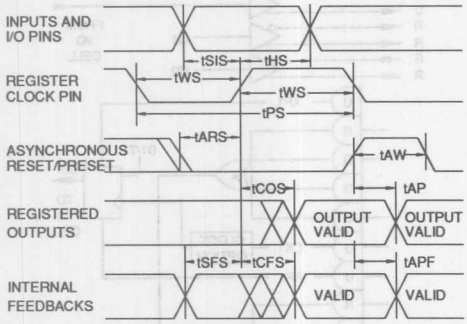
7

D.C. Characteristics

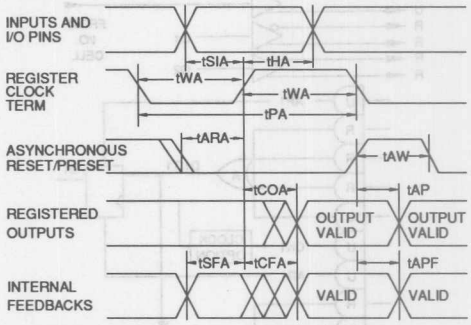
Symbol	Parameter	Condition		Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1 V to V_{CC}+1 V				10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1 V to V_{CC}+0.1 V				10	µA
I_{CC}	Power Supply Current ATV5000	V_{CC} = MAX, V_{IN} = GND or V_{CC} Outputs Open	Com.		200	350	mA
			Ind.,Mil.		200	400	mA
I_{CC}	Power Supply Current ATV5000L	V_{CC} = MAX, V_{IN} = GND or V_{CC} Outputs Open	Com.		32	40	mA
			Ind.,Mil.		32	50	mA
I_{CC2}	Clocked Power Supply Current, ATV5000L Only	f = 1 MHz, V_{CC} = MAX Outputs Open	Com.		30	50	mA
			Ind.,Mil.		30	60	mA
I_{OS} (1)	Output Short Circuit Current	V_{OUT} = 0.5 V				-90	mA
V_{IL}	Input Low Voltage			-0.6		0.8	V
V_{IH}	Input High Voltage			2.0		V_{CC}+0.75	V
V_{OL}	Output Low Voltage	V_{IN} = V_{IH} or V_{IL}, I_{OL} = 8 mA Com,Ind; 6 mA Mil.				0.5	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA		V_{CC}-0.3			V
		I_{OH} = -4.0 mA		2.4			V

Note: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 seconds.

A.C. Waveforms[1] Input Pin Clock



A.C. Waveforms[1] Product Term Clock



Notes: 1. Timing measurement reference is 1.5 V. Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.

Register A.C. Characteristics, Input Pin Clock

Symbol	Parameter	ATV5000-25 Min	ATV5000-25 Max	ATV5000/L-30 Min	ATV5000/L-30 Max	ATV5000/L-35 Min	ATV5000/L-35 Max	Units
t_{COS}	Clock to Output		15		20		25	ns
t_{CFS}	Clock to Feedback	0	9	0	12	0	15	ns
t_{SIS}	Input Setup Time[1]	16		17		20		ns
t_{SFS}	Feedback Setup Time[1]	11		13		15		ns
t_{HS}	Hold Time	0		0		0		ns
t_{WS}	Clock Width	10		12		15		ns
t_{PS}	Clock Period	20		25		30		ns
F_{MAXS}	Maximum Frequency (1/t_{PS})		50		40		33	MHz
t_{ARS}	Asynchronous Reset/Preset Recovery Time	20		25		30		ns

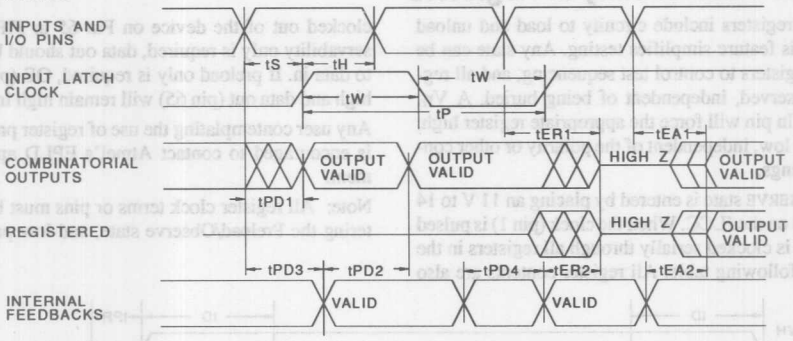
Note: 1. Add 3 ns for Universal Product Terms.

Register A.C. Characteristics, Product Term Clock

Symbol	Parameter	ATV5000-25 Min	ATV5000-25 Max	ATV5000/L-30 Min	ATV5000/L-30 Max	ATV5000/L-35 Min	ATV5000/L-35 Max	Units
t_{COA}	Clock to Output		25		30		35	ns
t_{CFA}	Clock to Feedback	7	20	10	25	12	27	ns
t_{SIA}	Input Setup Time[1]	10		12		15		ns
t_{SFA}	Feedback Setup Time[1]	5		8		13		ns
t_{HA}	Hold Time	8		10		12		ns
t_{WA}	Clock Width	12		15		15		ns
t_{PA}	Clock Period	25		33		40		ns
F_{MAXA}	Maximum Frequency (1/t_{PA})		40		30		25	MHz
t_{ARA}	Asynchronous Reset/Preset Recovery Time	15		20		25		ns

Note: 1. Add 3 ns for Universal Product Terms.

A.C. Waveforms [1]



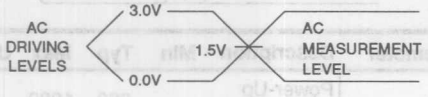
Notes: 1. Timing measurement reference is 1.5 V. Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.

A.C. Characteristics

Symbol	Parameter	ATV5000-25 Min	ATV5000-25 Max	ATV5000/L-30 Min	ATV5000/L-30 Max	ATV5000/L-35 Min	ATV5000/L-35 Max	Units
t_{PD1}	Input to Non-Registered Output[1]		25		30		35	ns
t_{PD2}	Feedback to Non-Registered Output[1]		20		25		30	ns
t_{PD3}	Input to Non-Registered Feedback[1]		20		25		30	ns
t_{PD4}	Feedback to Non-Registered Feedback[1]		15		18		22	ns
t_{EA1}	Input to Output Enable		30		35		40	ns
t_{ER1}	Input to Output Disable		30		35		40	ns
t_{EA2}	Feedback to Output Enable		25		30		35	ns
t_{ER2}	Feedback to Output Disable		25		30		35	ns
t_S	Input Latch Setup Time	5		6		7		ns
t_H	Input Latch Hold Time	5		5		5		ns
t_W	Clock Width	10		12		12		ns
t_P	Clock Period	20		25		30		ns
F_{MAX}	Maximum Frequency ($1/t_P$)		50		40		33	MHz
t_{AW}	Asynchronous Reset/Preset Width	15		20		20		ns
t_{AP}	Asynchronous Reset/ Preset to Registered Output		30		35		40	ns
t_{APF}	Asynchronous Reset/ Preset to Registered Feedback		25		30		35	ns

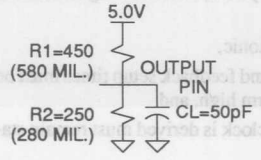
Note: 1. Add 3 ns for Universal Product Terms.

Input Test Waveforms and Measurement Levels



t_R, t_F < 5 ns (10% to 90%)

Output Test Load



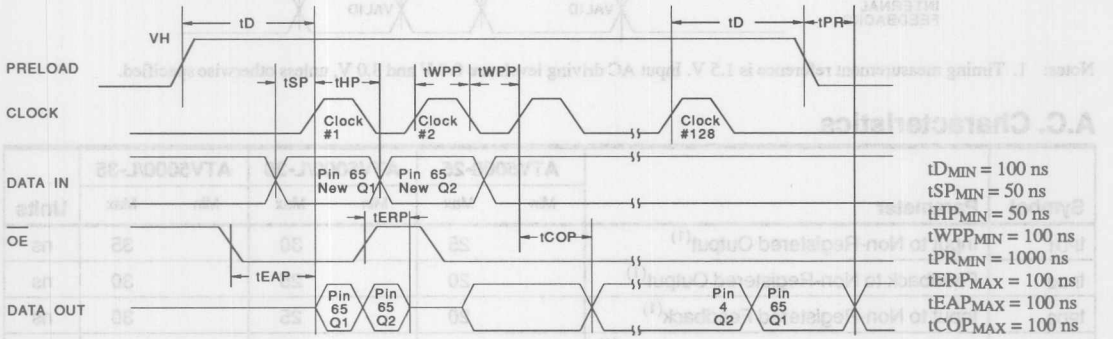
Preload and Observability of Registers

The ATV5000's registers include circuity to load and unload them serially. This feature simplifies testing. Any state can be forced into the registers to control test sequencing, and all registers may be observed, independent of being buried. A V_{IH} level on the Data In pin will force the appropriate register high; a V_{IL} will force it low, independent of the polarity or other configuration bit settings.

The PRELOAD/OBSERVE state is entered by placing an 11 V to 14 V signal on pin 68 on the JLCC. When the clock (pin 1) is pulsed high, data (pin 2) is clocked serially through all registers in the device, as in the following table. All register contents are also clocked out of the device on Pin 65 in FIFO fashion. If observability only is required, data out should be connected back to data in. If preload only is required, OE (pin 66) can be held high and data out (pin 65) will remain high impedance.

Any user contemplating the use of register preload/obervability is encouraged to contact Atmel's EPLD applications department.

Note: All register clock terms or pins must be low prior to entering the Preload/Observe state, and low prior to leaving the



Preload / Observe Register Scan Order

Quadrant	Pin																					
Quadrant 1	Pin	4				5			6			•••		15			17					
	D_{IN}	→ Q2	→ Q1	→ B23	→ Q2	→ Q1	→ Q2	→ Q1		•••	B18	→ Q2	→ Q1	→ Q2	→ Q1	→ (Quadrant 2)						
Quadrant 2	Pin	18			19				21			22		•••			31					
(Quadrant 1)→		Q2	→ Q1	→ Q2	→ Q1	→ B17	→ Q2	→ Q1	→ Q2	→ Q1	•••	B12	→ Q2	→ Q1	→ (Quadrant 3)							
Quadrant 3	Pin	38				39			40			•••		49			51					
(Quadrant 2)→		Q2	→ Q1	→ B11	→ Q2	→ Q1	→ Q2	→ Q1		•••	B6	→ Q2	→ Q1	→ Q2	→ Q1	→ (Quadrant 4)						
Quadrant 4	Pin	52				53			55			56		•••			65					
(Quadrant 3)→		Q2	→ Q1	→ Q2	→ Q1	→ B5	→ Q2	→ Q1	→ Q2	→ Q1	•••	B0	→ Q2	→ Q1	→ D_{OUT}							

Power Up Reset

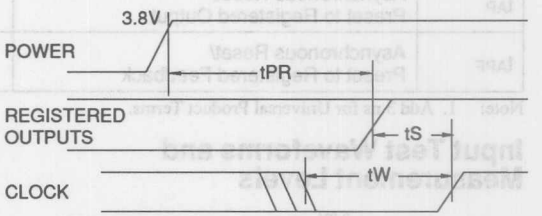
The registers in the ATV5000 are designed to reset during power up. At a point delayed slightly from V_{CC} crossing 3.8 V, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1) The V_{CC} rise must be monotonic,

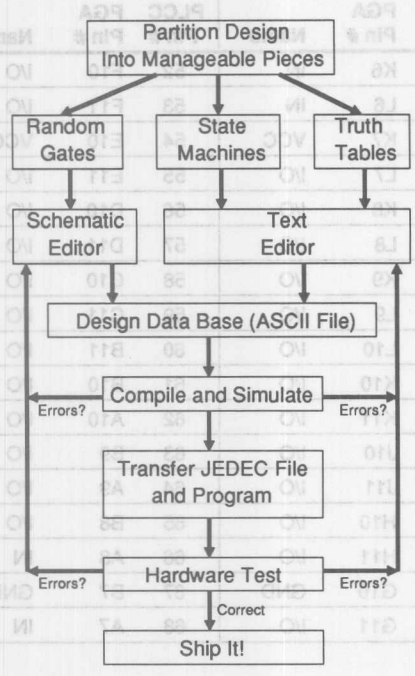
2) After reset occurs, all input and feedback setup times must be met before driving the clock term high, and

3) The signals from which the clock is derived must remain stable during t_{PR}.



Parameter	Description	Min	Typ	Max	Units
t_{PR}	Power-Up Reset Time		600	1000	ns

Design Flow Diagram



Using The ATV5000

The ATV5000's simple, regular architecture means that only simple logic compilers are required to configure the device. No layout or route and place are required. These software tools are readily available from companies such as Data I/O Corporation (ABEL™), Logical Devices (CUPL™), and ISDATA (LOGiC™).

The first step in designing a device as complex as the ATV5000 is to partition your design into manageable blocks. These blocks are then allocated proportionally to each of the four quadrants of the ATV5000. Random gates can be described either with boolean equations (a behavioral description) or with a schematic editor. Truth table logic and state machines are best described behaviorially and entered with a text editor. The design is then combined into one ASCII file, which is then submitted to the logic compiler. Compilation, logic reduction, simulation, JEDEC file creation and documentation are then completed by all of the popular compilers.

Assignment of signals to pins or buried nodes as well as selecting the various options of the ATV5000 (such as register clocks and input latches) can be done manually in the design data base file, or an automatic fitter may be used.

A logic fitter assigns pins and nodes to make best use of the features in the ATV5000, and frees the designer from being required to learn all of the features of a complex device such as the ATV5000. For further information on fitters for the ATV5000, contact Atmel's EPLD applications department.

After correcting any syntax and logic errors discovered by the compiler, the JEDEC file is ready to download to an EPLD programmer. These are available from a number of manufacturers. Programmed devices are usually first tested in the programmer with your supplied test vectors. The next step is check out your "custom chip" in the target system. When this hardware debug step is complete, your system is ready to go— all in a matter of hours.

ABEL™, CUPL™ and LOGiC™ may be trademarks of others.

7

Operating Modes

	68-Lead LCC Pin								
Mode	1	2	36	34	68	66	Vcc (3,20,37,54)	I/O's	I/O Pin 65
"EPLD"	X (1)	X	X	X	X	X	5V	I/O	I/O
Program	V_{PP}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	6V	ADD/D_{IN}	ADD
PGM Verify	V_{PP}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	X	6V	ADD/D_{OUT}	ADD
PGM Inhibit	V_{PP}	V_{IH}	V_{IH}	V_{IH}	V_{IH}	X	6V	High Z	High Z
Preload/Observe	⎍	D_{IN}	X	X	V_H (2)	$\overline{OE}$	5V	High Z	D_{OUT}

Notes: 1. X can be V_{IL} or V_{IH}.
2. V_H = 11.0 V to 14.0 V

ATV5000 PLCC/PGA Pin Assignments

PLCC Pin #	PGA Pin #	Name	PLCC Pin #	PGA Pin #	Name	PLCC Pin #	PGA Pin #	Name	PLCC Pin #	PGA Pin #	Name
1	B6	IN	18	F2	I/O	35	K6	IN	52	F10	I/O
2	A6	IN	19	F1	I/O	36	L6	IN	53	F11	I/O
3	B5	VCC	20	G2	VCC	37	K7	VCC	54	E10	VCC
4	A5	I/O	21	G1	I/O	38	L7	I/O	55	E11	I/O
5	B4	I/O	22	H2	I/O	39	K8	I/O	56	D10	I/O
6	A4	I/O	23	H1	I/O	40	L8	I/O	57	D11	I/O
7	B3	I/O	24	J2	I/O	41	K9	I/O	58	C10	I/O
8	A3	I/O	25	J1	I/O	42	L9	I/O	59	C11	I/O
9	A2	I/O	26	K1	I/O	43	L10	I/O	60	B11	I/O
10	B2	I/O	27	K2	I/O	44	K10	I/O	61	B10	I/O
11	B1	I/O	28	L2	I/O	45	K11	I/O	62	A10	I/O
12	C2	I/O	29	K3	I/O	46	J10	I/O	63	B9	I/O
13	C1	I/O	30	L3	I/O	47	J11	I/O	64	A9	I/O
14	D2	I/O	31	K4	I/O	48	H10	I/O	65	B8	I/O
15	D1	I/O	32	L4	IN	49	H11	I/O	66	A8	IN
16	E2	GND	33	K5	GND	50	G10	GND	67	B7	GND
17	E1	I/O	34	L5	IN	51	G11	I/O	68	A7	IN

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	6	8	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATV5000 fuse patterns. Once programmed, all outputs appear programmed during verify. The security fuse should be programmed last (after verifying all other programmed bits), as its effect is immediate.

The security fuse also inhibits Preload and Observability.

Erasure Characteristics

The entire memory array of an ATV5000 is erased after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 $W \cdot sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPLD which will be subjected to continuous fluorescent indoor lighting or sunlight.

Ordering Information

t_{PD} (ns)	t_{COS} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
25	15	50	ATV5000-25JC ATV5000-25KC ATV5000-25UC	68J 68KW 68UW	Commercial (0°C to 70°C)
30	20	40	ATV5000-30JC ATV5000-30KC ATV5000-30UC	68J 68KW 68UW	Commercial (0°C to 70°C)
			ATV5000-30KI ATV5000-30UI	68KW 68UW	Industrial (-40°C to 85°C)
			ATV5000-30KM ATV5000-30UM	68KW 68UW	Military (-55°C to 125°C)
			ATV5000-30KM/883 ATV5000-30UM/883	68KW 68UW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
35	25	33	ATV5000-35JC ATV5000-35KC ATV5000-35UC	68J 68KW 68UW	Commercial (0°C to 70°C)
			ATV5000-35KI ATV5000-35UI	68KW 68UW	Industrial (-40°C to 85°C)
			ATV5000-35KM ATV5000-35UM	68KW 68UW	Military (-55°C to 125°C)
			ATV5000-35KM/883 ATV5000-35UM/883	68KW 68UW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

7

Package Type	
68J	68 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
68KW	68 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
68UW	68 Pin, Windowed, Ceramic Pin Grid Array (PGA)

Ordering Information

t_{PD} (ns)	t_{COS} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
30	20	40	ATV5000L-30JC ATV5000L-30KC ATV5000L-30UC	68J 68KW 68UW	Commercial (0°C to 70°C)
35	25	33	ATV5000L-35JC ATV5000L-35KC ATV5000L-35UC	68J 68KW 68UW	Commercial (0°C to 70°C)
			ATV5000L-35KI ATV5000L-35UI	68KW 68UW	Industrial (-40°C to 85°C)
			ATV5000L-35KM ATV5000L-35UM	68KW 68UW	Military (-55°C to 125°C)
			ATV5000L-35KM/883 ATV5000L-35UM/883	68KW 68UW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

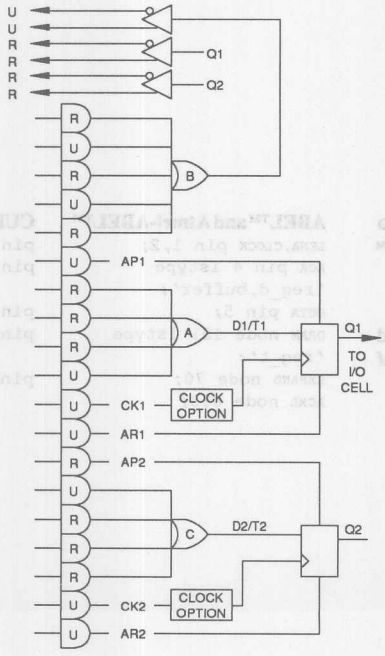
Package Type	
68J	68 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
68KW	68 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
68UW	68 Pin, Windowed, Ceramic Pin Grid Array (PGA)

Using the ATV5000

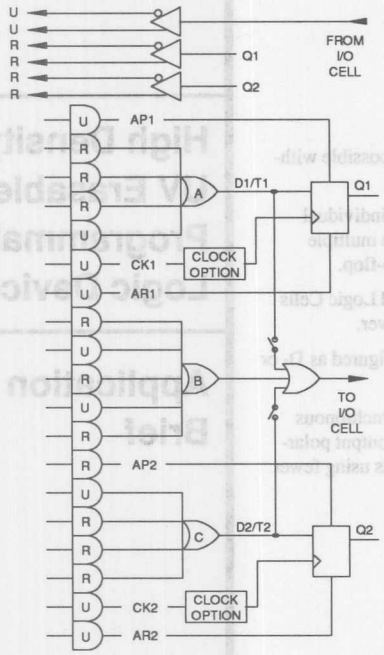
The ATV5000 Logic Cells retain the ATV2500's basic features with two registers, three sum terms and Q1, Q2, and pin feedback options. In addition, these following features make the ATV5000 even more versatile:

1. Input latches are added to every I/O pin. Each latch can be enabled or disabled independently.
2. The ATV5000 can be configured to feedback a combinatorial sum term and send Q1 to the output. Feeding the combinatorial sum term internally makes implementing logic equations with large number of product terms possible without sacrificing an I/O pin.
3. Dedicated clock pins and individual clock product terms create multiple clock options for each flip-flop.
4. The addition of the Buried Logic Cells handles more logic than ever.
5. Each flip-flop can be configured as D- or T-type flip-flop.
6. Asynchronous Preset, Asynchronous Reset and programmable output polarity allow registered outputs using fewer product terms.

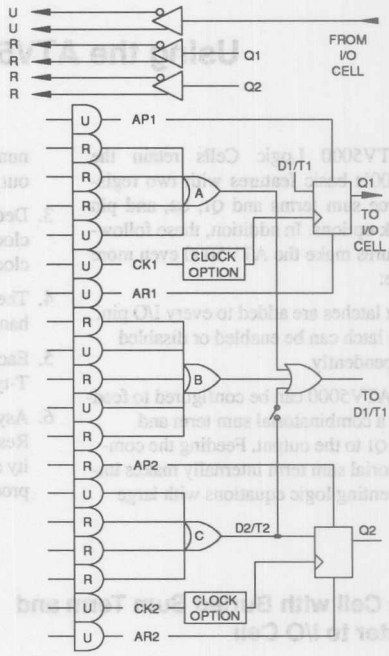
Logic Cell with Buried Sum Term and Register to I/O Cell



Logic Cell, Two Buried Registers, Combinatorial to I/O Cell



Logic Cell with Combinable Sum Terms, Register to I/O Cell



The following are sections of ABEL™ and CUPL™ source files to illustrate how each of these features is described in the ABEL™ and CUPL™ high level description languages.

Pin and Node Assignments

All the buried registers used in the design need to be assigned node numbers. The following tables show the complete set of node numbers by quadrant.

ABEL™ and Atmel-ABEL™

```
LENA,CLOCK pin 1,2;
ACK pin 4 istype
'reg_d,buffer';
OUTA pin 5;
DRAM node 121 istype
'reg_t';
EXPAND node 70;
ACKL node 813;
```

CUPL™

```
pin 1,2 = LENA,CLOCK;
pin 4 = ACK;

pin 5 = OUTA;
pinnode 105 = DRAM;

pinnode 208 = EXPAND;
```

Quadrant I

Pin	Input Latch	Sum Term A	Sum Term B	Sum Term C
4	813	761	69	121
5	814	762	70	122
6	815	763	71	123
7	816	764	72	124
8	817	765	73	125
9	818	766	74	126
10	819	767	75	127
11	820	768	76	128
12	821	769	77	129
13	822	770	78	130
14	823	771	79	131
15	824	772	80	132
17	825	773	81	133

6 Buried Logic Cells
B23 - B18 node 173 - 178
LCK1 pin 1; Quadrant Latch clock
RCK1 pin 2; Quadrant Synchronous Register Clock

Quadrant II

Pin	Input Latch	Sum Term A	Sum Term B	Sum Term C
18	826	774	82	134
19	827	775	83	135
21	828	776	84	136
22	829	777	85	137
23	830	778	86	138
24	831	779	87	139
25	832	780	88	140
26	833	781	89	141
27	834	782	90	142
28	835	783	91	143
29	836	784	92	144
30	837	785	93	145
31	838	786	94	146

6 Buried Logic Cells
B17 - B12 node 179 - 184
LCK2 pin 34; Quadrant Latch Clock
RCK2 pin 32; Quadrant Synchronous Register Clock

Quadrant III

Pin	Input Latch	Sum Term A	Sum Term B	Sum Term C
38	839	787	95	147
39	840	788	96	148
40	841	789	97	149
41	842	790	98	150
42	843	791	99	151
43	844	792	100	152
44	845	793	101	153
45	846	794	102	154
46	847	795	103	155
47	848	796	104	156
48	849	797	105	157
49	850	798	106	158
51	851	799	107	159

6 Buried Logic Cells
B11 - B6 node 185 - 190
LCK3 pin 35; Quadrant Latch Clock
RCK3 pin 36; Quadrant Synchronous Register Clock

Quadrant IV

Pin	Input Latch	Sum Term A	Sum Term B	Sum Term C
52	852	800	108	160
53	853	801	109	161
55	854	802	110	162
56	855	803	111	163
57	856	804	112	164
58	857	805	113	165
59	858	806	114	166
60	859	807	115	167
61	860	808	116	168
62	861	809	117	169
63	862	810	118	170
64	863	811	119	171
65	864	812	120	172

6 Buried Logic Cells
B5 - B0 node 191 - 196
LCK4 pin 68; Quadrant Latch Clock
RCK4 pin 66; Quadrant Synchronous Register Clock

Quadrant I

Sum Term

Pin	A	B	C
4	157	209	105
5	156	208	104
6	155	207	103
7	154	206	102
8	153	205	101
9	152	204	100
10	151	203	99
11	150	202	98
12	149	201	97
13	148	200	96
14	147	199	95
15	146	198	94
17	145	197	93

6 Buried Logic Cells
B23 - B18 node 74 - 69
LCK1 pin 1; Quadrant Latch Clock
RCK1 pin 2; Quadrant Synchronous Register Clock

Quadrant II

Sum Term

Pin	A	B	C
18	158	210	106
19	159	211	107
21	160	212	108
22	161	213	109
23	162	214	110
24	163	215	111
25	164	216	112
26	165	217	113
27	166	218	114
28	167	219	115
29	168	220	116
30	169	221	117
31	170	222	118

6 Buried Logic Cells
B17 - B12 node 75 - 80
LCK2 pin 34; Quadrant Latch Clock
RCK2 pin 32; Quadrant Synchronous Register Clock

Quadrant III

Sum Term

Pin	A	B	C
38	183	235	131
39	182	234	130
40	181	233	129
41	180	232	128
42	179	231	127
43	178	230	126
44	177	229	125
45	176	228	124
46	175	227	123
47	174	226	122
48	173	225	121
49	172	224	120
51	171	223	119

6 Buried Logic Cells
B11 - B6 node 86 - 81
LCK3 pin 35; Quadrant Latch Clock
RCK3 pin 36; Quadrant Synchronous Register Clock

Quadrant IV

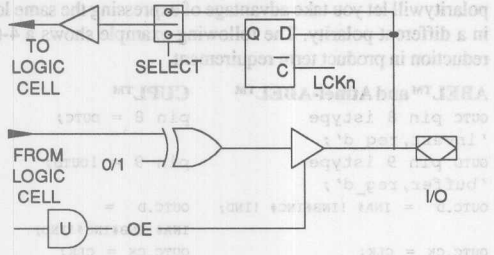
Sum Term

Pin	A	B	C
52	184	236	132
53	185	237	133
55	186	238	134
56	187	239	135
57	188	240	136
58	189	241	137
59	190	242	138
60	191	243	139
61	192	244	140
62	193	245	141
63	194	246	142
64	195	247	143
65	196	248	144

6 Buried Logic Cells
B5 - B0 node 87 - 92
LCK4 pin 68; Quadrant Latch Clock
RCK4 pin 66; Quadrant Synchronous Register Clock

Input Latch

Each of the 52 I/Os has an input latch that can be enabled and disabled individually. When the latch is enabled and latch clock is high, the pin value is latched. When the quadrant latch clock is low, the latch becomes transparent. When the latch is disabled, an ATV5000 I/O acts like those of the ATV750 and ATV2500 I/Os. The pin input is fed directly to the array (except when sum term B is being used as a buried feedback).



The .D and the .LE (latch enable) equations are required to enable the input latch in ABEL™ AHDL. The only allowed input to the latch is the IO pin with which it is associated. The only allowed .LE input is the quadrant latch clock (pin 1,34, 35, or 68). Notice that CUPL™ does not have node numbers for the input latches. Any pin name used in a feedback with the dot extension IOL tells CUPL™ that particular pin should be a latched pin.

ABEL™ and Atmel-ABEL™

```
ACKL.D  = ACK;
ACKL.LE = LENA;
OUTA := ACKL;
```

CUPL™

```
OUTA.D = ACK.IOL;
```

Internal Combinatorial Feedback for an I/O Cell

To implement the combinatorial feedback of the B sum term, first define the node name with the corresponding node number. This node will take a five-product term equation. Regular syntax describing a combinatorial equation will describe the B sum term.

Note: This B sum term node number is defined only when this feature is needed. When this feature is used, the output is from Q1 through an inverter/buffer. *The I/O pin becomes a output-only pin. It cannot be used as an input or as an input/output.*

ABEL™ and Atmel-ABEL™

```
OUTA pin 5;
EXPAND node 70;
OUTA.D = INA&INB# !INC&!IND;
EXPAND = INA & !INC # IND;
```

CUPL™

```
pin 5 = OUTA;
pinnode 208 = EXPAND;
OUTA.D = INA&INB#!INC&!IND;
EXPAND = INA & !INC #
IND;
```

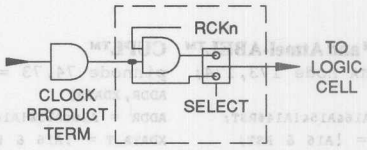
(OUTA and EXPAND are in the same I/O Logic Cell. OUTA is the Q1 output to pin after the inverter/buffer and EXPAND is the combinatorial sum term feedback. The feedbacks from this Logic Cell are Q1 before the inverter/buffer, Q2, and the B sum term)

Clocking Options

There are different methods of clocking the registers in the ATV5000. The clock options can best described as either the AND function of (Quadrant Clock & Clock Product Term) or purely the function of the Clock Product Term (like ATV750 and ATV2500).

Synchronous Operation

The quadrant clock is the only clocking element in this mode of operation. The clock product term must be defined to be equal to 1. In ABEL AHDL, .CK defines the clock product term and .CE is the corresponding quadrant clock.



In CUPL, .CE has a different implication. The keyword .CE means the user wants the AND function (Quadrant Clock & Clock Product Term) for the clock.

ABEL™ and Atmel-ABEL™

```
OUTA.CK = 1;
OUTA.CE = CLOCK; "CLOCK is pin 2
```

CUPL™

```
OUTA.CE = 'B'1;
```

Gated Synchronous Operation

This clock option still uses the fast quadrant register clock pin, but now it has a gating element. The clock product term enables or disables the clock going to the register.

ABEL™ and Atmel-ABEL™

```
OUTA.CK = INX & INY & !INZ;
OUTA.CE = CLOCK; "CLOCK is pin 2
```

CUPL™

```
OUTA.CE = INX&INY&!INZ;
```

Asynchronous Operation

The quadrant clock has no effect on the register in this mode of clock option. The register is clocked by the clock product term like the ATV750 and ATV2500 registers.

ABEL™ and Atmel-ABEL™

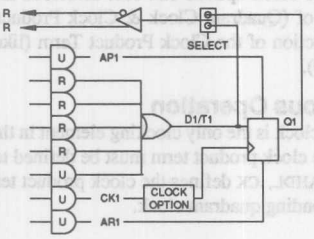
```
OUTA.CK = INA & !INB & INC;
```

CUPL™

```
OUTA.CK = INA & !INB &
INC;
```

Buried Logic Cells

There are six Buried Logic Cells in each quadrant. Every Buried Logic Cell can be configured as a buried register or as a combinatorial feedback to the quadrant array. In the buried register mode, it's used the same way as Q1 and Q2. In the combinatorial feedback mode, it's used the same way as the B sum term feedback.



ABEL™ and Atmel-ABEL™	CUPL™
`ADDR,XDATA node 173,174;`	`pinnode 74,73 = ADDR,XDATA;`
`ADDR = A16&A15&!A14#RST;`	`ADDR = A16&A15&!A14#RST;`
`XDATA.T = !A16 & RST;`	`XDATA.T = !A16 & RST;`
`XDATA.CK = INA & INC;`	`XDATA.CK = INA & INC;`
`XDATA.AR = INB;`	`XDATA.AR = INB;`

D-Type and T-Type Registers

All the registers in the ATV5000 can be configured as D- or T-type. The ISTYPE statement after the PIN or NODE definition in ABEL AHDL tells ABEL which type of register is needed.

ABEL™ and Atmel-ABEL™	CUPL™
`ABC node 123 istype 'reg_t';`	`pinnode 103 = ABC;`
`XYZ pin 7 istype 'reg_d';`	`pin 7 = XYZ;`
`ABC.T = INA & INB # INC;`	`ABC.T = INA & INB # INC;`
`XYZ.D = !INA # INC;`	`XYZ.D = !INA # INC;`

In both languages, the .T extension is reserved for T flip-flop and .D extension for D flip-flop.

Asynchronous Preset

One of the advantanges of having a programmable output polarity I/O is that the same combinatorial output often take fewer product terms to implement using negative logic rather than positive logic or vice versa.

The same can be done for a registered output provided the power-up state is not crucial (all flip-flops are reset upon power up). With an Asynchronous Preset and an Asynchronous Reset, simply swap the two product terms and invert your equation and polaritywill let you take advantage of expressing the same logic in a different polarity. The following example shows a 4-to-1 reduction in product term requirement.

ABEL™ and Atmel-ABEL™	CUPL™
`OUTC pin 8 istype 'invert,reg_d';`	`pin 8 = OUTC;`
`OUTD pin 9 istype 'buffer,reg_d';`	`pin 9 = !OUTD;`
`OUTC.D = INA# !INB#INC# !IND;`	`OUTC.D = INA#!INB#INC#!IND;`
`OUTC.CK = CLK;`	`OUTC.CK = CLK;`
`OUTC.AR = !INA & RST;`	`OUTC.AR = !INA & RST;`
`OUTC.AP = INB & PRESET;`	`OUTC.AP = INB & PRESET;`
`OUTD.D = !INA&INB&!INC&IND;`	`OUTD.D = !INA&INB&!INC&IND;`
`OUTD.CK = CLK;`	`OUTD.CK = CLK;`
`OUTD.AR = INB & PRESET;`	`OUTD.AR = INB & PRESET;`
`OUTD.AP = !INA & RST;`	`OUTD.AP = !INA & RST;`

ABEL™and CUPL™ may be trademarks of others.

Example ABEL™ Description File

```
module V5000;
title    'Demo ATV5000 features with ATMEL-ABEL (IBM386 or compatible)
      ATMEL Corporation EPLD   Joe Yu                April 28, 1991'
V5K device 'P5000';
"   The IOs, registers, latches, inputs, and combinatorial sum terms
"   feedbacks are named with the following prefixes for clarity:
"   Prefix
"   I      -   Quadrant Clocks, Latch Enables.
"   IO     -   IO pins
"   IL     -   Input Latches
"   BLC  - Buried Logic Cells
"   STF    -   Sum Term Feedbacks
"   Valid ABEL AHDL identifiers can be used in place of them.
declarations
I1 pin 1;      " Quadrant 1   Latch Enable/Input
I2 pin 2;      " Quadrant 1   Synchronous Register Clock/Input
I32 pin 32;     " Quadrant 2  Synchronous Register Clock/Input
I34 pin 34;     " Quadrant 2  Latch Enable/Input
I35 pin 35;     " Quadrant 3  Latch Enable/Input
I36 pin 36;     " Quadrant 3  Synchronous Register Clock/Input
I66 pin 66;     " Quadrant 4  Synchronous Register Clock/Input
I68 pin 68;     " Quadrant 4  Latch Enable/Input
"    **** Quadrant I ****
" I/O LOGIC CELL
" ===============
IO4,IO5,IO6,IO7,IO8,IO9                          pin 4,5,6,7,8,9 istype 'buffer,reg_d';
STF4,STF5,STF6,STF7,STF8,STF9                    node 69,70,71,72,73,74;
IO4Q1,IO5Q1,IO6Q1,IO7Q1,IO8Q1,IO9Q1              node 761,762,763,764,765,766;
IO4Q2,IO5Q2,IO6Q2,IO7Q2,IO8Q2,IO9Q2              node 121,122,123,124,125,126;
IO10,IO11,IO12,IO13,IO14,IO15,IO17               pin 10,11,12,13,14,15,17 istype
                                                  'buffer,reg_d'
STF10,STF11,STF12,STF13,STF14,STF15,STF17        node 75,76,77,78,79,80,81;
IO10Q1,IO11Q1,IO12Q1,IO13Q1,IO14Q1,IO15Q1,IO17Q1 node 767,768,769,770,771,772,773;
IO10Q2,IO11Q2,IO12Q2,IO13Q2,IO14Q2,IO15Q2,IO17Q2 node 127,128,129,130,131,132,133;
" INPUT LATCHES
" ===============
IL4,IL5,IL6,IL7,IL8,IL9                          node 813,814,815,816,817,818;
IL10,IL11,IL12,IL13,IL14,IL15,IL17               node 819,820,821,822,823,824,825;
" BURIED LOGIC CELL
" =================
BLC18,BLC19,BLC20,BLC21,BLC22,BLC23              node 178,177,176,175,174,173 ;
declarations "   **** Quadrant II ****
" I/O LOGIC CELL
" ===============
IO18,IO19,IO21,IO22,IO23,IO24                    pin 18,19,21,22,23,24 istype
                                                  'buffer,reg_d';
STF18,STF19,STF21,STF22,STF23,STF24              node 82,83,84,85,86,87;
IO18Q1,IO19Q1,IO21Q1,IO22Q1,IO23Q1,IO24Q1        node 774,775,776,777,778,779;
IO18Q2,IO19Q2,IO21Q2,IO22Q2,IO23Q2,IO24Q2        node 134,135,136,137,138,139;
IO25,IO26,IO27,IO28,IO29,IO30,IO31               pin 25,26,27,28,29,30,31 ISTYPE 'BUFFER'
STF25,STF26,STF27,STF28,STF29,STF30,STF31        node 88,89,90,91,92,93,94;
IO25Q1,IO26Q1,IO27Q1,IO28Q1,IO29Q1,IO30Q1,IO31Q1 node 780,781,782,783,784,785,786 ;
IO25Q2,IO26Q2,IO27Q2,IO28Q2,IO29Q2,IO30Q2,IO31Q2 node 140,141,142,143,144,145,146 ;
" INPUT LATCHES
" ===============
IL18,IL19,IL21,IL22,IL23,IL24                    node 826,827,828,829,830,831;
IL25,IL26,IL27,IL28,IL29,IL30,IL31               node 832,833,834,835,836,837,838;
" BURIED LOGIC CELL
" =================
BLC12,BLC13,BLC14,BLC15,BLC16,BLC17              node 184,183,182,181,180,179;
```

```
" I/O LOGIC CELL
" ==============
IO38,IO39,IO40,IO41,IO42,IO43                    pin 38,39,40,41,42,43;
STF38,STF39,STF40,STF41,STF42,STF43              node 95,96,97,98,99,100;
IO38Q1,IO39Q1,IO40Q1,IO41Q1,IO42Q1,IO43Q1        node 787,788,789,790,791,792;
IO38Q2,IO39Q2,IO40Q2,IO41Q2,IO42Q2,IO43Q2        node 147,148,149,150,151,152
                                                  istype'reg_t';
IO44,IO45,IO46,IO47,IO48,IO49,IO51               pin 44,45,46,47,48,49,51;
STF44,STF45,STF46,STF47,STF48,STF49,STF51        node 101,102,103,104,105,106,107;
IO44Q1,IO45Q1,IO46Q1,IO47Q1,IO48Q1,IO49Q1,IO51Q1 node 793,794,795,796,797,798,799;
IO44Q2,IO45Q2,IO46Q2,IO47Q2,IO48Q2,IO49Q2,IO51Q2 node 153,154,155,156,157,158,159;
" INPUT LATCHES
" ===============
IL38,IL39,IL40,IL41,IL42,IL43                    node 839,840,841,842,843,844;
IL44,IL45,IL46,IL47,IL48,IL49,IL51               node 845,846,847,848,849,850,851;
" BURIED LOGIC CELL
" ==================
BLC6,BLC7,BLC8,BLC9,BLC10,BLC11                  node 190,189,188,187,186,185
                                                  ISTYPE 'REG_D';

declarations "    **** Quadrant IV ****
" I/O LOGIC CELL
" ==============
IO52,IO53,IO55,IO56,IO57,IO58                    pin 52,53,55,56,57,58 istype 'buffer';
STF52,STF53,STF55,STF56,STF57,STF58              node 108,109,110,111,112,113;
IO52Q1,IO53Q1,IO55Q1,IO56Q1,IO57Q1,IO58Q1        node 800,801,802,803,804,805;
IO52Q2,IO53Q2,IO55Q2,IO56Q2,IO57Q2,IO58Q2        node 160,161,162,163,164,165;
IO59,IO60,IO61,IO62,IO63,IO64,IO65               pin 59,60,61,62,63,64,65 istype 'buffer';
STF59,STF60,STF61,STF62,STF63,STF64,STF65        node 114,115,116,117,118,119,120;
IO59Q1,IO60Q1,IO61Q1,IO62Q1,IO63Q1,IO64Q1,IO65Q1 node 806,807,808,809,810,811,812;
IO59Q2,IO60Q2,IO61Q2,IO62Q2,IO63Q2,IO64Q2,IO65Q2 node 166,167,168,169,170,171,172;
" INPUT LATCHES
" ===============
IL52,IL53,IL55,IL56,IL57,IL58                    node 852,853,854,855,856,857;
IL59,IL60,IL61,IL62,IL63,IL64,IL65               node 858,859,860,861,862,863,864;
" BURIED LOGIC CELL
" ==================
BLC0,BLC1,BLC2,BLC3,BLC4,BLC5                    node 196,195,194,193,192,191;
   H,L,C,D,K,U,X,Z = 1,0,.C.,.D.,.K.,.U.,.X.,.Z.;
"    MACRO (INPUT LATCH)
INPUT_LATCH MACRO (IL,IO,QUAD_LE)
{?IL.D  = ?IO;
?IL.LE  = ?QUAD_LE;}
equations
"             INPUT LATCH
"  Each of the 52 I/Os has an input latch. When the quadrant latch enable is high,
"  the pin value is latched.
"  When the quadrant latch clock is low, the latch becomes transparent.
IL4.D   = IO4;   "The .D and the .LE (latch enable) extentions are required to describe a
IL4.LE  = I1;    "latch in ABEL AHDL. The only allowed input to he latch is the IO pin it
                 "associates with. Theonly allowed .LE input is the quadrant latch enable.
                 "They are Pin 1, 34, 35, and 68.
"  INPUT_LATCH macro is another way to describe the latch.
INPUT_LATCH (IL5,IO5,I1); "Latch Pin 5
INPUT_LATCH (IL6,IO6,I1); "Latch Pin 6
IO4.d   = !IO4.fb;  " When .oe is enabled by IO8, IO4 outputs a 1 bit counter.
IO4.oe  = IO8;      " When .oe is disabled by !IO8, IO4 latches a data bit  from the bus.
IO4.ck  = 1;
IO4.ce  = I2;
IO7     = IL4;
test_vectors (   "Test the latches...
[I1,I2,IO8,IO4]-[IO4,IO7])
[ 0,  0,  1,X  ]  ->  [  0,   0 ]; "Transparent
```

```
[ 0, C, 1,X  ]  -> [  1,   1 ]; "Transparent
[ U, 0, 0,0  ]  -> [  Z,   0 ]; "Disable .oe and latch 0
[ 1, C, 1,X  ]  -> [  0,   0 ]; "Latched 0
[ 1, C, 1,X  ]  -> [  1,   0 ]; "Latched 0
[ D, C, 1,X  ]  -> [  0,   0 ]; "Transparent
[ 0, C, 1,X  ]  -> [  1,   1 ]; "Transparent
[ 0, C, 1,X  ]  -> [  0,   0 ]; "Transparent
[ U, 0, 0,1  ]  -> [  Z,   1 ]; "Disable .oe and latch 1
[ 1, 0, 1,X  ]  -> [  0,   1 ]; "Latched 1
[ 1, C, 1,X  ]  -> [  1,   1 ]; "Latched 1
[ 1, C, 1,X  ]  -> [  0,   1 ]; "Latched 1
equations
"   CLOCKING OPTIONS
"  There are different methods of clocking the registers in the ATV5000. The clock is
"  best described as either the AND function of (Quadrant Clock & Clock Product term)
"  or the product term by it self. In the following examples the register can be a
"  name from a pin, Q1, Q2, or Buried Logic Cell. The register can be either .t or
"  .d flip-flop.
IO22.d  = !IO22.fb;
IO22.ck = IO18 & !IO19;     "Note there is no .ce equation defined. This is an
IO22.ar = IO21;             "asynchronous clocking method where the quadrant clock
                            "has no effect.
test_vectors (
[IO18,IO19,IO21  ]  -> [ IO22 ])
[  0,   0,1      ]  -> [   0 ];
[  0,   0,0      ]  -> [   0 ];
[  C,   0,0      ]  -> [   1 ];
[  C,   0,0      ]  -> [   0 ];
equations
IO23.d  = !IO23.fb;
IO23.ck = IO18 & !IO19;     "The clock product term (.ck) is used to gate the quadrant
IO23.ce = I32;              "clock pin. Using quadrant clock pin in a synchronous mode
IO23.ar = IO21;             "allows higher clock rate. Pin 32 is the Quadrant 2 clock pin.
test_vectors (
[I32,IO18,IO19,IO21 ]  ->  [ IO23])
[  0,  1,0,  1   ]  ->  [ 0];
[  C,  0,0,  0   ]  ->  [ 0]; "Product term blocks quadrant clock
[  C,  1,0,  0   ]  ->  [ 1]; "Product term enables quadrant clock
[  C,  1,0,  0   ]  ->  [ 0];
equations
IO24.d  = !IO24.fb;
IO24.ck = 1;        "Note that the .ck is defined to 1. The quadrant clock is the only
IO24.ce = I32;      "clocking element. The .ce is Pin 32 because it's the proper quadrant
IO24.ar = IO21;     "clock to use for synchronous operation.
test_vectors (
[ I32, IO21  ]  -> [ IO24  ])
[  0,  1     ]  -> [  0    ];
[  C,  0     ]  -> [  1    ];
[  C,  0     ]  -> [  0    ];
[  C,  0     ]  -> [  1    ];
"  D-TYPE and T-TYPE REGISTERS
"  All the registers in the ATV5000 can be configured as D or T type. The ISTYPE
"  statement after the PIN or NODE definition tells ABEL which type of register is
"  needed.
"  ABC  node  122 istype 'reg_t';
"  XYZ  pin   5 istype 'reg_d';
"  Use the .t extension for ABC and .d extension for XYZ when you write the equations.
equations
" 3 Bit Synchronous Counter using T flip-flops
IO38Q2.t = 1;                IO38Q2.ck = 1;      IO38Q2.ce = I36;      IO38Q2.ar = IO38;
IO39Q2.t = IO38Q2;           IO39Q2.ck = 1;      IO39Q2.ce = I36;      IO39Q2.ar = IO38;
IO40Q2.t = IO38Q2 & IO39Q2;  IO40Q2.ck = 1;      IO40Q2.ce = I36;      IO40Q2.ar = IO38;
```

```
test_vectors (
[ I36, IO38   ]   -> [ IO40Q2,IO39Q2,IO38Q2])
[   0,   1    ]   -> [ 0,  0,  0 ];
[   C,   0    ]   -> [ 0,  0,  1 ];
[   C,   0    ]   -> [ 0,  1,  0 ];
[   C,   0    ]   -> [ 0,  1,  1 ];
[   C,   0    ]   -> [ 1,  0,  0 ];
[   C,   0    ]   -> [ 1,  0,  1 ];
[   C,   0    ]   -> [ 1,  1,  0 ];
[   C,   0    ]   -> [ 1,  1,  1 ];
[   C,   0    ]   -> [ 0,  0,  0 ];
equations
" 3 Bit Synchronous Counter using D flip-flops
BLC6.d = !BLC6;                BLC6.ck = 1;          BLC6.ce = I36;          BLC6.ar = IO38;
BLC7.d = BLC6 $ BLC7;          BLC7.ck = 1;          BLC7.ce = I36;          BLC7.ar = IO38;
BLC8.d = BLC8 $ (BLC6 & BLC7); BLC8.ck = 1;          BLC8.ce = I36;          BLC8.ar = IO38;
test_vectors (
[ I36, IO38   ]   -> [BLC8,BLC7,BLC6])
[   0,   1 ]   -> [   0,  0,   0 ];
[   C,   0 ]   -> [   0,  0,   1 ];
[   C,   0 ]   -> [   0,  1,   0 ];
[   C,   0 ]   -> [   0,  1,   1 ];
[   C,   0 ]   -> [   1,  0,   0 ];
[   C,   0 ]   -> [   1,  0,   1 ];
[   C,   0 ]   -> [   1,  1,   0 ];
[   C,   0 ]   -> [   1,  1,   1 ];
[   C,   0 ]   -> [   0,  0,   0 ];
"         UNIVERSAL AND REGIONAL PRODUCT TERMS
"   A Regional product term has inputs from all the feedbacks of its quadrant Buried
"   Logic Cells, Q1's, Q2's, and the dedicated Inputs. In addition, a Universal
"   product term has the Pin/B Sum Term Feedbacks.
"         OUTPUTS and FEEDBACKS
"   Combinatorial:
"   Use IO pin name to define the equation. The sum terms may combine to allow 5, 9,
"   or 13 product terms depending on the need of the reduced equation. If the reduced
"   equation requires 5 or less product terms, it leaves Q1 and Q2 each with 4 product
"   terms to use.
"   IO52              =   up to 5 PRODUCT TERMS (2 UNIVERSAL)
"   IO52.oe           =   1 PRODUCT TERM (1 UNIVERSAL)
"   IO52Q1.(d or t)   =   up to 4 PRODUCT TERMS (1 UNIVERSAL)
"   IO52Q1.ck         =   1 PRODUCT TERM (1 UNIVERSAL)
"   IO52Q1.ce         =   QUADRANT CLOCK
"   IO52Q1.ar         =   1 PRODUCT TERM (1 UNIVERSAL)
"   IO52Q1.ap         =   1 PRODUCT TERM (1 UNIVERSAL)
"   IO52Q2.(d or t)   =   up to 4 PRODUCT TERMS (1 UNIVERSAL)
"   IO52Q2.ck         =   1 PRODUCT TERM (1 UNIVERSAL)
"   IO52Q2.ce         =   QUADRANT CLOCK
"   IO52Q2.ar         =   1 PRODUCT TERM (1 UNIVERSAL)
"   IO52Q2.ap         =   1 PRODUCT TERM (0 UNIVERSAL)
"   ALLOWED FEEDBACKS:        SOURCE:
"   IO52                --    Pin feedback, after the buffer/inverter.
"   IO52Q1,IO52Q1.FB    --    Q1 register feedback.
"   IO52Q2,IO52Q2.FB    --    Q2 register feedback.
"   Combinatorial:
"   If the reduced equation requires 6 to 9 product terms, it leaves Q2 with 4 product
"   terms to use. Q1 will  feedback the A Sum Term portion of the output logic.
"   IO52              =   up to 9 PRODUCT TERMS (3 UNIVERSAL)
"   IO52.oe           =   1 PRODUCT TERM (1 UNIVERSAL)
"   IO52Q2.(d or t)   =   up to 4 PRODUCT TERMS (1 UNIVERSAL)
"   IO52Q2.ck         =   1 PRODUCT TERM (1 UNIVERSAL)
"   IO52Q2.ce         =   QUADRANT CLOCK
"   IO52Q2.ar         =   1 PRODUCT TERM (1 UNIVERSAL)
"   IO52Q2.ap         =   1 PRODUCT TERM (0 UNIVERSAL)
```

```
"  ALLOWED FEEDBACKS:                                SOURCE:
"  IO52,IO52.PIN              --                     Pin feedback, after the buffer/inverter.
"  IO52Q2,IO52Q2.FB,IO52Q2.Q  --                     Q2 register feedback.
"  Combinatorial:
"  If the reduced equation requires more than 9 product terms, it leaves no product
"  terms for Q1 and Q2. Q1 feeds back A Sum Term and Q2 feeds back C Sum Term
"  IO52             =   up to 13 PRODUCT TERMS (4 UNIVERSAL)
"  IO52.oe          =   1 PRODUCT TERM (1 UNIVERSAL)
"  ALLOWED FEEDBACKS:       SOURCE:
"  IO52                --   Pin feedback, after the buffer/inverter.
"  Registered:
"  Use IO pin name to define the equation. The sum terms may combine to allow 4, 9,
"  or 13 product terms depending on the need of the reduced equation. If the reduced
"  equation requires 4 or less product terms, you may define a 5 product term
"  equation for the STF (Sum Term Feedback) and define a 4 product term equation for
"  Q2.
"  IO52.(d or t)    =   up to 4 PRODUCT TERMS (1 UNIVERSAL)
"  IO52.oe          =   1 PRODUCT TERM (1 UNIVERSAL)
"  IO52.ck          =   1 PRODUCT TERM (1 UNIVERSAL)
"  IO52.ce          =   QUADRANT CLOCK
"  IO52.ar          =   1 PRODUCT TERM (1 UNIVERSAL)
"  IO52.ap          =   1 PRODUCT TERM (1 UNIVERSAL)
"  STF52            =   up to 5 PRODUCT TERMS (2 UNIVERSAL)
"  IO52Q2.(d or t)  =   up to 4 PRODUCT TERMS (1 UNIVERSAL)
"  IO52Q2.ck        =   1 PRODUCT TERM (1 UNIVERSAL)
"  IO52Q2.ce        =   QUADRANT CLOCK
"  IO52Q2.ar        =   1 PRODUCT TERM (1 UNIVERSAL)
"  IO52Q2.ap        =   1 PRODUCT TERM (0 UNIVERSAL)

"  ALLOWED FEEDBACKS:            SOURCE:
"  IO52.FB                  --   Register feedback prior to buffer/inverter.
"  IO52Q2,IO52Q2.FB         --   Q2 register feedback.
"  STF52                    --   Sum Term Feedback for logic expansion.
"  Registered:
"  If the reduced equation requires 9 to 5 product terms, you may write a 4 product
"  term equation for Q2.
"  IO52.(d or t)    =   up to 9 PRODUCT TERMS (3 UNIVERSAL)
"  IO52.oe          =   1 PRODUCT TERM (1 UNIVERSAL)
"  IO52.ck          =   1 PRODUCT TERM (1 UNIVERSAL)
"  IO52.ce          =   QUADRANT CLOCK
"  IO52.ar          =   1 PRODUCT TERM (1 UNIVERSAL)
"  IO52.ap          =   1 PRODUCT TERM (1 UNIVERSAL)
"  IO52Q2.(d or t)  =   up to 4 PRODUCT TERMS (1 UNIVERSAL)
"  IO52Q2.ck        =   1 PRODUCT TERM (1 UNIVERSAL)
"  IO52Q2.ce        =   QUADRANT CLOCK
"  IO52Q2.ar        =   1 PRODUCT TERM (1 UNIVERSAL)
"  IO52Q2.ap        =   1 PRODUCT TERM (0 UNIVERSAL)
"  ALLOWED FEEDBACKS:          SOURCE:
"  IO52                   --   Pin feedback, after the buffer/inverter.
"  IO52.FB                --   Register feedback prior to buffer/inverter.
"  IO52Q2,IO52Q2.FB,      --   Q2 register feedback.
"  Registered:
"  If the reduced equation requires more than 9 product terms, it leaves zero
"  product terms for Q1 and Q2.
"  IO52.(d or t)    =   up to 13 PRODUCT TERMS (4 UNIVERSAL)
"  IO52.oe          =   1 PRODUCT TERM (1 UNIVERSAL)
"  IO52.ck          =   1 PRODUCT TERM (1 UNIVERSAL)
"  IO52.ce          =   QUADRANT CLOCK
"  IO52.ar          =   1 PRODUCT TERM (1 UNIVERSAL)
"  IO52.ap          =   1 PRODUCT TERM (1 UNIVERSAL)
"  ALLOWED FEEDBACKS:          SOURCE:
"  IO52,                  --   Pin feedback, after the buffer/inverter.
"  IO52.FB                --   Register feedback prior to buffer/inverter.
```

```
"       AP, AR, and CK
"   Each of the 128 registers has its own .AP (Asynchronous Preset), .AR (Asynchronous
"   Reset) and .CK. All ARs and CKs are Universal product terms. The APs are Universal
"   product terms except the APs for Q2.
"   NOTE:  AP and AR should never be active at the same time.
equations
IO10.d     =   !IO10.fb;
IO10.ck    =   IO8;
IO10.ar    =   IO11;
IO10.ap    =   IO12;
test_vectors (
[ IO8, IO11, IO12    ]   ->   [ IO10])
[       0, 1, 0      ]   ->   [  0  ]; "AR
[       0, 0, 0      ]   ->   [  0  ];
[       C, 0, 0      ]   ->   [  1  ];
[       C, 0, 0      ]   ->   [  0  ];
[       0, 0, 1      ]   ->   [  1  ]; "AP
[       0, 1, 0      ]   ->   [  0  ]; "AR
"        BURIED LOGIC CELLS
"   Buried Logic Cell can be configured as a register feedback like Q2. It can also be
"   configured as combinatorial feedback to accommodate for logic expansion.
equations
BLC17.t    =   1; "Registered
BLC17.ck   =   IO9;
BLC17.ar   =   IO21;
BLC14      =   I1; "Combinatiorial
IO25       =   BLC17;
IO26       =   BLC14;
test_vectors (
[IO9, IO21, I1    ]   -> [ BLC17,BLC14,IO25,IO26])
[   0, 1, 0       ]   -> [ 0, 0, 0, 0 ];
[   C, 0, 0       ]   -> [ 1, 0, 1, 0 ];
[   0, 0, 1       ]   -> [ 1, 1, 1, 1 ];
[   C, 0, 1       ]   -> [ 0, 1, 0, 1 ];
[   C, 0, 0       ]   -> [ 1, 0, 1, 0 ];
END;
```

Example CUPL™ Description File

```
Name      V5K;
Partno    NA;
Date      7/22/91;
Revision  01;
Designer  Joe Yu;
Company ATMEL Corporation;
Assembly  NA;
Location  U1;
Device    V5000;
Format    j;
/* Compiled with CUPL 386 version */
/* The IOs, registers, inputs, and combinatorial sum terms feedbacks are named with
 * the following prefixes for clarity:
 * Prefix
 * I      -  Quadrant Clocks, Latch Enables.
 * IO     -  IO pins
 * BLC    -  Buried Logic Cells
 * STF    -  Sum Term Feedbacks
 * Valid CUPL HDL identifiers can be used in place of them. */
pin 1   =     I1;    /* Quadrant 1                  Latch Enable/Input                */
pin 2   =     I2;    /* Quadrant 1                  Synchronous Register Clock/Input */
pin 32  =     I32;   /* Quadrant 2                  Synchronous Register Clock/Input */
pin 34  =     I34;   /* Quadrant 2                  Latch Enable/Input               */
pin 35  =     I35;   /* Quadrant 3                  Latch Enable/Input               */
pin 36  =     I36;   /* Quadrant 3                  Synchronous Register Clock/Input */
pin 66  =     I66;   /* Quadrant 4                  Synchronous Register Clock/Input */
pin 68  =     I68;   /* Quadrant 4                  Latch Enable/Input               */
        /**** Quadrant I ****/
/*  I/O LOGIC CELL  */
/*  ==============  */
pin     [4..9]          =    [IO4..9];
pinnode [209..204]      =    [STF4..9];
pinnode [157..152]      =    [IO4Q1,IO5Q1,IO6Q1,IO7Q1,IO8Q1,IO9Q1];
pinnode [105..100]      =    [IO4Q2,IO5Q2,IO6Q2,IO7Q2,IO8Q2,IO9Q2];
pin     [10..15,17]     =    [IO10..15,IO17];
pinnode [203..197]      =    [STF10..15,STF17];
pinnode [151..145]      =    [IO10Q1,IO11Q1,IO12Q1,IO13Q1,IO14Q1,IO15Q1,IO17Q1];
pinnode [99..93]        =    [IO10Q2,IO11Q2,IO12Q2,IO13Q2,IO14Q2,IO15Q2,IO17Q2];
/* BURIED LOGIC CELL    */
/* ==================   */
pinnode   [69..74]      =    [BLC18..23];
        /**** Quadrant II ****/
/* I/O LOGIC CELL   */
/* ==============   */
pin     [18,19,21..24]  =    [IO18,IO19,IO21..24];
pinnode [210..215]      =    [STF18,STF19,STF21..24];
pinnode [158..163]      =    [IO18Q1,IO19Q1,IO21Q1,IO22Q1,IO23Q1,IO24Q1];
pinnode [106..111]      =    [IO18Q2,IO19Q2,IO21Q2,IO22Q2,IO23Q2,IO24Q2];
pin     [25..31]        =    [IO25..31];
pinnode [216..222]      =    [STF25..31];
pinnode [164..170]      =    [IO25Q1,IO26Q1,IO27Q1,IO28Q1,IO29Q1,IO30Q1,IO31Q1];
pinnode [112..118]      =    [IO25Q2,IO26Q2,IO27Q2,IO28Q2,IO29Q2,IO30Q2,IO31Q2];
/* BURIED LOGIC CELL    */
/* ==================   */
pinnode [80..75]        =    [BLC12..17];
         /**** Quadrant III ****/
/* I/O LOGIC CELL   */
/* ==============   */
pin     [38..43]        =    [IO38..43];
pinnode [235..230]      =    [STF38..43];
```

```
pinnode [183..178]      =    [IO38Q1,IO39Q1,IO40Q1,IO41Q1,IO42Q1,IO43Q1];
pinnode [131..126]      =    [IO38Q2,IO39Q2,IO40Q2,IO41Q2,IO42Q2,IO43Q2];
pin     [44..49,51]     =    [IO44..49,IO51];
pinnode [229..223]      =    [STF44..49,STF51];
pinnode [177..171]      =    [IO44Q1,IO45Q1,IO46Q1,IO47Q1,IO48Q1,IO49Q1,IO51Q1];
pinnode [125..119]      =    [IO44Q2,IO45Q2,IO46Q2,IO47Q2,IO48Q2,IO49Q2,IO51Q2];
/* BURIED LOGIC CELL    */
/* =================    */
pinnode [81..86]        =    [BLC6..11];
          /**** Quadrant IV ****/
/* I/O LOGIC CELL    */
/* ==============    */
pin     [52,53,55..58]  =    [IO52,IO53,IO55..58];
pinnode [236..241]      =    [STF52,STF53,STF55..58];
pinnode [184..189]      =    [IO52Q1,IO53Q1,IO55Q1,IO56Q1,IO57Q1,IO58Q1];
pinnode [132..137]      =    [IO52Q2,IO53Q2,IO55Q2,IO56Q2,IO57Q2,IO58Q2];
pin     [59..65]        =    [IO59..65];
pinnode [242..248]      =    [STF59..65];
pinnode [190..196]      =    [IO59Q1,IO60Q1,IO61Q1,IO62Q1,IO63Q1,IO64Q1,IO65Q1];
pinnode [138..144]      =    [IO59Q2,IO60Q2,IO61Q2,IO62Q2,IO63Q2,IO64Q2,IO65Q2];
/* BURIED LOGIC CELL    */
/* =================    */
pinnode [92..87]        =    [BLC0..5];
/*        INPUT LATCH
   Each of the 52 I/Os has an input latch. When the quadrant latch enable is high,
   the pin value is latched. When the quadrant latch clock is low, the latch becomes
   transparent.    */
IO4.d   = !IO4;
IO4.oe  = IO8.io;
IO4.ce  = 'B'1;
IO7     = IO4.IOL;  /* When the latched input is needed in the design, i.e.. IO4.IOL, IO4
                       is configured as having a latched input.        */
/*        CLOCKING OPTIONS
   There are different methods of clocking the registers in the ATV5000. The clock is
   best described as either the AND function of (Quadrant Clock & Clock Product term)
   or the product term by it self. In the following examples the register can be a
   name from a pin, Q1, Q2, or Buried Logic Cell. The register can be either  .t or .d
   flip-flop.    */
IO22.d  = !IO22;
IO22.ck = IO18 & !IO19; /* Note there is no .ce equation defined. This is an      */
IO22.ar = IO21;         /* asynchronous clocking method where the quadrant clock  */
                        /* has no effect.                                         */
IO23.d  = !IO23;
IO23.ce = IO18 & !IO19; /* The clock product term is used to gate the quadrant     */
IO23.ar = IO21;         /* clock pin.Using quadrant clock pin in a synchronous    */
IO24.d  = !IO24;        /* mode allows higher clock rate. Pin 32 is the Quadrant  */
                        /* 2 clock pin.                                           */
IO24.d  = !IO24;
IO24.ce = 'B'1;         /* Note that the .ce is defined to 1. The quadrant clock  */
IO24.ar = IO21;         /* is the only clocking element. The clock is Pin 32      */
                        /* because it's the proper quadrant clock to use for      */
                        /* synchronous operation.                                 */
/*        D-TYPE and T-TYPE REGISTERS
   All the registers in the ATV5000 can be configured as D or T type. Use the .d
   extension for D type register and .t extension for T type register.    */
/* 3 Bit Synchronous Counter using T flip-flops */
IO38Q2.t = 'B'1;              IO38Q2.ce = 'B'1;    IO38Q2.ar = IO38;
IO39Q2.t = IO38Q2;            IO39Q2.ce = 'B'1;    IO39Q2.ar = IO38;
IO40Q2.t = IO38Q2 & IO39Q2;   IO40Q2.ce = 'B'1;    IO40Q2.ar = IO38;
/* 3 Bit Synchronous Counter using D flip-flops */
BLC6.d = !BLC6;               BLC6.ce = 'B'1;      BLC6.ar = IO38;
BLC7.d = BLC6 $ BLC7;         BLC7.ce = 'B'1;      BLC7.ar = IO38;
BLC8.d = BLC8 $ (BLC6 & BLC7); BLC8.ce = 'B'1;     BLC8.ar = IO38;
```

```
/*      UNIVERSAL AND REGIONAL PRODUCT TERMS
   A Regional product term has inputs from all the feedbacks of its quadrant Buried
   Logic Cells, Q1's, Q2's, and the dedicated Inputs. In addition, a Universal product
   term has the Pin/B Sum Term Feedbacks.                              */
/*        OUTPUTS and FEEDBACKS
   Combinatorial:
   Use IO pin name to define the equation. The sum terms may combine to allow 5, 9, or
   13 product terms depending on the need of the reduced equation. If the reduced
   equation requires 5 or less product terms, it leaves Q1 and Q2 each with 4 product
   terms to use.
        IO52                = up to 5 PRODUCT TERMS (2 UNIVERSAL)
        IO52.oe             = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52Q1.(d or t)     = up to 4 PRODUCT TERMS (1 UNIVERSAL)
        IO52Q1.(ck or ce)   = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52Q1.ar           = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52Q1.ap           = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52Q2.(d or t)     = up to 4 PRODUCT TERMS (1 UNIVERSAL)
        IO52Q2.(ck or ce)   = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52Q2.ar           = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52Q2.ap           = 1 PRODUCT TERM (0 UNIVERSAL)
   ALLOWED FEEDBACKS:         SOURCE:
   IO52,IO52.IO         --    Pin feedback, after the buffer/inverter.
   IO52Q1               --    Q1 register feedback.
   IO52Q2               --    Q2 register feedback.          */
/* Combinatorial:
   If the reduced equation requires 6 to 9 product terms, it leaves Q2 with 4 product
   terms to use. Q1 will feedback the A Sum Term portion of the output logic.
        IO52                = up to 9 PRODUCT TERMS (3 UNIVERSAL)
        IO52.oe             = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52Q2.(d or t)     = up to 4 PRODUCT TERMS (1 UNIVERSAL)
        IO52Q2.(ck or ce)   = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52Q2.ar           = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52Q2.ap           = 1 PRODUCT TERM (0 UNIVERSAL)
   ALLOWED FEEDBACKS:         SOURCE:
   IO52,IO52.IO         --    Pin feedback, after the buffer/inverter.
   IO52Q2               --    Q2 register feedback.          */
/* Combinatorial:
   If the reduced equation requires more than 9 product terms, it leaves no product
   terms for Q1 and Q2. Q1 feeds back A. Sum Term and Q2 feeds back C Sum Term.
        IO52                = up to 13 PRODUCT TERMS (4 UNIVERSAL)
        IO52.oe             = 1 PRODUCT TERM (1 UNIVERSAL)
   ALLOWED FEEDBACKS:         SOURCE:
   IO52,IO52.IO         --    Pin feedback, after the buffer/inverter.    */
/* Registered:
   Use IO pin name to define the equation. The sum terms may combine to allow 4, 9, or
   13 product terms depending on the  need of the reduced equation. If the reduced
   equation requires 4 or less product terms, you may define a 5 product term equation
   for the STF (Sum Term Feedback) and define a 4 product
   term equation for Q2.
        IO52.(d or t)       = up to 4 PRODUCT TERMS (1 UNIVERSAL)
        IO52.oe             = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52.(ck or ce)     = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52.ar             = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52.ap             = 1 PRODUCT TERM (1 UNIVERSAL)
        STF52  = up to 5 PRODUCT TERMS (2 UNIVERSAL)
        IO52Q2.(d or t)     = up to 4 PRODUCT TERMS (1 UNIVERSAL)
        IO52Q2.(ck or ce)   = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52Q2.ar           = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52Q2.ap           = 1 PRODUCT TERM (0 UNIVERSAL)
   ALLOWED FEEDBACKS:         SOURCE:
   IO52                 --    Register feedback prior to buffer/inverter.
   IO52Q2               --    Q2 register feedback.
   STF52                --    Sum Term Feedback for logic expansion.      */
```

```
/* Registered:
   If the reduced equation requires 9 to 5 product terms, you may write a 4 product
   term equation for Q2.
        IO52.(d or t)        = up to 9 PRODUCT TERMS (3 UNIVERSAL)
        IO52.oe              = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52.(ck or ce)      = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52.ar              = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52.ap              = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52Q2.(d or t)      = up to 4 PRODUCT TERMS (1 UNIVERSAL)
        IO52Q2.(ck or ce)    = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52Q2.ar            = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52Q2.ap            = 1 PRODUCT TERM (0 UNIVERSAL)
   ALLOWED FEEDBACKS:          SOURCE:
   IO52.IO              --     Pin feedback, after the buffer/inverter.
   IO52                 --     Register feedback prior to buffer/inverter.
   IO52Q2               --     Q2 register feedback. */
/* Registered:
   If the reduced equation requires more than 9 product terms, it leaves zero product
   terms for Q1 and Q2.
        IO52.(d or t)        = up to 13 PRODUCT TERMS (4 UNIVERSAL)
        IO52.oe              = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52.(ck or ce)      = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52.ar              = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52.ap              = 1 PRODUCT TERM (1 UNIVERSAL)
   ALLOWED FEEDBACKS:          SOURCE:
   IO52.IO              --     Pin feedback, after the buffer/inverter.
   IO52                 --     Register feedback prior to buffer/inverter.*/
/*        AP, AR, and CK
   Each of the 128 registers has its own .AP (Asynchronous Preset), .AR (Asynchronous
   Reset) and .CK or .CE. All ARs and CKs are Universal product terms. The APs are
   Universal product terms except the APs for Q2.
   NOTE: AP and AR should never be active at the same time.          */
IO10.d    =  !IO10;
IO10.ck   =  IO8;
IO10.ar   =  IO11;
IO10.ap   =  IO12;
/*        BURIED LOGIC CELLS
   Buried Logic Cell can be configured as a register feedback like Q2. It can also be
   configured as combinatorial feedback to accommodate for logic expansion. */
BLC17.t   =  'B'1;  /*Registered */
BLC17.ck  =  IO9;
BLC17.ar  =  IO21;
BLC14     =  I1;/*Combinatiorial */
IO25      =  BLC17;
IO26      =  BLC14;
END;
```

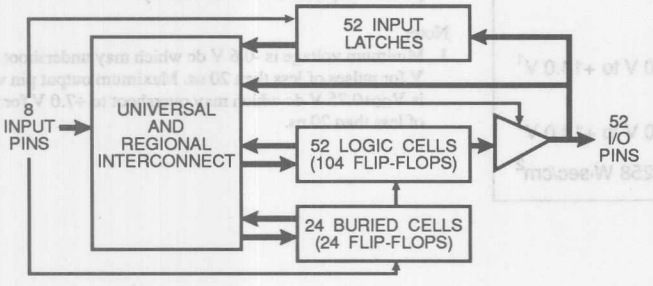
Features

- Advanced Programmable Logic Device - High Gate Utilization
- Pin-Compatible with Atmel's ATV5000
- Flexible Interconnect Architecture - Similar to ATV5000 with More Emphasis on Universal Routing
- Flexible Logic Cells - 128 Flip-Flops and 52 Latches
- Multiple Flip-Flop Types - Synchronous or Asynchronous Registers
- High Speed - 50 MHz Operation
- Complete Third Party Software Support
  - No Placement, Routing or Layout Software Required
- Proven and Reliable High Speed CMOS EPROM Process
  - 2000 V ESD Protection
  - 200 mA Latchup Immunity
- Reprogrammable - Tested 100% for Programmability
- Commercial, Industrial and Military Temperature Grades

High Density UV Erasable Programmable Logic Device

7

Block Diagram



Description

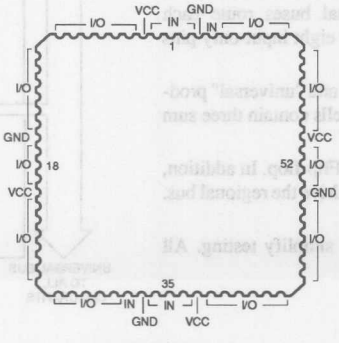
The Atmel V5100 is an easy to use, high density programmable logic device. Its simple, regular architecture translates into increased utilization and high performance. Additional universal routing simplifies design fitting.

The ATV5100 has one programmable combinatorial logic array. This guarantees easy interconnection of and uniform performance from all nodes. "Sum terms", which are easy to use groupings of AND-OR gates, provide combinatorial logic blocks. Sum terms can be wire-OR'd together to integrate larger logic blocks. To expand the levels of logic, buried sum terms

continued on next page

Chip Carrier Pin Configuration

Pin Name	Function
IN	Logic and Clock Inputs
Pins 2,32,36,66	Input/Register Clocks 1-4
Pins 1,34,35,68	Input/Latch Clocks 1-4
I/O	Bidirectional Buffers
VCC	+5 V Supply



Description (Continued)

feed back into the logic array. The 52 I/O pins can each be driven by a register or a sum term. Each I/O pin has an individually enabled input latch.

All 128 registers are configurable as D- or T-types without using extra logic gates. Individual sum terms, asynchronous presets, resets and clocks give each flip-flop added flexibility. A direct "clock from pin" option guarantees synchronization and fast clock to output performance.

Standard, off-the-shelf third party software tools and programmers support the ATV5100. This minimizes start-up investment and improves product support.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V[1]
Voltage on Input Pins with Respect to Ground During Programming	-2.0 V to +14.0 V[1]
Programming Voltage with Respect to Ground	-2.0 V to +14.0 V[1]
Integrated UV Erase Dose	7258 W·sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC}+0.75 V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

Functional Logic Diagram Description

There are 52 identical Input/Ouput logic cells and 24 identical buried logic cells in the ATV5100. Each I/O cell has two flip-flops, up to three sum terms, individual clock, reset, and preset terms per flip-flop, and one output enable term. Independent of output configuration, all flip-flops are always usable, and have at least four Product Term inputs each.

Each I/O pin (52 total) signal or its latched version drives the logic array. There is one latch clock per quadrant.

The ATV5100 has four identical quadrants (see Figure 2). The Universal Bus routes true and false signals from each of the 52 I/O pins to all four quadrants. Regional buses route each quadrant's flip-flop Q and $\overline{Q}$ locally. The eight input-only pins are available in all four regional buses.

Each logic cell has a number of "regional" and "universal" product terms (see Figure 1). The I/O Logic Cells contain three sum terms, two flip-flops, and an I/O buffer.

The Buried Logic Cells each contain one Flip-flop. In addition, in each buried logic cell the sum term can drive the regional bus. This allows for logic expansion.

Serial register preload and observability simplify testing. All registers automatically clear at power up.

Quadrant Functional Logic Diagram ATV5100

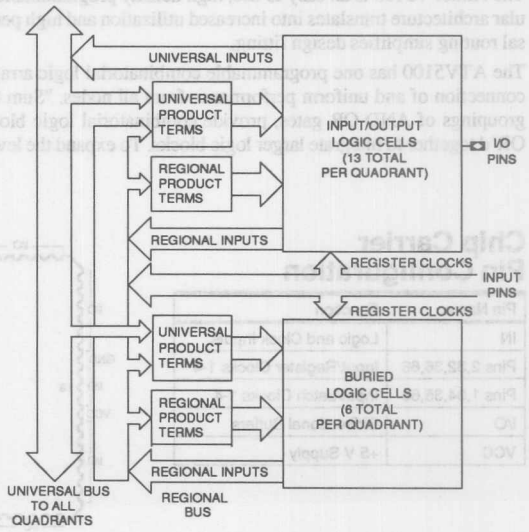


Figure 1

D.C. and A.C. Operating Range

		ATV5100-25	ATV5100/L-30	ATV5100/L-35
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.		-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C
Vcc Power Supply		5 V ± 10%	5 V ± 10%	5 V ± 10%

ATV5100 Block Diagram

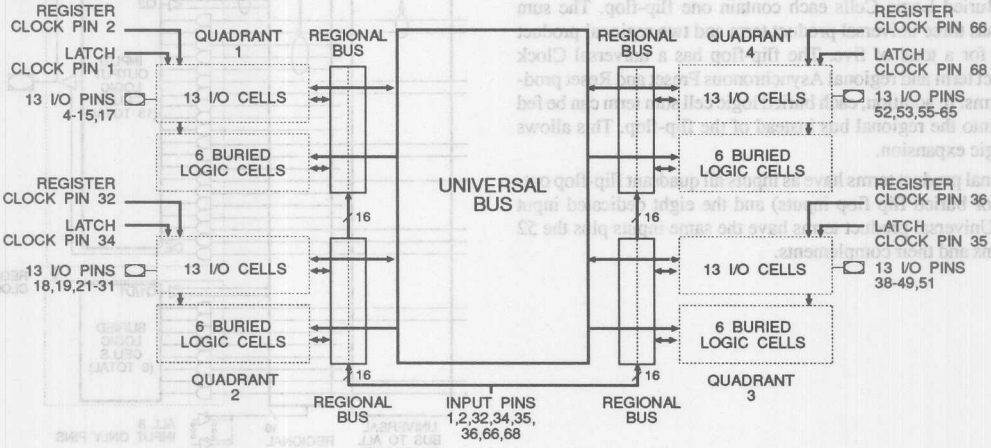


Figure 2

Quadrant Logic Diagram and Description

The ATV5100 has: four identical quadrants, 52 identical input/output logic cells, and 24 identical buried logic cells. The Universal Bus routes true and false signals from each of the 52 I/O pins to all four quadrants. Regional buses route each quadrant's flip-flop Q and $\overline{Q}$ locally. The eight input-only pins are available in every Regional Bus.

Each logic cell has a number of "regional" and "universal" product terms. The I/O Logic Cells contain three sum terms, two flip-flops, and an I/O buffer. Sum term B has five product terms - three universal and two regional. Sum term A has four product terms - two universal and two regional. Sum term C has four product terms - three universal and one regional (see next page). Flip-flops Q1 and Q2 have universal Clock and regional Preset and Reset product terms. There is one regional product term for the I/O pin Output Enable.

The Buried Logic Cells each contain one flip-flop. The sum term has three universal product term and two regional product terms for a total of five. The flip-flop has a universal Clock product term and regional Asynchronous Preset and Reset product terms. In addition, each buried logic cell sum term can be fed back into the regional bus instead of the flip-flop. This allows for logic expansion.

Regional product terms have as inputs all quadrant flip-flop outputs (or buried flip flop inputs) and the eight dedicated input pins. Universal product terms have the same inputs plus the 52 I/O pins and their complements.

Quadrant Clock Pin Assignments

Quadrant Number	Register Clock Pin	Latch Clock Pin
1	2	1
2	32	34
3	36	35
4	66	68

Quadrant Logic Diagram

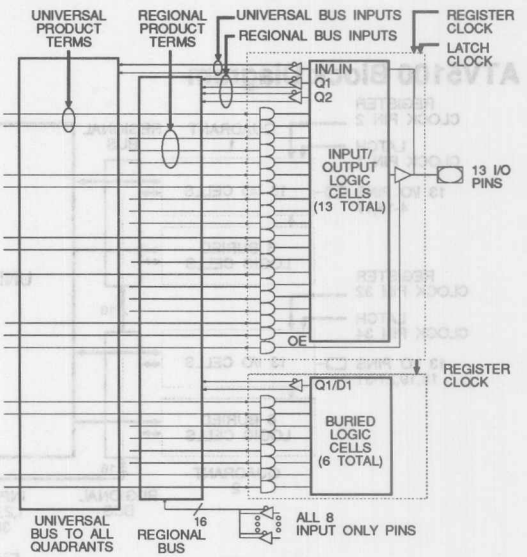


Figure 3

Logic Cell Options

The ATV5100 Logic Cells contain most of the chip's logic options. The standard Logic Cell contains two flip-flops, three sum terms and three array inputs. The three sum terms can be combined to provide sum term options of four, five, nine, or 13 product terms. A combinatorial signal or the output of Q1 can be sent to the I/O cell.

The ATV5100 retains the ATV2500's ability to bury both registers in the I/O cell and still output a combinatorial signal (see Figure 8). A new feature, unique to the ATV5000 and ATV5100, is the ability to output Q1 and feedback the combinatorial term directly (see Figure 7). This high speed logic expansion term increases the devices flexibility and gate utilization.

Buried Logic Cells

Each quadrant has six buried logic cells (see Figure 4). Each cell contains one sum term with five product terms, a flip-flop, and individual preset, clear, and clock terms. A configuration bit selects either the Q output or the D input for feedback into the regional bus.

Buried Logic Cells

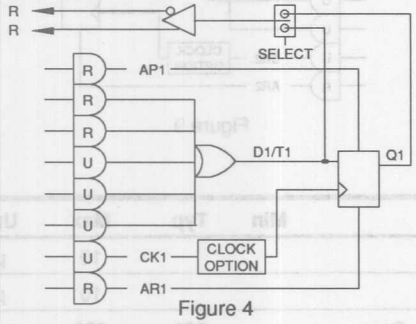


Figure 4

Clock Option

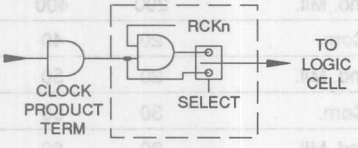


Figure 5

I/O Pin Logic

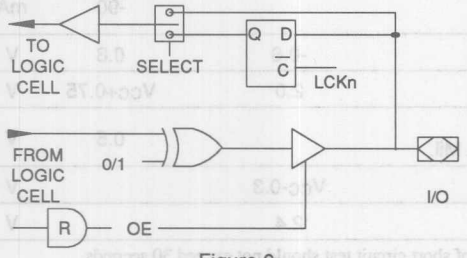


Figure 6

Logic Cell with Buried Sum Term and Register to I/O Cell

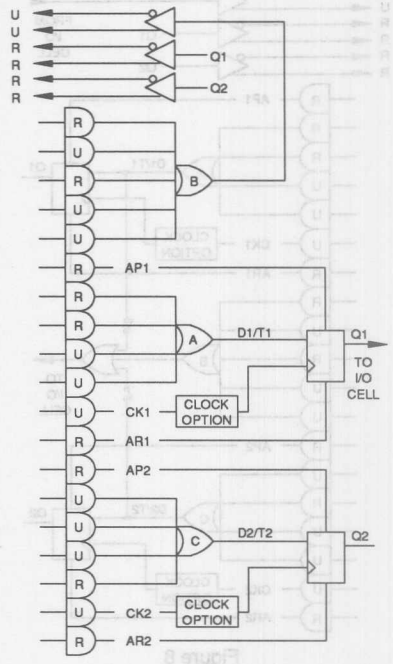


Figure 7

Flip-Flop Clock Options

Each register may be connected to its regional clock to provide fast clock to output timing (see Figure 5). In this "synchronous" mode, the clock is one of four input pins, a unique clock pin for each chip quadrant. One product term defines each flip-flop's clock in the "asynchronous" mode.

In the "synchronous" mode, the regional clock is ANDed with the product term. This provides the fast timing of a synchronous clock with the local control of the product term.

I/O Pin Latches

Each I/O pin of the ATV5100 has an input latch which can be individually enabled or disabled (see Figure 6). Each chip quadrant has a unique latch clock. When the latch is inactive, pin input flows directly into the array. When activated, the latch is flow-through when the clock signal is low, and data is captured on the clock's rising edge.

Flip-Flop Types

Each flip-flop in the ATV5100 may be configured as either a T- or D-type flip-flop. A T-type flip-flop can also easily be configured into a JK or SR flip-flop.

7

Combinatorial to I/O Cell

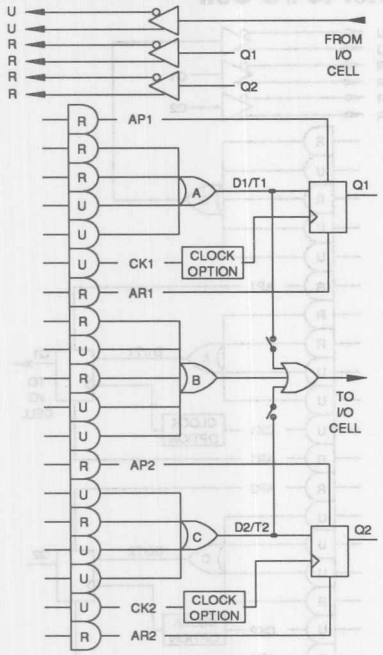


Figure 8

Sum Terms, Register to I/O Cell

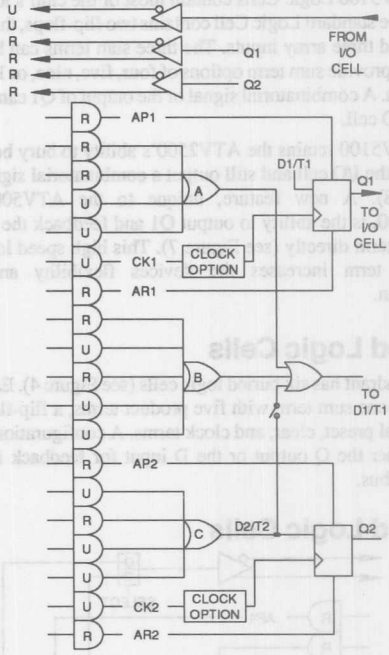


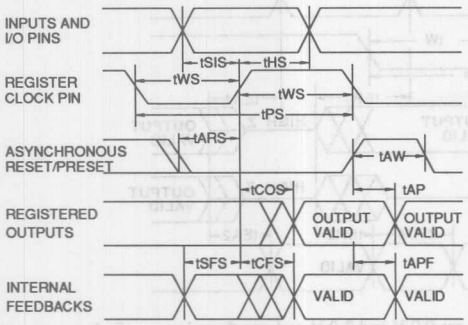
Figure 9

D.C. Characteristics

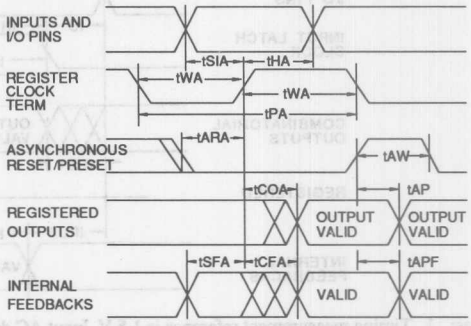
Symbol	Parameter	Condition		Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1 V to V_{CC}+1 V				10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1 V to V_{CC}+0.1 V				10	µA
I_{CC}	Power Supply Current ATV5100	V_{CC} = MAX, V_{IN} = GND or V_{CC} Outputs Open	Com.		200	350	mA
			Ind.,Mil.		200	400	mA
I_{CC}	Power Supply Current ATV5100L	V_{CC} = MAX, V_{IN} = GND or V_{CC} Outputs Open	Com.		20	40	mA
			Ind.,Mil.		20	50	mA
I_{CC2}	Clocked Power Supply Current, ATV5100L Only	f = 1 MHz, V_{CC} = MAX Outputs Open	Com.		30	50	mA
			Ind.,Mil.		30	60	mA
I_{OS} (1)	Output Short Circuit Current	V_{OUT} = 0.5 V				-90	mA
V_{IL}	Input Low Voltage			-0.6		0.8	V
V_{IH}	Input High Voltage			2.0		V_{CC}+0.75	V
V_{OL}	Output Low Voltage	V_{IN} = V_{IH} or V_{IL}, I_{OL} = 8 mA Com,Ind; 6 mA Mil.				0.5	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA		V_{CC}-0.3			V
		I_{OH} = -4.0 mA		2.4			V

Note: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 seconds.

A.C. Waveforms [1] Input Pin Clock



A.C. Waveforms [1] Product Term Clock



Notes: 1. Timing measurement reference is 1.5 V. Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.

Register A.C. Characteristics, Input Pin Clock

Symbol	Parameter	ATV5100-25 Min	ATV5100-25 Max	ATV5100/L-30 Min	ATV5100/L-30 Max	ATV5100/L-35 Min	ATV5100/L-35 Max	Units
t_{COS}	Clock to Output		15		20		25	ns
t_{CFS}	Clock to Feedback	0	9	0	12	0	15	ns
t_{SIS}	Input Setup Time[1]	16		17		20		ns
t_{SFS}	Feedback Setup Time[1]	11		13		15		ns
t_{HS}	Hold Time	0		0		0		ns
t_{WS}	Clock Width	10		12		15		ns
t_{PS}	Clock Period	20		25		30		ns
F_{MAXS}	Maximum Frequency (1/t_{PS})		50		40		33	MHz
t_{ARS}	Asynchronous Reset/Preset Recovery Time	20		25		30		ns

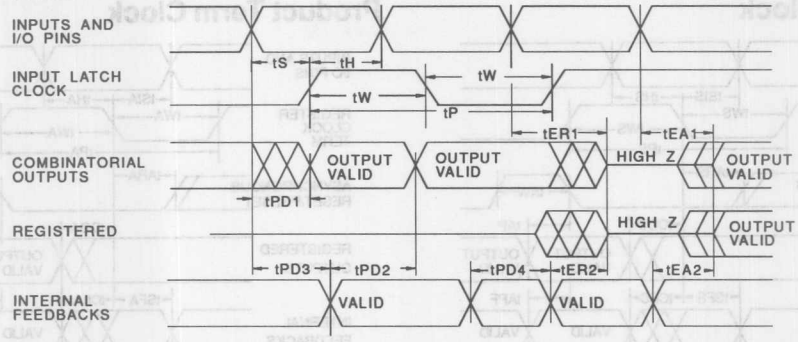
Note: 1. Add 3 ns for Universal Product Terms.

Register A.C. Characteristics, Product Term Clock

Symbol	Parameter	ATV5100-25 Min	ATV5100-25 Max	ATV5100/L-30 Min	ATV5100/L-30 Max	ATV5100/L-35 Min	ATV5100/L-35 Max	Units
t_{COA}	Clock to Output		25		30		35	ns
t_{CFA}	Clock to Feedback	7	20	10	25	12	27	ns
t_{SIA}	Input Setup Time[1]	10		12		15		ns
t_{SFA}	Feedback Setup Time[1]	5		8		13		ns
t_{HA}	Hold Time	8		10		12		ns
t_{WA}	Clock Width	12		15		15		ns
t_{PA}	Clock Period	25		33		40		ns
F_{MAXA}	Maximum Frequency (1/t_{PA})		40		30		25	MHz
t_{ARA}	Asynchronous Reset/Preset Recovery Time	15		20		25		ns

Note: 1. Add 3 ns for Universal Product Terms.

A.C. Waveforms [1]



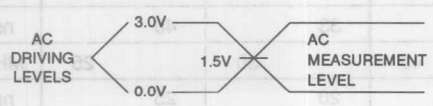
Notes: 1. Timing measurement reference is 1.5 V. Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.

A.C. Characteristics

Symbol	Parameter	ATV5100-25 Min	ATV5100-25 Max	ATV5100/L-30 Min	ATV5100/L-30 Max	ATV5100/L-35 Min	ATV5100/L-35 Max	Units
t_{PD1}	Input to Non-Registered Output[1]		25		30		35	ns
t_{PD2}	Feedback to Non-Registered Output[1]		20		25		30	ns
t_{PD3}	Input to Non-Registered Feedback[1]		20		25		30	ns
t_{PD4}	Feedback to Non-Registered Feedback[1]		15		18		22	ns
t_{EA1}	Input to Output Enable		30		35		40	ns
t_{ER1}	Input to Output Disable		30		35		40	ns
t_{EA2}	Feedback to Output Enable		25		30		35	ns
t_{ER2}	Feedback to Output Disable		25		30		35	ns
t_S	Input Latch Setup Time	5		6		7		ns
t_H	Input Latch Hold Time	5		5		5		ns
t_W	Clock Width	10		12		12		ns
t_P	Clock Period	20		25		30		ns
F_{MAX}	Maximum Frequency (1/t_P)		50		40		33	MHz
t_{AW}	Asynchronous Reset/Preset Width	15		20		20		ns
t_{AP}	Asynchronous Reset/ Preset to Registered Output		30		35		40	ns
t_{APF}	Asynchronous Reset/ Preset to Registered Feedback		25		30		35	ns

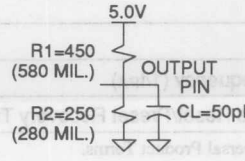
Note: 1. Add 3 ns for Universal Product Terms.

Input Test Waveforms and Measurement Levels



t_R, t_F < 5 ns (10% to 90%)

Output Test Load



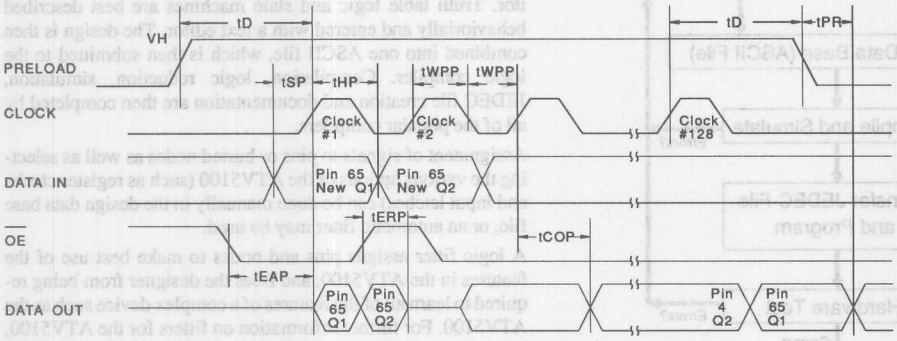
Preload and Observability of Registers

The ATV5100's registers include circuity to load and unload them serially. This feature simplifies testing. Any state can be forced into the registers to control test sequencing, and all registers may be observed, independent of being buried. A V_{IH} level on the Data In pin will force the appropriate register high; a V_{IL} will force it low, independent of the polarity or other configuration bit settings.

The PRELOAD/OBSERVE state is entered by placing an 11 V to 14 V signal on pin 68 on the JLCC. When the clock (pin 1) is pulsed high, data (pin 2) is clocked serially through all registers in the device, as in the following table. All register contents are also clocked out of the device on Pin 65 in FIFO fashion. If observability only is required, data out should be connected back to data in. If preload only is required, OE (pin 66) can be held high and data out (pin 65) will remain high impedance.

Any user contemplating the use of register preload/obervability is encouraged to contact Atmel's EPLD applications department.

Note: All register clock terms or pins must be low prior to entering the Preload/Observe state, and low prior to leaving the



tD_{MIN} = 100 ns
tSP_{MIN} = 50 ns
tHP_{MIN} = 50 ns
$tWPP_{MIN}$ = 100 ns
tPR_{MIN} = 1000 ns
$tERP_{MAX}$ = 100 ns
$tEAP_{MAX}$ = 100 ns
$tCOP_{MAX}$ = 100 ns

7

Preload / Observe Register Scan Order

Quadrant	Pin																			
Quadrant 1	Pin	4			5			6		•••			15			17				
	D_{IN}	→ Q2	→ Q1	→ B23	→ Q2	→ Q1	→ Q2	→ Q1	•••		B18	→ Q2	→ Q1	→ Q2	→ Q1	→ (Quadrant 2)				
Quadrant 2	Pin	18			19			21		22		•••			31					
(Quadrant 1)→		Q2	→ Q1	→ Q2	→ Q1	→ B17	→ Q2	→ Q1	→ Q2	→ Q1	•••		B12	→ Q2	→ Q1	→ (Quadrant 3)				
Quadrant 3	Pin	38			39			40		•••			49			51				
(Quadrant 2)→		Q2	→ Q1	→ B11	→ Q2	→ Q1	→ Q2	→ Q1	•••		B6	→ Q2	→ Q1	→ Q2	→ Q1	→ (Quadrant 4)				
Quadrant 4	Pin	52			53			55		56		•••			65					
(Quadrant 3)→		Q2	→ Q1	→ Q2	→ Q1	→ B5	→ Q2	→ Q1	→ Q2	→ Q1	•••		B0	→ Q2	→ Q1	→ D_{OUT}				

Power Up Reset

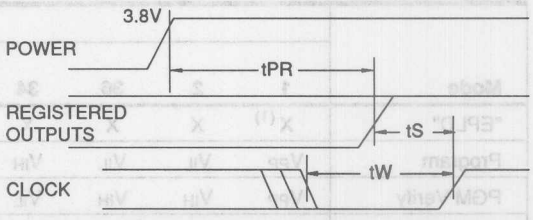
The registers in the ATV5100 are designed to reset during power up. At a point delayed slightly from V_{CC} crossing 3.8 V, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

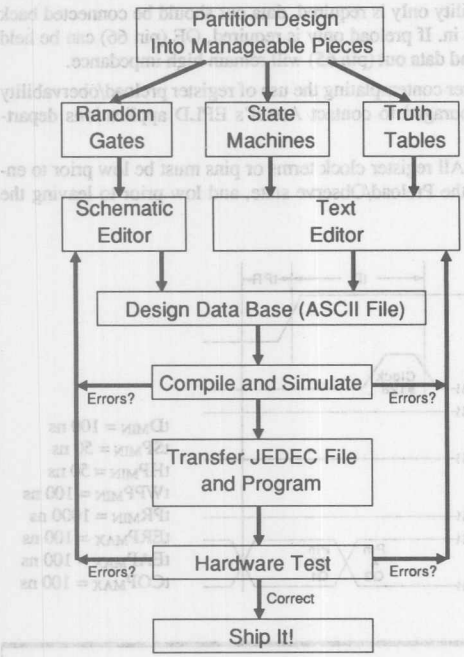
1) The V_{CC} rise must be monotonic,

2) After reset occurs, all input and feedback setup times must be met before driving the clock term high, and

3) The signals from which the clock is derived must remain stable during t_{PR}.



Parameter	Description	Min	Typ	Max	Units
t_{PR}	Power-Up Reset Time		600	1000	ns



The ATV5100's simple, regular architecture means that only simple logic compilers are required to configure the device. No layout or route and place are required. These software tools are readily available from companies such as Data I/O Corporation (ABEL™), Logical Devices (CUPL™), and ISDATA (LOGiC™).

The first step in designing a device as complex as the ATV5100 is to partition your design into manageable blocks. These blocks are then allocated proportionally to each of the four quadrants of the ATV5100. Random gates can be described either with boolean equations (a behavioral description) or with a schematic editor. Truth table logic and state machines are best described behaviorially and entered with a text editor. The design is then combined into one ASCII file, which is then submitted to the logic compiler. Compilation, logic reduction, simulation, JEDEC file creation and documentation are then completed by all of the popular compilers.

Assignment of signals to pins or buried nodes as well as selecting the various options of the ATV5100 (such as register clocks and input latches) can be done manually in the design data base file, or an automatic fitter may be used.

A logic fitter assigns pins and nodes to make best use of the features in the ATV5100, and frees the designer from being required to learn all of the features of a complex device such as the ATV5100. For further information on fitters for the ATV5100, contact Atmel's EPLD applications department.

After correcting any syntax and logic errors discovered by the compiler, the JEDEC file is ready to download to an EPLD programmer. These are available from a number of manufacturers. Programmed devices are usually first tested in the programmer with your supplied test vectors. The next step is check out your "custom chip" in the target system. When this hardware debug step is complete, your system is ready to go— all in a matter of hours.

ABEL™,CUPL™ and LOGiC™ may be trademarks of others.

Operating Modes

	68-Lead LCC								
Mode	1	2	36	34	68	66	V_{CC} (3,20,37,54)	I/O's	I/O Pin 65
"EPLD"	X (1)	X	X	X	X	X	5V	I/O	I/O
Program	V_{PP}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	6V	ADD/D_{IN}	ADD
PGM Verify	V_{PP}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	X	6V	ADD/D_{OUT}	ADD
PGM Inhibit	V_{PP}	V_{IH}	V_{IH}	V_{IH}	V_{IH}	X	6V	High Z	High Z
Preload/Observe	⎍	D_{IN}	X	X	V_H (2)	$\overline{OE}$	5V	High Z	D_{OUT}

Notes: 1. X can be V_{IL} or V_{IH}.

2. V_H = 11.0 V to 14.0 V

ATV5100 PLCC/PGA Pin Assignments

PLCC Pin #	PGA Pin #	Name	PLCC Pin #	PGA Pin #	Name	PLCC Pin #	PGA Pin #	Name	PLCC Pin #	PGA Pin #	Name
1	B6	IN	18	F2	I/O	35	K6	IN	52	F10	I/O
2	A6	IN	19	F1	I/O	36	L6	IN	53	F11	I/O
3	B5	VCC	20	G2	VCC	37	K7	VCC	54	E10	VCC
4	A5	I/O	21	G1	I/O	38	L7	I/O	55	E11	I/O
5	B4	I/O	22	H2	I/O	39	K8	I/O	56	D10	I/O
6	A4	I/O	23	H1	I/O	40	L8	I/O	57	D11	I/O
7	B3	I/O	24	J2	I/O	41	K9	I/O	58	C10	I/O
8	A3	I/O	25	J1	I/O	42	L9	I/O	59	C11	I/O
9	A2	I/O	26	K1	I/O	43	L10	I/O	60	B11	I/O
10	B2	I/O	27	K2	I/O	44	K10	I/O	61	B10	I/O
11	B1	I/O	28	L2	I/O	45	K11	I/O	62	A10	I/O
12	C2	I/O	29	K3	I/O	46	J10	I/O	63	B9	I/O
13	C1	I/O	30	L3	I/O	47	J11	I/O	64	A9	I/O
14	D2	I/O	31	K4	I/O	48	H10	I/O	65	B8	I/O
15	D1	I/O	32	L4	IN	49	H11	I/O	66	A8	IN
16	E2	GND	33	K5	GND	50	G10	GND	67	B7	GND
17	E1	I/O	34	L5	IN	51	G11	I/O	68	A7	IN

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	6	8	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATV5100 fuse patterns. Once programmed, all outputs appear programmed during verify. The security fuse should be programmed last (after verifying all other programmed bits), as its effect is immediate.

The security fuse also inhibits Preload and Observability.

Erasure Characteristics

The entire memory array of an ATV5100 is erased after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 $W \cdot sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPLD which will be subjected to continuous fluorescent indoor lighting or sunlight.

Ordering Information

t_{PD} (ns)	t_{COS} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
25	15	50	ATV5100-25JC ATV5100-25KC ATV5100-25UC	68J 68KW 68UW	Commercial (0°C to 70°C)
30	20	40	ATV5100-30JC ATV5100-30KC ATV5100-30UC	68J 68KW 68UW	Commercial (0°C to 70°C)
			ATV5100-30KI ATV5100-30UI	68KW 68UW	Industrial (-40°C to 85°C)
			ATV5100-30KM ATV5100-30UM	68KW 68UW	Military (-55°C to 125°C)
			ATV5100-30KM/883 ATV5100-30UM/883	68KW 68UW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
35	25	33	ATV5100-35JC ATV5100-35KC ATV5100-35UC	68J 68KW 68UW	Commercial (0°C to 70°C)
			ATV5100-35KI ATV5100-35UI	68KW 68UW	Industrial (-40°C to 85°C)
			ATV5100-35KM ATV5100-35UM	68KW 68UW	Military (-55°C to 125°C)
			ATV5100-35KM/883 ATV5100-35UM/883	68KW 68UW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
68J	68 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
68KW	68 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
68UW	68 Pin, Windowed, Ceramic Pin Grid Array (PGA)

Ordering Information

t_{PD} (ns)	t_{COS} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
30	20	40	ATV5100L-30JC ATV5100L-30KC ATV5100L-30UC	68J 68KW 68UW	Commercial (0°C to 70°C)
35	25	33	ATV5100L-35JC ATV5100L-35KC ATV5100L-35UC	68J 68KW 68UW	Commercial (0°C to 70°C)
			ATV5100L-35KI ATV5100L-35UI	68KW 68UW	Industrial (-40°C to 85°C)
			ATV5100L-35KM ATV5100L-35UM	68KW 68UW	Military (-55°C to 125°C)
			ATV5100L-35KM/883 ATV5100L-35UM/883	68KW 68UW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

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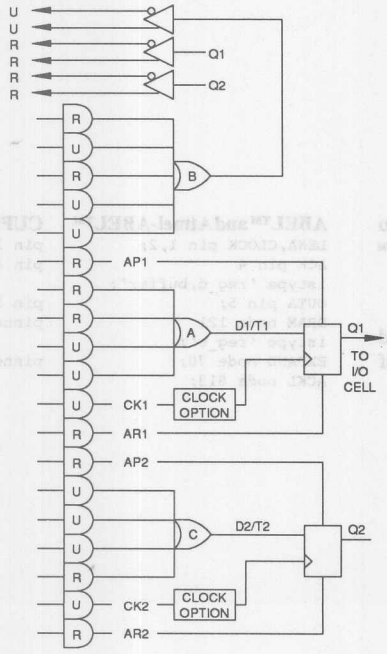
Package Type	
68J	68 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
68KW	68 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
68UW	68 Pin, Windowed, Ceramic Pin Grid Array (PGA)

Using the ATV5100

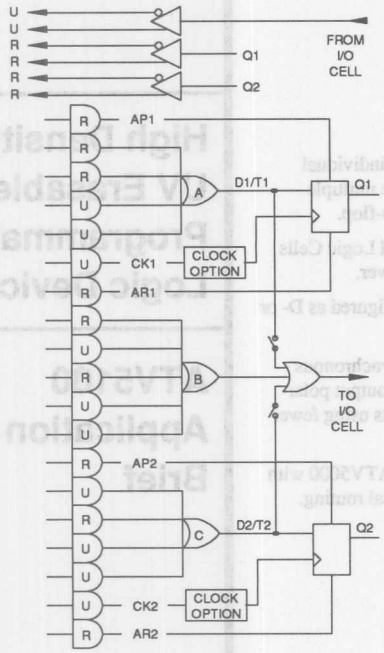
The ATV5100 Logic Cells retain the ATV2500's basic features with two registers, three sum terms and Q1, Q2, and pin feedback options. In addition, these following features make the ATV5100 even more versatile:

1. Input latches are added to every I/O pin. Each latch can be enabled or disabled independently.
2. The ATV5100 can be configured to feedback a combinatorial sum term and send Q1 to the output. Feeding the combinatorial sum term internally makes implementing logic equations with large number of product terms possible without sacrificing an I/O pin.
3. Dedicated clock pins and individual clock product terms create multiple clock options for each flip-flop.
4. The addition of the Buried Logic Cells handles more logic than ever.
5. Each flip-flop can be configured as D- or T-type flip-flop.
6. Asynchronous Preset, Asynchronous Reset and programmable output polarity allow registered outputs using fewer product terms.
7. Same architecture as the ATV5000 with more emphasis on universal routing.

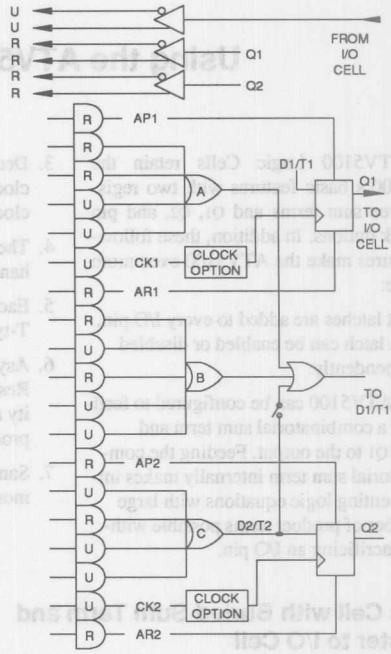
Logic Cell with Buried Sum Term and Register to I/O Cell



Logic Cell, Two Buried Registers, Combinatorial to I/O Cell



Logic Cell with Combinable Sum Terms, Register to I/O Cell



The following are sections of ABEL™ and CUPL™ source files to illustrate how each of these features is described in the ABEL™ and CUPL™ high level description languages.

Pin and Node Assignments

All the buried registers used in the design need to be assigned node numbers. The following tables show the complete set of node numbers by quadrant.

ABEL™ and Atmel-ABEL™

```
LENA,CLOCK pin 1,2;
ACK pin 4
istype 'reg_d,buffer';
OUTA pin 5;
DRAM node 121
istype 'reg_t';
EXPAND node 70;
ACKL node 813;
```

CUPL™

```
pin 1,2 = LENA,CLOCK;
pin 4 = ACK;

pin 5 = OUTA;
pinnode 105 = DRAM;

pinnode 208 = EXPAND;
```

ATV5100 ABEL™ and Atmel-ABEL™ Node Numbers

Quadrant I

Pin	Input Latch	Sum Term A	Sum Term B	Sum Term C
4	813	761	69	121
5	814	762	70	122
6	815	763	71	123
7	816	764	72	124
8	817	765	73	125
9	818	766	74	126
10	819	767	75	127
11	820	768	76	128
12	821	769	77	129
13	822	770	78	130
14	823	771	79	131
15	824	772	80	132
17	825	773	81	133

6 Buried Logic Cells
B23 - B18 node 173 - 178
LCK1 pin 1; Quadrant Latch clock
RCK1 pin 2; Quadrant Synchronous Register Clock

Quadrant II

Pin	Input Latch	Sum Term A	Sum Term B	Sum Term C
18	826	774	82	134
19	827	775	83	135
21	828	776	84	136
22	829	777	85	137
23	830	778	86	138
24	831	779	87	139
25	832	780	88	140
26	833	781	89	141
27	834	782	90	142
28	835	783	91	143
29	836	784	92	144
30	837	785	93	145
31	838	786	94	146

6 Buried Logic Cells
B17 - B12 node 179 - 184
LCK2 pin 34; Quadrant Latch Clock
RCK2 pin 32; Quadrant Synchronous Register Clock

Quadrant III

Pin	Input Latch	Sum Term A	Sum Term B	Sum Term C
38	839	787	95	147
39	840	788	96	148
40	841	789	97	149
41	842	790	98	150
42	843	791	99	151
43	844	792	100	152
44	845	793	101	153
45	846	794	102	154
46	847	795	103	155
47	848	796	104	156
48	849	797	105	157
49	850	798	106	158
51	851	799	107	159

6 Buried Logic Cells
B11 - B6 node 185 - 190
LCK3 pin 35; Quadrant Latch Clock
RCK3 pin 36; Quadrant Synchronous Register Clock

Quadrant IV

Pin	Input Latch	Sum Term A	Sum Term B	Sum Term C
52	852	800	108	160
53	853	801	109	161
55	854	802	110	162
56	855	803	111	163
57	856	804	112	164
58	857	805	113	165
59	858	806	114	166
60	859	807	115	167
61	860	808	116	168
62	861	809	117	169
63	862	810	118	170
64	863	811	119	171
65	864	812	120	172

6 Buried Logic Cells
B5 - B0 node 191 - 196
LCK4 pin 68; Quadrant Latch Clock
RCK4 pin 66; Quadrant Synchronous Register Clock

Quadrant I

Sum Term

Pin	A	B	C
4	157	209	105
5	156	208	104
6	155	207	103
7	154	206	102
8	153	205	101
9	152	204	100
10	151	203	99
11	150	202	98
12	149	201	97
13	148	200	96
14	147	199	95
15	146	198	94
17	145	197	93

6 Buried Logic Cells
B23 - B18 node 74 - 69
LCK1 pin 1; Quadrant Latch Clock
RCK1 pin 2; Quadrant Synchronous Register Clock

Quadrant II

Sum Term

Pin	A	B	C
18	158	210	106
19	159	211	107
21	160	212	108
22	161	213	109
23	162	214	110
24	163	215	111
25	164	216	112
26	165	217	113
27	166	218	114
28	167	219	115
29	168	220	116
30	169	221	117
31	170	222	118

6 Buried Logic Cells
B17 - B12 node 75 - 80
LCK2 pin 34; Quadrant Latch Clock
RCK2 pin 32; Quadrant Synchronous Register Clock

Quadrant III

Sum Term

Pin	A	B	C
38	183	235	131
39	182	234	130
40	181	233	129
41	180	232	128
42	179	231	127
43	178	230	126
44	177	229	125
45	176	228	124
46	175	227	123
47	174	226	122
48	173	225	121
49	172	224	120
51	171	223	119

6 Buried Logic Cells
B11 - B6 node 86 - 81
LCK3 pin 35; Quadrant Latch Clock
RCK3 pin 36; Quadrant Synchronous Register Clock

Quadrant IV

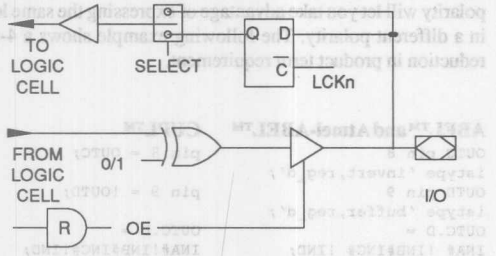
Sum Term

Pin	A	B	C
52	184	236	132
53	185	237	133
55	186	238	134
56	187	239	135
57	188	240	136
58	189	241	137
59	190	242	138
60	191	243	139
61	192	244	140
62	193	245	141
63	194	246	142
64	195	247	143
65	196	248	144

6 Buried Logic Cells
B5 - B0 node 87 - 92
LCK4 pin 68; Quadrant Latch Clock
RCK4 pin 66; Quadrant Synchronous Register Clock

Input Latch

Each of the 52 I/Os has an input latch that can be enabled and disabled individually. When the latch is enabled and latch clock is high, the pin value is latched. When the quadrant latch clock is low, the latch becomes transparent. When the latch is disabled, an ATV5100 I/O acts like those of the ATV750 and ATV2500 I/Os. The pin input is fed directly to the array (except when sum term B is being used as a buried feedback).



The .D and the .LE (latch enable) equations are required to enable the input latch in ABEL AHDL. The only allowed input to the latch is the IO pin with which it is associated. The only allowed .LE input is the quadrant latch clock (pin 1,34, 35, or 68). Notice that CUPL™ does not have node numbers for the input latches. Any pin name used in a feedback with the dot extension IOL tells CUPL™ that particular pin should be a latched pin.

ABEL™ and Atmel-ABEL™

```
ACKL.D = ACK;
ACKL.LE = LENA;
OUTA := ACKL;
```

CUPL™

```
OUTA.D = ACK.IOL;
```

Internal Combinatorial Feedback for an I/O Cell

To implement the combinatorial feedback of the B sum term, first define the node name with the corresponding node number. This node will take a five product term equation. Regular syntax describing a combinatorial equation will describe the B sum term.

Note: This B sum term node number is defined only when this feature is needed. When this feature is used, the output is from Q1 through an inverter/buffer. *The I/O pin becomes a output-only pin. It cannot be used as an input or as an input/output.*

ABEL™ and Atmel-ABEL™

```
OUTA pin 5;
EXPAND node 70;
OUTA.D =
INA&INB# !INC&!IND;
EXPAND = INA & !INC # IND;
```

CUPL™

```
pin 5 = OUTA;
pinnode 208 = EXPAND;
OUTA.D =
INA&INB#!INC&!IND;
EXPAND = INA & !INC # IND;
```

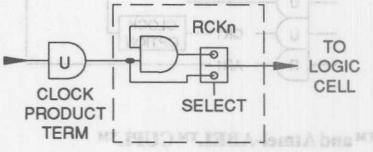
(OUTA and EXPAND are in the same I/O Logic Cell. OUTA is the Q1 output to pin after the inverter/buffer and EXPAND is the combinatorial sum term feedback. The feedbacks from this Logic Cell are Q1 before the inverter/buffer, Q2, and the B sum term)

Clocking Options

There are different methods of clocking the registers in the ATV5100. The clock options can best described as either the AND function of (Quadrant Clock & Clock Product Term) or purely the function of the Clock Product Term (like ATV750 and ATV2500).

Synchronous Operation

The quadrant clock is the only clocking element in this mode of operation. The clock product term must be defined to be equal to 1. In ABEL AHDL, .CK defines the clock product term and .CE



is the corresponding quadrant clock.

In CUPL, .CE has a different implication. The keyword .CE means the user wants the AND function (Quadrant Clock & Clock Product Term) for the clock.

ABEL™ and Atmel-ABEL™

```
OUTA.CK = 1;
OUTA.CE = CLOCK; "CLOCK is pin 2
```

CUPL™

```
OUTA.CE = 'B'1;
```

Gated Synchronous Operation

This clock option still uses the fast quadrant register clock pin, but now it has a gating element. The clock product term enables or disables the clock going to the register.

ABEL™ and Atmel-ABEL™

```
OUTA.CK = INX & INY & !INZ;
OUTA.CE = CLOCK; "CLOCK is pin 2
```

CUPL™

```
OUTA.CE =
INX&INY&!INZ;
```

Asynchronous Operation

The quadrant clock has no effect on the register in this mode of clock option. The register is clocked by the clock product term like the ATV750 and ATV2500 registers.

ABEL™ and Atmel-ABEL™

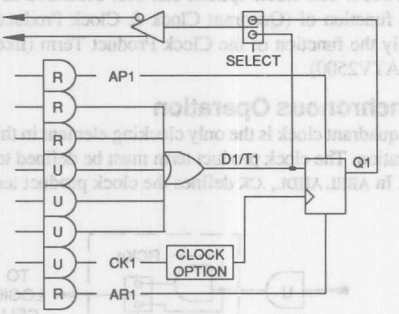
```
OUTA.CK =
INA & !INB & INC;
```

CUPL™

```
OUTA.CK =
INA & !INB & INC;
```

Buried Logic Cells

There are six Buried Logic Cells in each quadrant. Every Buried Logic Cell can be configured as a buried register or as a combinatorial feedback to the quadrant array. In the buried register mode, it's used the same way as Q1 and Q2. In the combinatorial feedback mode, it's used the same way as the B sum term feedback.



ABEL™ and Atmel-ABEL™	CUPL™
`ADDR,XDATA node 173,174;`	`pinnode 74,73 = ADDR,XDATA;`
`ADDR = A16&A15&!A14#RST;`	`ADDR = A16&A15&!A14#RST;`
`XDATA.T = !A16 & RST;`	`XDATA.T = !A16 & RST;`
`XDATA.CK = INA & INC;`	`XDATA.CK = INA & INC;`
`XDATA.AR = INB;`	`XDATA.AR = INB;`

D-Type and T-Type Registers

All the registers in the ATV5100 can be configured as D- or T-type. The ISTYPE statement after the PIN or NODE definition in ABEL AHDL tells ABEL which type of register is needed.

ABEL™ and Atmel-ABEL™	CUPL™
`ABC node 123 istype 'reg_t';`	`pinnode 103 = ABC;`
`XYZ pin 7 istype 'reg_d';`	`pin 7 = XYZ;`
`ABC.T = INA & INB # INC;`	`ABC.T = INA & INB # INC;`
`XYZ.D = !INA # INC;`	`XYZ.D = !INA # INC;`

In both languages, the .T extension is reserved for T flip-flop and .D extension for D flip-flop.

Asynchronous Preset and Reset

One of the advantanges of having a programmable output polarity I/O is that the same combinatorial output often takes fewer product terms to implement using negative logic rather than positive logic or vice versa.

The same can be done for a registered output provided the power-up state is not crucial (all flip-flops are reset upon power up). With an Asynchronous Preset and an Asynchronous Reset, simply swap the two product terms and invert your equation and polarity will let you take advantage of expressing the same logic in a different polarity. The following example shows a 4-to-1 reduction in product term requirement.

ABEL™ and Atmel-ABEL™	CUPL™
`OUTC pin 8`	`pin 8 = OUTC;`
`istype 'invert,reg_d';`	
`OUTD pin 9`	`pin 9 = !OUTD;`
`istype 'buffer,reg_d';`	
`OUTC.D =`	`OUTC.D =`
`INA# !INB#INC# !IND;`	`INA#!INB#INC#!IND;`
`OUTC.CK = CLK;`	`OUTC.CK = CLK;`
`OUTC.AR = !INA & RST;`	`OUTC.AR = !INA & RST;`
`OUTC.AP = INB & PRESET;`	`OUTC.AP = INB & PRESET;`
`OUTD.D =`	`OUTD.D =`
`!INA&INB&!INC&IND;`	`!INA&INB&!INC&IND;`
`OUTD.CK = CLK;`	`OUTD.CK = CLK;`
`OUTD.AR = INB & PRESET;`	`OUTD.AR = INB & PRESET;`
`OUTD.AP = !INA & RST;`	`OUTD.AP = !INA & RST;`

In the ATV5100, all Asynchronous Reset and Preset terms are regional. Hence, their inputs must be from the eight dedicated input pins or from the other regional bus signals (logic cell Q1 and Q2 feedback and buried cell feedback).

ABEL™ and CUPL™ may be trademarks of others.

Example ABEL™ Description File

```
module  V5100;
title   'Demo ATV5100 features with ATMEL-ABEL (IBM386 or compatible)
        ATMEL Corporation EPLD    Joe Yu          May 20, 1992'
V5K device 'P5100';
"  The IOs, registers, latches, inputs, and combinatorial sum terms feedbacks are named "with the
following prefixes for clarity:
"  Prefix
"  I      -  Quadrant Clocks, Latch Enables.
"  IO     -  IO pins
"  IL     -  Input Latches
"  BLC    -  Buried Logic Cells
"  STF    -  Sum Term Feedbacks
"  Valid ABEL AHDL identifiers can be used in place of them.
declarations
I1 pin 1;     " Quadrant 1   Latch Enable/Input
I2 pin 2;     " Quadrant 1   Synchronous Register Clock/Input
I32 pin 32;   " Quadrant 2   Synchronous Register Clock/Input
I34 pin 34;   " Quadrant 2   Latch Enable/Input
I35 pin 35;   " Quadrant 3   Latch Enable/Input
I36 pin 36;   " Quadrant 3   Synchronous Register Clock/Input
I66 pin 66;   " Quadrant 4   Synchronous Register Clock/Input
I68 pin 68;   " Quadrant 4   Latch Enable/Input
"    **** Quadrant I ****
" I/O LOGIC CELL
" ===============
IO4,IO5,IO6,IO7,IO8,IO9                          pin 4,5,6,7,8,9 istype 'buffer,reg_d';
STF4,STF5,STF6,STF7,STF8,STF9                    node 69,70,71,72,73,74;
IO4Q1,IO5Q1,IO6Q1,IO7Q1,IO8Q1,IO9Q1              node 761,762,763,764,765,766 ;
IO4Q2,IO5Q2,IO6Q2,IO7Q2,IO8Q2,IO9Q2              node 121,122,123,124,125,126 ;
IO10,IO11,IO12,IO13,IO14,IO15,IO17               pin 10,11,12,13,14,15,17 istype 'buffer,reg_d';
STF10,STF11,STF12,STF13,STF14,STF15,STF17        node 75,76,77,78,79,80,81;
IO10Q1,IO11Q1,IO12Q1,IO13Q1,IO14Q1,IO15Q1,IO17Q1 node 767,768,769,770,771,772,773 ;
IO10Q2,IO11Q2,IO12Q2,IO13Q2,IO14Q2,IO15Q2,IO17Q2 node 127,128,129,130,131,132,133 ;
" INPUT LATCHES
" ===============
IL4,IL5,IL6,IL7,IL8,IL9                          node 813,814,815,816,817,818;
IL10,IL11,IL12,IL13,IL14,IL15,IL17               node 819,820,821,822,823,824,825;
" BURIED LOGIC CELL
" =================
BLC18,BLC19,BLC20,BLC21,BLC22,BLC23              node 178,177,176,175,174,173 ;
declarations "   **** Quadrant II ****
" I/O LOGIC CELL
" ==============
IO18,IO19,IO21,IO22,IO23,IO24                    pin 18,19,21,22,23,24 istype 'buffer,reg_d';
STF18,STF19,STF21,STF22,STF23,STF24              node 82,83,84,85,86,87;
IO18Q1,IO19Q1,IO21Q1,IO22Q1,IO23Q1,IO24Q1        node 774,775,776,777,778,779;
IO18Q2,IO19Q2,IO21Q2,IO22Q2,IO23Q2,IO24Q2        node 134,135,136,137,138,139;
IO25,IO26,IO27,IO28,IO29,IO30,IO31               pin 25,26,27,28,29,30,31 ISTYPE 'BUFFER';
STF25,STF26,STF27,STF28,STF29,STF30,STF31        node 88,89,90,91,92,93,94;
IO25Q1,IO26Q1,IO27Q1,IO28Q1,IO29Q1,IO30Q1,IO31Q1 node 780,781,782,783,784,785,786 ;
IO25Q2,IO26Q2,IO27Q2,IO28Q2,IO29Q2,IO30Q2,IO31Q2 node 140,141,142,143,144,145,146 ;
" INPUT LATCHES
" ===============
IL18,IL19,IL21,IL22,IL23,IL24                    node 826,827,828,829,830,831;
IL25,IL26,IL27,IL28,IL29,IL30,IL31               node 832,833,834,835,836,837,838;
" BURIED LOGIC CELL
" =================
BLC12,BLC13,BLC14,BLC15,BLC16,BLC17              node 184,183,182,181,180,179;
declarations "    **** Quadrant III ****
```

```
IO38,IO39,IO40,IO41,IO42,IO43                    pin 38,39,40,41,42,43;
STF38,STF39,STF40,STF41,STF42,STF43              node 95,96,97,98,99,100;
IO38Q1,IO39Q1,IO40Q1,IO41Q1,IO42Q1,IO43Q1        node 787,788,789,790,791,792;
IO38Q2,IO39Q2,IO40Q2,IO41Q2,IO42Q2,IO43Q2        node 147,148,149,150,151,152 istype 'reg_t';
IO44,IO45,IO46,IO47,IO48,IO49,IO51               pin 44,45,46,47,48,49,51;
STF44,STF45,STF46,STF47,STF48,STF49,STF51        node 101,102,103,104,105,106,107;
IO44Q1,IO45Q1,IO46Q1,IO47Q1,IO48Q1,IO49Q1,IO51Q1 node 793,794,795,796,797,798,799;
IO44Q2,IO45Q2,IO46Q2,IO47Q2,IO48Q2,IO49Q2,IO51Q2 node 153,154,155,156,157,158,159;
" INPUT LATCHES
" ===============
IL38,IL39,IL40,IL41,IL42,IL43                    node 839,840,841,842,843,844;
IL44,IL45,IL46,IL47,IL48,IL49,IL51               node 845,846,847,848,849,850,851;
" BURIED LOGIC CELL
" =================
BLC6,BLC7,BLC8,BLC9,BLC10,BLC11                  node 190,189,188,187,186,185 ISTYPE 'REG_D';
declarations "    **** Quadrant IV ****
" I/O LOGIC CELL
" ==============
IO52,IO53,IO55,IO56,IO57,IO58                    pin 52,53,55,56,57,58 istype 'buffer';
STF52,STF53,STF55,STF56,STF57,STF58              node 108,109,110,111,112,113;
IO52Q1,IO53Q1,IO55Q1,IO56Q1,IO57Q1,IO58Q1        node 800,801,802,803,804,805;
IO52Q2,IO53Q2,IO55Q2,IO56Q2,IO57Q2,IO58Q2        node 160,161,162,163,164,165;
IO59,IO60,IO61,IO62,IO63,IO64,IO65               pin 59,60,61,62,63,64,65 istype 'buffer';
STF59,STF60,STF61,STF62,STF63,STF64,STF65        node 114,115,116,117,118,119,120;
IO59Q1,IO60Q1,IO61Q1,IO62Q1,IO63Q1,IO64Q1,IO65Q1 node 806,807,808,809,810,811,812;
IO59Q2,IO60Q2,IO61Q2,IO62Q2,IO63Q2,IO64Q2,IO65Q2 node 166,167,168,169,170,171,172;
" INPUT LATCHES
" ===============
IL52,IL53,IL55,IL56,IL57,IL58                    node 852,853,854,855,856,857;
IL59,IL60,IL61,IL62,IL63,IL64,IL65               node 858,859,860,861,862,863,864;
" BURIED LOGIC CELL
" =================
BLC0,BLC1,BLC2,BLC3,BLC4,BLC5                    node 196,195,194,193,192,191;
   H,L,C,D,K,U,X,Z = 1,0,.C.,.D.,.K.,.U.,.X.,.Z.;
"   MACRO (INPUT LATCH)
INPUT_LATCH MACRO (IL,IO,QUAD_LE)
{?IL.D  = ?IO;
?IL.LE  = ?QUAD_LE;}
equations
"            INPUT LATCH
"  Each of the 52 I/Os has an input latch. When the quadrant latch enable is high, the
"  pin value is latched.
"  When the quadrant latch clock is low, the latch becomes transparent.

IL4.D   = IO4;       "The .D and the .LE (latch enable) extentions are required to describe a
IL4.LE  = I1;        "latch in. ABEL AHDL. The only allowed input to the latch is the IO pin
                     "it associates with.The only allowed .LE input is the quadrant latch
                     "enable. They are Pin 1, 34, 35, and 68.
"  INPUT_LATCH macro is another way to describe the latch.
INPUT_LATCH (IL5,IO5,I1);   "Latch Pin 5
INPUT_LATCH (IL6,IO6,I1);   "Latch Pin 6
IO4.d   = !IO4.fb;  " When .oe is enabled by IO8, IO4 outputs a 1 bit counter.
IO4.oe  = I34;      " When .oe is disabled by !I34, IO4 latches a data bit  from the bus.
IO4.ck  = 1;
IO4.ce  = I2;
IO7=    IL4;
test_vectors (   "Test the latches...
[I1,I2,I34,IO4]-[IO4,IO7])
[ 0, 0, 1,X  ]  -> [  0,   0 ]; "Transparent
[ 0, C, 1,X  ]  -> [  1,   1 ]; "Transparent
[ U, 0, 0,0  ]  -> [  Z,   0 ]; "Disable .oe and latch 0
```

```
[ 1, C, 1,X  ]  ->  [  0,   0 ]; "Latched 0
[ 1, C, 1,X  ]  ->  [  1,   0 ]; "Latched 0
[ D, C, 1,X  ]  ->  [  0,   0 ]; "Transparent
[ 0, C, 1,X  ]  ->  [  1,   1 ]; "Transparent
[ 0, C, 1,X  ]  ->  [  0,   0 ]; "Transparent
[ U, 0, 0,1  ]  ->  [  Z,   1 ]; "Disable .oe and latch 1
[ 1, 0, 1,X  ]  ->  [  0,   1 ]; "Latched 1
[ 1, C, 1,X  ]  ->  [  1,   1 ]; "Latched 1
[ 1, C, 1,X  ]  ->  [  0,   1 ]; "Latched 1
equations
"  CLOCKING OPTIONS
"  There are different methods of clocking the registers in the ATV5001. The clock is
"  best described as either the AND function of (Quadrant Clock & Clock Product term)
"  or the product term by it self. In the following examples the register can be a name
"  from a pin, Q1, Q2, or Buried Logic Cell. The register can be either .t or.d
"  flip-flop.
IO22.d    =  !IO22.fb;
IO22.ck   =  IO18 & !IO19;  "Note there is no .ce equation defined.This is an asynchronous
IO22.ar   =  I66;           "clocking method  where the quadrant clock  has no effect.

test_vectors (
[IO18,IO19,I66  ]  ->  [ IO22 ])
[  0,   0,1     ]  ->  [   0 ];
[  0,   0,0     ]  ->  [   0 ];
[  C,   0,0     ]  ->  [   1 ];
[  C,   0,0     ]  ->  [   0 ];
equations
IO23.d    =  !IO23.fb;
IO23.ck   =  IO18 & !IO19;  "The clock product term (.ck) is used to gate the quadrant
                            "clock pin.
IO23.ce   =  I32;           "Using quadrant clock pin in a synchronous mode allows higher
                            "clock rate.
IO23.ar   =  I66;           "Pin 32 is the Quadrant 2 clock pin.
test_vectors (
[I32,IO18,IO19,I66  ]  ->  [ IO23])
[  0,   1,0,  1     ]  ->  [  0];
[  C,   0,0,  0     ]  ->  [  0]; "Product term blocks quadrant clock
[  C,   1,0,  0     ]  ->  [  1]; "Product term enables quadrant clock
[  C,   1,0,  0     ]  ->  [  0];
equations
IO24.d    =  !IO24.fb;
IO24.ck   =  1;             "Note that the .ck is defined to 1. The quadrant clock is the only
                            "clocking element.
IO24.ce   =  I32;           "The .ce is Pin 32 because it's the proper quadrant clock to use for
IO24.ar   =  I66;           "synchronous  operation.

test_vectors (
[ I32, I66   ]  ->  [ IO24  ])
[  0,   1    ]  ->  [  0    ];
[  C,   0    ]  ->  [  1    ];
[  C,   0    ]  ->  [  0    ];
[  C,   0    ]  ->  [  1    ];
"   D-TYPE and T-TYPE REGISTERS
"  All the registers in the ATV5001 can be configured as D or T type. The ISTYPE
"  statement after the PIN or NODE definition tells ABEL which type of register is
"  needed.

"  ABC    node   122 istype 'reg_t';
"  XYZ    pin    5 istype 'reg_d';
"  Use the .t extension for ABC and .d extension for XYZ when you write the equations.

equations
" 3 Bit Synchronous Counter using T flip-flops
```

```
IO38Q2.t = 1;                IO38Q2.ck = 1;      IO38Q2.ce = I36;     IO38Q2.ar = I68;
IO39Q2.t = IO38Q2;           IO39Q2.ck = 1;      IO39Q2.ce = I36;     IO39Q2.ar = I68;
IO40Q2.t = IO38Q2 & IO39Q2;                      IO40Q2.ck = 1;       IO40Q2.ce = I36;IO40Q2.ar

test_vectors (
[ I36, I68    ]  -> [ IO40Q2,IO39Q2,IO38Q2])
[  0,   1     ]  -> [   0,   0,   0  ];
[  C,   0     ]  -> [   0,   0,   1  ];
[  C,   0     ]  -> [   0,   1,   0  ];
[  C,   0     ]  -> [   0,   1,   1  ];
[  C,   0     ]  -> [   1,   0,   0  ];
[  C,   0     ]  -> [   1,   0,   1  ];
[  C,   0     ]  -> [   1,   1,   0  ];
[  C,   0     ]  -> [   1,   1,   1  ];
[  C,   0     ]  -> [   0,   0,   0  ];

equations
" 3 Bit Synchronous Counter using D flip-flops

BLC6.d = !BLC6;              BLC6.ck = 1;        BLC6.ce = I36;       BLC6.ar = I68;
BLC7.d = BLC6 $ BLC7;        BLC7.ck = 1;        BLC7.ce = I36;       BLC7.ar = I68;
BLC8.d = BLC8 $ (BLC6 & BLC7); BLC8.ck = 1;      BLC8.ce = I36;       BLC8.ar = I68;

test_vectors (
[ I36, I68    ]  -> [BLC8,BLC7,BLC6])
[  0,   1     ]  -> [  0,   0,   0  ];
[  C,   0     ]  -> [  0,   0,   1  ];
[  C,   0     ]  -> [  0,   1,   0  ];
[  C,   0     ]  -> [  0,   1,   1  ];
[  C,   0     ]  -> [  1,   0,   0  ];
[  C,   0     ]  -> [  1,   0,   1  ];
[  C,   0     ]  -> [  1,   1,   0  ];
[  C,   0     ]  -> [  1,   1,   1  ];
[  C,   0     ]  -> [  0,   0,   0  ];
"       UNIVERSAL AND REGIONAL PRODUCT TERMS
"  A Regional product term has inputs from all the feedbacks of its quadrant Buried
"  Logic Cells, Q1's, Q2's,and the dedicated Inputs. In addition, a Universal product
"  term has the Pin/B Sum Term Feedbacks.
"       OUTPUTS and FEEDBACKS
"  Combinatorial:
"  Use IO pin name to define the equation. The sum terms may combine to allow 5, 9, or
"  13 product terms depending on the need of the reduced equation. If the reduced
"  equation requires 5 or less product terms, it leaves Q1 and Q2 each with 4 product
"  terms to use.
"       IO52              =    up to 5 PRODUCT TERMS (3UNIVERSAL)
"       IO52.oe           =    1 PRODUCT TERM (REGIONAL)
"       IO52Q1.(d or t) =      up to 4 PRODUCT TERMS (2 UNIVERSAL)
"       IO52Q1.ck         =    1 PRODUCT TERM (1 UNIVERSAL)
"       IO52Q1.ce         =    QUADRANT CLOCK
"       IO52Q1.ar         =    1 PRODUCT TERM  (REGIONAL)
"       IO52Q1.ap         =    1 PRODUCT TERM  (REGIONAL)
"       IO52Q2.(d or t) =      up to 4 PRODUCT TERMS (3 UNIVERSAL)
"       IO52Q2.ck         =    1 PRODUCT TERM (1 UNIVERSAL)
"       IO52Q2.ce         =    QUADRANT CLOCK
"       IO52Q2.ar         =    1 PRODUCT TERM  (REGIONAL)
"       IO52Q2.ap         =    1 PRODUCT TERM (REGIONAL)
"  ALLOWED FEEDBACKS:          SOURCE:
"  IO52                   --    Pin feedback, after the buffer/inverter.
"  IO52Q1,IO52Q1.FB       --    Q1 register feedback.
"  IO52Q2,IO52Q2.FB       --    Q2 register feedback.
"  Combinatorial:
"  If the reduced equation requires 6 to 9 product terms, it leaves Q2 with 4 product
"  terms to use. Q1 will feedback the A Sum Term portion of the output logic.
```

```
"       IO52            =    up to 9 PRODUCT TERMS (5 UNIVERSAL)
"       IO52.oe         =    1 PRODUCT TERM (REGIONAL)
"       IO52Q2.(d or t) =    up to 4 PRODUCT TERMS (3 UNIVERSAL)
"       IO52Q2.ck       =    1 PRODUCT TERM (1 UNIVERSAL)
"       IO52Q2.ce       =    QUADRANT CLOCK
"       IO52Q2.ar       =    1 PRODUCT TERM (REGIONAL)
"       IO52Q2.ap       =    1 PRODUCT TERM (REGIONAL)
"   ALLOWED FEEDBACKS:         SOURCE:
"   IO52                --     Pin feedback, after the buffer/inverter.
"   IO52Q2,IO52Q2.FB    --     Q2 register feedback.
"   Combinatorial:
"   If the reduced equation requires more than 9 product terms, it leaves no product
"   terms for Q1 and Q2. Q1 feeds back A Sum Term and Q2 feeds back C Sum Term.
"       IO52            =    up to 13 PRODUCT TERMS (8 UNIVERSAL)
"       IO52.oe         =    1 PRODUCT TERM (REGIONAL)
"   ALLOWED FEEDBACKS:         SOURCE:
"   IO52                --     Pin feedback, after the buffer/inverter.
"   Registered:
"   Use IO pin name to define the equation. The sum terms may combine to allow 4, 9, or
"   13 product terms depending on the need of the reduced equation. If the reduced
"   equation requires 4 or less product terms, you may define a 5 product term equation
"   for the STF (Sum Term Feedback) and define a 4 product term equation for Q2.
"       IO52.(d or t)   =    up to 4 PRODUCT TERMS (2 UNIVERSAL)
"       IO52.oe         =    1 PRODUCT TERM (REGIONAL)
"       IO52.ck         =    1 PRODUCT TERM (1 UNIVERSAL)
"       IO52.ce         =    QUADRANT CLOCK
"       IO52.ar         =    1 PRODUCT TERM (REGIONAL)
"       IO52.ap         =    1 PRODUCT TERM (REGIONAL)
"       STF52           =    up to 5 PRODUCT TERMS (3 UNIVERSAL)
"       IO52Q2.(d or t) =    up to 4 PRODUCT TERMS (3 UNIVERSAL)
"       IO52Q2.ck       =    1 PRODUCT TERM (1 UNIVERSAL)
"       IO52Q2.ce       =    QUADRANT CLOCK
"       IO52Q2.ar       =    1 PRODUCT TERM (REGIONAL)
"       IO52Q2.ap       =    1 PRODUCT TERM (REGIONAL)

"   ALLOWED FEEDBACKS:         SOURCE:
"   IO52.FB,IO52.Q      --     Register feedback prior to buffer/inverter.
"   IO52Q2              --     Q2 register feedback.
"   STF52               --     Sum Term Feedback for logic expansion.
"   Registered:
"   If the reduced equation requires 9 to 5 product terms, you may write a 4 product
"   term equation for Q2.
"       IO52.(d or t)   =    up to 9 PRODUCT TERMS (5 UNIVERSAL)
"       IO52.oe         =    1 PRODUCT TERM (REGIONAL)
"       IO52.ck         =    1 PRODUCT TERM (1 UNIVERSAL)
"       IO52.ce         =    QUADRANT CLOCK
"       IO52.ar         =    1 PRODUCT TERM (REGIONAL)
"       IO52.ap         =    1 PRODUCT TERM (REGIONAL)
"       IO52Q2.(d or t) =    up to 4 PRODUCT TERMS (3 UNIVERSAL)
"       IO52Q2.ck       =    1 PRODUCT TERM (1 UNIVERSAL)
"       IO52Q2.ce       =    QUADRANT CLOCK
"       IO52Q2.ar       =    1 PRODUCT TERM (REGIONAL)
"       IO52Q2.ap       =    1 PRODUCT TERM (REGIONAL)
"   ALLOWED FEEDBACKS:         SOURCE:
"   IO52                --     Pin feedback, after the buffer/inverter.
"   IO52.FB             --     Register feedback prior to buffer/inverter.
"   IO52Q2              --     Q2 register feedback.
"   Registered:
"   If the reduced equation requires more than 9 product terms, it leaves zero product
terms for Q1 and Q2.
"       IO52.(d or t)   =    up to 13 PRODUCT TERMS (8 UNIVERSAL)
"       IO52.oe         =    1 PRODUCT TERM (REGIONAL)
"       IO52.ck         =    1 PRODUCT TERM (1 UNIVERSAL)
```

```
"       IO52.ar          =    1 PRODUCT TERM (REGIONAL)
"       IO52.ap          =    1 PRODUCT TERM (REGIONAL)
"  ALLOWED FEEDBACKS:          SOURCE:
"  IO52                 --     Pin feedback, after the buffer/inverter.
"  IO52.FB              --     Register feedback prior to buffer/inverter.
"       AP, AR, and CK
"  Each of the 128 registers has its own .AP (Asynchronous Preset), .AR (Asynchronous
"  Reset) and .CK. AlL CKs are Universal product terms. The ARs and APs are Regional
"  product terms.
"  NOTE:  AP and AR should never be active at the same time.

equations
IO10.d    =  !IO10.fb;
IO10.ck   =  IO8;
IO10.ar   =  I66;
IO10.ap   =  I35;

test_vectors (
[ IO8, I66, I35 ]  ->  [ IO10 ])
[  0,   1,0     ]  ->  [    0 ]; "AR
[  0,   0,0     ]  ->  [    0 ];
[  C,   0,0     ]  ->  [    1 ];
[  C,   0,0     ]  ->  [    0 ];
[  0,   0,1     ]  ->  [    1 ]; "AP
[  0,   1,0     ]  ->  [    0 ]; "AR
"        BURIED LOGIC CELLS
"  Buried Logic Cell can be configured as a register feedback like Q2. It can also be
"  configured as  combinatorial feedback to accommodate for logic expansion.

equations
BLC17.t   =  1; "Registered
BLC17.ck  =  IO9;
BLC17.ar  =  I66;
BLC14     =  I1; "Combinatiorial
IO25      =  BLC17;
IO26      =  BLC14;

test_vectors (
[IO9, I66,   I1 ]  ->  [ BLC17,BLC14,IO25,IO26])
[  0,1,0     ]  ->  [    0,   0,   0,   0  ];
[  C,  0,0   ]  ->  [    1,   0,   1,   0  ];
[  0,  0,   1]  ->  [    1,   1,   1,   1  ];
[  C,  0,1   ]  ->  [    0,   1,   0,   1  ];
[  C,  0,   0]  ->  [    1,   0,   1,   0  ] ;
END;
```

Example CUPL™ Description File

```
Name      V5100CU;
Partno    NA;
Date      5/20/92;
Revision  01;
Designer  Joe Yu;
Company   ATMEL Corporation;
Assembly  NA;
Location  U1;
Device    V5100;
Format    j;
/* Compiled with CUPL 386 version */
/* The IOs, registers, inputs, and combinatorial sum terms feedbacks are named with
/* the following prefixes for clarity:

*  Prefix
 * I      -  Quadrant Clocks, Latch Enables.
 * IO     -  IO pins
 * BLC    -  Buried Logic Cells
 * STF    -  Sum Term Feedbacks
 * Valid CUPL HDL identifiers can be used in place of them. */

pin 1   = I1;       /* Quadrant 1              Latch Enable/Input    */
pin 2   = I2;       /* Quadrant 1              Synchronous Register Clock/Input*/
pin 32  = I32;      /* Quadrant 2              Synchronous Register Clock/Input*/
pin 34  = I34;      /* Quadrant 2              Latch Enable/Input    */
pin 35  = I35;      /* Quadrant 3              Latch Enable/Input    */
pin 36  = I36;      /* Quadrant 3              Synchronous Register Clock/Input*/
pin 66  = I66;      /* Quadrant 4              Synchronous Register Clock/Input*/
pin 68  = I68;      /* Quadrant 4              Latch Enable/Input    */
        /**** Quadrant I ****/
/* I/O LOGIC CELL    */
/* ==============    */
pin       [4..9]          = [IO4..9];
pinnode   [209..204]      = [STF4..9];
pinnode   [157..152]      = [IO4Q1,IO5Q1,IO6Q1,IO7Q1,IO8Q1,IO9Q1];
pinnode   [105..100]      = [IO4Q2,IO5Q2,IO6Q2,IO7Q2,IO8Q2,IO9Q2];
pin       [10..15,17]     = [IO10..15,IO17];
pinnode   [203..197]      = [STF10..15,STF17];
pinnode   [151..145]      = [IO10Q1,IO11Q1,IO12Q1,IO13Q1,IO14Q1,IO15Q1,IO17Q1];
pinnode   [99..93]        = [IO10Q2,IO11Q2,IO12Q2,IO13Q2,IO14Q2,IO15Q2,IO17Q2];
/* BURIED LOGIC CELL    */
/* =================    */
pinnode   [69..74]        = [BLC18..23];
        /**** Quadrant II ****/
/* I/O LOGIC CELL    */
/* ==============    */
pin       [18,19,21..24]  = [IO18,IO19,IO21..24];
pinnode   [210..215]      = [STF18,STF19,STF21..24];
pinnode   [158..163]      = [IO18Q1,IO19Q1,IO21Q1,IO22Q1,IO23Q1,IO24Q1];
pinnode   [106..111]      = [IO18Q2,IO19Q2,IO21Q2,IO22Q2,IO23Q2,IO24Q2];
pin       [25..31]        = [IO25..31];
pinnode   [216..222]      = [STF25..31];
pinnode   [164..170]      = [IO25Q1,IO26Q1,IO27Q1,IO28Q1,IO29Q1,IO30Q1,IO31Q1];
pinnode   [112..118]      = [IO25Q2,IO26Q2,IO27Q2,IO28Q2,IO29Q2,IO30Q2,IO31Q2];
/* BURIED LOGIC CELL    */
/* =================    */
pinnode   [80..75]        = [BLC12..17];
        /**** Quadrant III ****/
/* I/O LOGIC CELL    */
/* ==============    */
```

7

```
pin       [38..43]          = [IO38..43];
pinnode   [235..230]        = [STF38..43];
pinnode   [183..178]        = [IO38Q1,IO39Q1,IO40Q1,IO41Q1,IO42Q1,IO43Q1];
pinnode   [131..126]        = [IO38Q2,IO39Q2,IO40Q2,IO41Q2,IO42Q2,IO43Q2];
pin       [44..49,51]       = [IO44..49,IO51];
pinnode   [229..223]        = [STF44..49,STF51];
pinnode   [177..171]        = [IO44Q1,IO45Q1,IO46Q1,IO47Q1,IO48Q1,IO49Q1,IO51Q1];
pinnode   [125..119]        = [IO44Q2,IO45Q2,IO46Q2,IO47Q2,IO48Q2,IO49Q2,IO51Q2];
/* BURIED LOGIC CELL    */
/* =================    */
pinnode   [81..86]          = [BLC6..11];
          /**** Quadrant IV ****/
/* I/O LOGIC CELL    */
/* ==============    */
pin       [52,53,55..58]    = [IO52,IO53,IO55..58];
pinnode   [236..241]        = [STF52,STF53,STF55..58];
pinnode   [184..189]        = [IO52Q1,IO53Q1,IO55Q1,IO56Q1,IO57Q1,IO58Q1];
pinnode   [132..137]        = [IO52Q2,IO53Q2,IO55Q2,IO56Q2,IO57Q2,IO58Q2];
pin       [59..65]          = [IO59..65];
pinnode   [242..248]        = [STF59..65];
pinnode   [190..196]        = [IO59Q1,IO60Q1,IO61Q1,IO62Q1,IO63Q1,IO64Q1,IO65Q1];
pinnode   [138..144]        = [IO59Q2,IO60Q2,IO61Q2,IO62Q2,IO63Q2,IO64Q2,IO65Q2];
/* BURIED LOGIC CELL    */
/* =================    */
pinnode   [92..87]          = [BLC0..5];
/*        INPUT LATCH
   Each of the 52 I/Os has an input latch. When the quadrant latch enable is high, the
   pin value is latched.  When the quadrant latch clock is low, the latch becomes
   transparent.     */
IO4.d     =     !IO4;
IO4.oe    =     I34;
IO4.ce    =     'B'1;
IO7       =     IO4.IOL;    /* When the latched input is needed in the design, i.e.,  */
                            /*IO4.IOL, IO4 is  configured as  having a latched input. */
/*        CLOCKING OPTIONS
   There are different methods of clocking the registers in the ATV5100. The clock is
   best described as either the AND function of (Quadrant Clock & Clock Product term) or
   the product term by it self. In the following examples the register can be a name
   from a pin, Q1, Q2, or Buried Logic Cell. The register can be either  .t or .d
   flip-flop.    */
IO22.d    =     !IO22;
IO22.ck   =     IO18 & !IO19; /* Note there is no .ce equation defined. This is an    */
IO22.ar   =     I66;          /* asynchronous clocking method where the quadrant      */
                              /* clock has no effect.                                 */
IO23.d    =     !IO23;
IO23.ce   =     IO18 & !IO19; /* The clock product term is used to gate the quadrant */
IO23.ar   =     I66;          /* clock pin.Using quadrant clock pin in a synchronous */
                              /* mode allows higher clock rate. Pin 32 is the        */
                              /* Quadrant 2 clock pin.                               */

IO24.d  = !IO24;
IO24.ce   =  'B'1;            /* Note that the .ce is defined to 1. The quadrant      */
IO24.ar   =  I66;             /* clock is the only clocking element. The clock is     */
                              /* Pin 32 because it's the proper quadrant clock to     */
                              /* use for synchronous operation.                       */
/*       D-TYPE and T-TYPE REGISTERS
   All the registers in the ATV5100 can be configured as D or T type. Use the .d
   extension for D type register and .t extension for T type register.*/
/* 3 Bit Synchronous Counter using T flip-flops */
IO38Q2.t = 'B'1;              IO38Q2.ce = 'B'1;  IO38Q2.ar = I68;
IO39Q2.t = IO38Q2;            IO39Q2.ce = 'B'1;  IO39Q2.ar = I68;
IO40Q2.t = IO38Q2 & IO39Q2;   IO40Q2.ce = 'B'1;  IO40Q2.ar = I68;
/* 3 Bit Synchronous Counter using D flip-flops */
```

```
BLC6.d = !BLC6;                  BLC6.ce = 'B'1;          BLC6.ar = I68;
BLC7.d = BLC6 $ BLC7;            BLC7.ce = 'B'1;          BLC7.ar = I68;
BLC8.d = BLC8 $ (BLC6 & BLC7);   BLC8.ce = 'B'1;          BLC8.ar = I68;
/*      UNIVERSAL AND REGIONAL PRODUCT TERMS
   A Regional product term has inputs from all the feedbacks of its quadrant Buried
   Logic Cells, Q1's, Q2's, and the dedicated Inputs. In addition, a Universal product
   term has the Pin/B Sum Term Feedbacks.          */
/*        OUTPUTS and FEEDBACKS
   Combinatorial:
   Use IO pin name to define the equation. The sum terms may combine to allow 5, 9, or
   13 product terms  depending on the need of the reduced equation. If the reduced
   equation requires 5 or less product terms,it leaves Q1 and Q2 each with 4 product
   terms to use.
        IO52                = up to 5 PRODUCT TERMS (3 UNIVERSAL)
        IO52.oe             = 1 PRODUCT TERM (REGIONAL)
        IO52Q1.(d or t)     = up to 4 PRODUCT TERMS (2 UNIVERSAL)
        IO52Q1.(ck or ce)   = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52Q1.ar           = 1 PRODUCT TERM (REGIONAL)
        IO52Q1.ap           = 1 PRODUCT TERM (REGIONAL)
        IO52Q2.(d or t)     = up to 4 PRODUCT TERMS (3 UNIVERSAL)
        IO52Q2.(ck or ce)   = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52Q2.ar           = 1 PRODUCT TERM (REGIONAL)
        IO52Q2.ap           = 1 PRODUCT TERM (REGIONAL)
   ALLOWED FEEDBACKS:       SOURCE:
   IO52,IO52.IO        --   Pin feedback, after the buffer/inverter.
   IO52Q1              --   Q1 register feedback.
   IO52Q2              --   Q2 register feedback.          */
/* Combinatorial:
   If the reduced equation requires 6 to 9 product terms, it leaves Q2 with 4 product
   terms to use. Q1 will feedback the A Sum Term portion of the output logic.
        IO52                = up to 9 PRODUCT TERMS (5 UNIVERSAL)
        IO52.oe             = 1 PRODUCT TERM (REGIONAL)
        IO52Q2.(d or t)     = up to 4 PRODUCT TERMS (3 UNIVERSAL)
        IO52Q2.(ck or ce)   = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52Q2.ar           = 1 PRODUCT TERM (REGIONAL)
        IO52Q2.ap           = 1 PRODUCT TERM (REGIONAL)
   ALLOWED FEEDBACKS:       SOURCE:
   IO52,IO52.IO        --   Pin feedback, after the buffer/inverter.
   IO52Q2              --   Q2 register feedback.          */
/* Combinatorial:
   If the reduced equation requires more than 9 product terms, it leaves no product
   terms for Q1 and Q2. Q1 feeds back A. Sum Term and Q2 feeds back C Sum Term.
        IO52      =  up to 13 PRODUCT TERMS (8UNIVERSAL)
        IO52.oe   =  1 PRODUCT TERM (REGIONAL)
   ALLOWED FEEDBACKS:       SOURCE:
   IO52,IO52.IO        --   Pin feedback, after the buffer/inverter. */
/* Registered:
   Use IO pin name to define the equation. The sum terms may combine to allow 4, 9, or
   13 product terms depending on the  need of the reduced equation. If the reduced
   equation requires 4 or less product terms, you may define a 5 product term equation
   for the STF (Sum Term Feedback) and define a 4 product term equation for Q2.
        IO52.(d or t)       = up to 4 PRODUCT TERMS (3 UNIVERSAL)
        IO52.oe             = 1 PRODUCT TERM (REGIONAL)
        IO52.(ck or ce)     = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52.ar             = 1 PRODUCT TERM (REGIONAL)
        IO52.ap             = 1 PRODUCT TERM (REGIONAL)

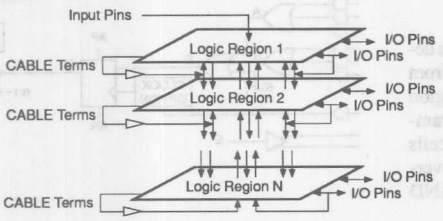
        STF52               = up to 5 PRODUCT TERMS (3 UNIVERSAL)
        IO52Q2.(d or t)     = up to 4 PRODUCT TERMS (3 UNIVERSAL)
        IO52Q2.(ck or ce)   = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52Q2.ar           = 1 PRODUCT TERM (REGIONAL)
        IO52Q2.ap           = 1 PRODUCT TERM (REGIONAL)
```

```
   ALLOWED FEEDBACKS:          SOURCE:
   IO52                --      Register feedback prior to buffer/inverter.
   IO52Q2              --      Q2 register feedback.
   STF52               --      Sum Term Feedback for logic expansion.  */
/* Registered:
   If the reduced equation requires 9 to 5 product terms, you may write a 4 product term
   equation for Q2.
        IO52.(d or t)       = up to 9 PRODUCT TERMS (5 UNIVERSAL)
        IO52.oe             = 1 PRODUCT TERM (REGIONAL)
        IO52.(ck or ce)     = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52.ar             = 1 PRODUCT TERM (REGIONAL)
        IO52.ap             = 1 PRODUCT TERM (REGIONAL)
        IO52Q2.(d or t)     = up to 4 PRODUCT TERMS (3 UNIVERSAL)
        IO52Q2.(ck or ce)   = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52Q2.ar           = 1 PRODUCT TERM (REGIONAL)
        IO52Q2.ap           = 1 PRODUCT TERM (REGIONAL)
   ALLOWED FEEDBACKS:          SOURCE:
   IO52.IO             --      Pin feedback, after the buffer/inverter.
   IO52                --      Register feedback prior to buffer/inverter.
   IO52Q2              --      Q2 register feedback.*/
/* Registered:
   If the reduced equation requires more than 9 product terms, it leaves zero product
   terms for Q1 and Q2.
        IO52.(d or t)       = up to 13 PRODUCT TERMS (8 UNIVERSAL)
        IO52.oe             = 1 PRODUCT TERM (REGIONAL)
        IO52.(ck or ce)     = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52.ar             = 1 PRODUCT TERM (REGIONAL)
        IO52.ap             = 1 PRODUCT TERM (REGIONAL)
   ALLOWED FEEDBACKS:          SOURCE:
   IO52.IO             --      Pin feedback, after the buffer/inverter.
   IO52                --      Register feedback prior to buffer/inverter.*/
/*       AP, AR, and CK
   Each of the 128 registers has its own .AP (Asynchronous Preset), .AR (Asynchronous
   Reset) and .CK or .CE. All CKs are Universal product terms. The ARs and APs are
   Regional product terms.
   NOTE:  AP and AR should never be active at the same time.          */
IO10.d  = !IO10;
IO10.ck      =      IO8;
IO10.ar      =      I66;
IO10.ap      =      I35;
/*       BURIED LOGIC CELLS
   Buried Logic Cell can be configured as a register feedback like Q2. It can also be
   configured as combinatorial feedback to accommodate for logic expansion. */
BLC17.t      =      'B'1;   /*Registered */
BLC17.ck     =      IO9;
BLC17.ar     =      I66;
BLC14        =      I1;     /*Combinatiorial */
IO25         =      BLC17;
IO26         =      BLC14;
END;
```

Features

- **High Throughput - Uniform and Predictable Performance**
- **High I/O Pin Counts**
- **High Speed - Over 80 MHz System Clock Rate Operation**
- **Flexible Interconnect Architecture - Universal Routing**
- **Multiple Flip-Flop Types - Synchronous or Asynchronous Registers**
- **Complete Third Party Software Support**
  - **No Placement, Routing or Layout Software Required**
- **Proven and Reliable High Speed CMOS EPROM Process**
  - **2000 V ESD Protection**
  - **200 mA Latchup Immunity**
- **Reprogrammable - Tested 100% for Programmability**
- **Commercial, Industrial and Military Temperature Grades**

Block Diagram



Description

The Atmel H-Series Programmable Logic Devices are easy to use, high throughput devices. Their simple, regular architecture translates into increased utilization and high performance.

The Atmel H-Series EPLDs have one programmable combinatorial logic array. This guarantees easy interconnection of and uniform performance from all nodes. Sum terms, which are easy to use blocks of gates, provide combinatorial AND/OR logic blocks. Sum terms can be wire-OR'd together to integrate larger logic blocks. Sum terms or registers can drive the I/O pins.

All registers are configurable as D- or T-types without using extra logic gates. Individual sum terms and clocks give each flip-flop added flexibility. A direct "clock-from-pin" option guarantees synchronization and fast clock to output performance.

(Continued on next page)

H-Series EPLDs

ATH3000/L	ATH4000/L	ATH4500/L	ATH5500/L
			Logic Region 10
			Logic Region 9
		Logic Region 8	Logic Region 8
	Logic Region 7	Logic Region 7	Logic Region 7
Logic Region 6	Logic Region 6	Logic Region 6	Logic Region 6
Logic Region 5	Logic Region 5	Logic Region 5	Logic Region 5
Logic Region 4	Logic Region 4	Logic Region 4	Logic Region 4
Logic Region 3	Logic Region 3	Logic Region 3	Logic Region 3
Logic Region 2	Logic Region 2	Logic Region 2	Logic Region 2
Logic Region 1	Logic Region 1	Logic Region 1	Logic Region 1

Part Number	ATH3000/L	ATH4000/L	ATH4500/L	ATH5500/L
Pins	68	84	100	132
I/Os	56	68	80	100
Flip-Flops	56	70	80	100
Logic Regions	6	7	8	10

High Throughput UV Erasable Programmable Logic Devices

7

H-Series EPLDs Overview

Description (Continued)

Standard off-the-shelf third party software tools and programmers support the H-Series. This minimizes start-up investment and improves product support.

The H-Series addresses applications that need high-frequency operation and a high I/O pin count. It achieves predictably high throughput rates over a wider range of designs than has been possible in the past through the use of innovative architecture and logic cell design. A logic cell with many possible configurations gives a finer logic granularity and maximizes logic resource usage. Complement Array Buried Logic Extender (CABLE) terms increase the connectivity between logic regions. Additional logic increases the number of input terms available to sum terms without degrading performance.

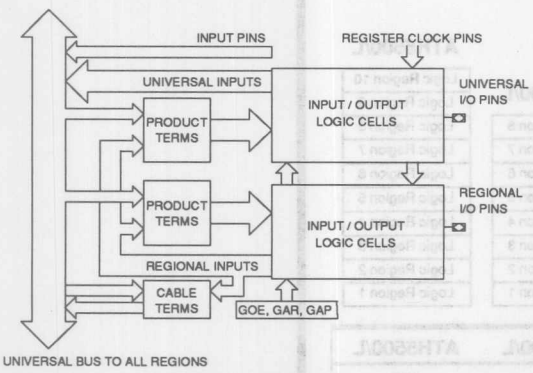
Logic Array Architecture

The block diagram shows the basic structure of the H-Series devices. Like the ATV5000 device currently available from Atmel, the H-Series uses regions within the device. Each region consists of a group of logic cells, CABLE terms, and a programmable AND logic array. Figure 1 shows that regional logic cells generate inputs that feed that region's AND logic array. Universal logic cells generate input that feed into the universal AND array, which provides interconnect to other regions.

The AND logic array for each region receives inputs from four different sources. These include the inputs from each logic cell within the region, from dedicated universal input pins, from universal logic cells, and from CABLE terms.

Each region's AND array provides complete interconnect for signals within that region. In addition, any product terms within a given region also have inputs available as the signals on the universal bus.

Figure 1. Functional Logic Diagram



Logic Cell Architecture

In the H-Series, each logic cell has eight product terms and generates one array feedback term. The product terms provide two three-inputs sum terms, a clock term, and an output enable term. Programmable switches combine sum terms with each other, and with sum terms from adjacent logic cells. This sum term joining is similar to Atmel's V-Series devices, and allows up to 12 product terms with no delay penalty. To further aid logic fit-

Node Feedbacks

Figure 2a. Registered Output, Combined Terms

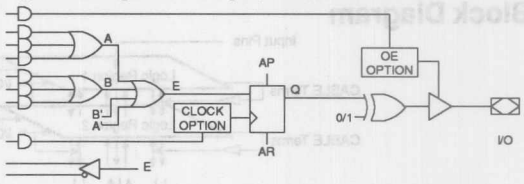


Figure 2b. Registered Output, Separate Terms

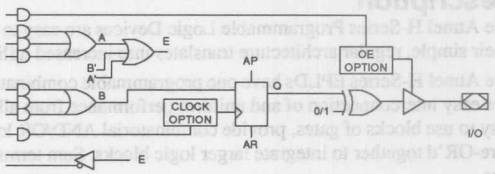


Figure 2c. Combinatorial Output, Combined Terms

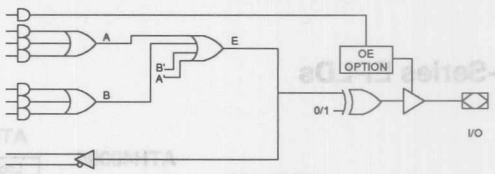
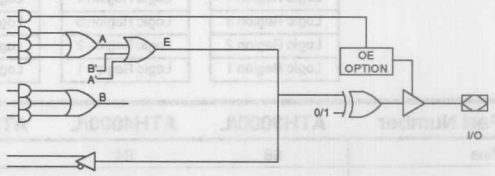


Figure 2d. Combinatorial Output, Separate Terms



ting, sum term joining also operates across region boundaries for two adjoining cells that lie in different regions.

The H-Series logic cell contains a single flip-flop which may be configured as D- or T-Type. Figures 2, 3 and 4 shows the logic cell's possible configurations. Modes are distinguished by output type (registered or combinatorial), feedback source (pin, register, or combinatorial node), and sum term configuration (combined or separate). Atmel's V-Series devices have featured two or three basic modes, whereas the H-Series breaks the logic cell down into smaller elements that may be utilized separately. This finer granularity allows higher gate utilization, while the reduced amount of interconnect guarantees high performance for all applications.

Register Feedbacks

Figure 3a. Register Output, Combined Terms

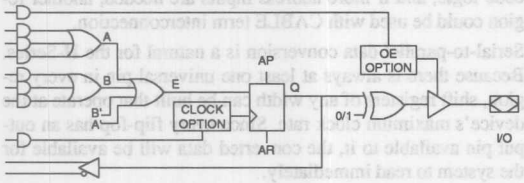


Figure 3b. Register Output, Separate Terms

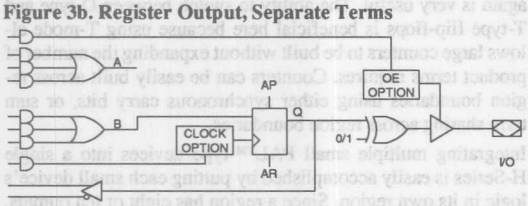


Figure 3c. Combinatorial Output, Combined Terms

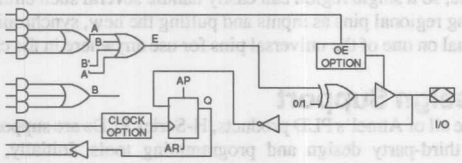
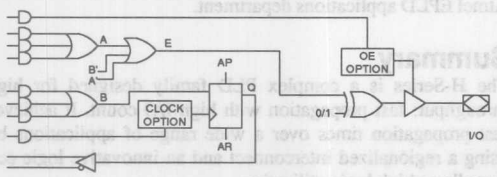


Figure 3d. Combinatorial Output, Separate Terms



Pin Feedbacks

Figure 4a. Register Output, Combined Terms

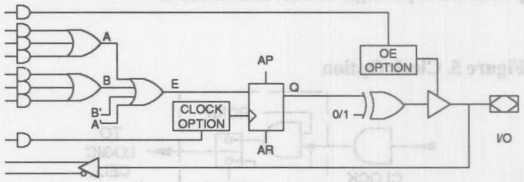


Figure 4b. Register Output, Separate Terms

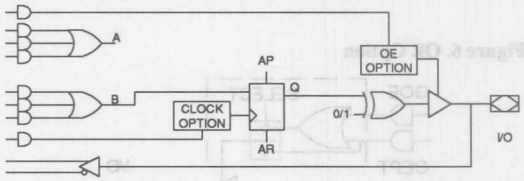


Figure 4c. Combinatorial Output, Combined Terms

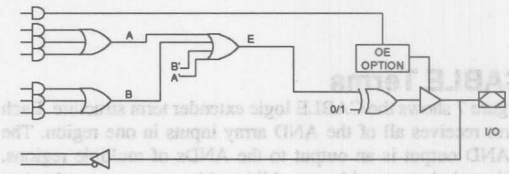
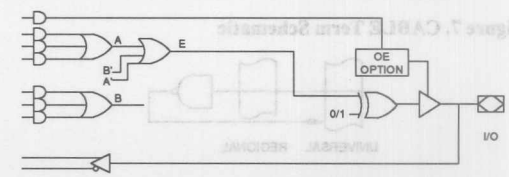


Figure 4d. Combinatorial Output, Separate Terms



The flip-flop clock option has three modes as shown in Figure 5, and is identical to the clock option used on the ATV5000. The clock product term controls asynchronous operation. A regional clock pin controls synchronous operation. Asynchronous clock gating is possible by ANDing the regional clock pin with the clock product term. As with the ATV5000, using the regional clock input pin results in faster clock-to-output delays than the product terms clock input.

The output enable function has three modes as shown in Figure 6. The output enable comes from the logic cell OE product term, a regional OE term, or an OR function of these. This last option realizes an AND/OR output enable control and uses only one product term per logic cell for this function.

Figure 5. Clock Option

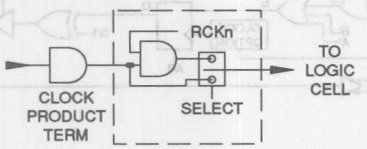
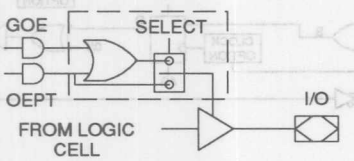


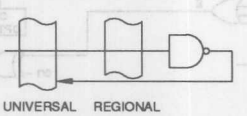
Figure 6. OE Option



CABLE Terms

Figure 7 shows the CABLE logic extender term structure. Each term receives all of the AND array inputs in one region. The NAND output is an output to the ANDs of multiple regions. This technique provides an additional interconnect mechanism between regions, allowing regional signals to be combined and fed onto the universal bus.

Figure 7. CABLE Term Schematic



Applications

The H-Series is ideal for applications requiring high speed and where most logic needs to be accessible to the rest of the system. Examples of such applications include:

- Decoders
- Serial-to-Parallel Data Conversion
- DMA Address Counters
- Integration of Multiple Small PLD Designs
- Signal Synchronization

Decoders are well-suited to the H-Series architecture, as they generally have a modest number of address inputs and a few control inputs. A single region can hold most normal bank decode logic, and if more address inputs are needed, another region could be used with CABLE term interconnection.

Serial-to-parallel data conversion is a natural for the H-Series. Because there is always at least one universal pin in every region, shift registers of any width can be built that operate at the device's maximum clock rate. Since every flip-fop has an output pin available to it, the converted data will be available for the system to read immediately.

DMA address counters also need their outputs available for use in the system, so the availability of I/O pins in H-Series devices again is very useful. The ability to switch between D-type and T-type flip-flops is beneficial here because using T-mode allows large counters to be built without expanding the number of product terms requires. Counters can be easily built across region boundaries using either synchronous carry bits, or sum term sharing across region boundaries.

Integrating multiple small PAL™-type devices into a single H-Series is easily accomplished by putting each small device's logic in its own region. Since a region has eight or ten outputs, a typical PAL™-type device will go into one or two regions (depending on how many input are signals are needed).

Signal synchronization uses a few flip-flops and some simple logic, so a single region can easily handle several such circuits, using regional pins as inputs and putting the new, synchronized signal on one of the universal pins for use anywhere in the chip.

Design Support

Like all of Atmel's PLD products, H-Series PLDs are supported by third-party design and programming tools. Initially, the H-Series devices have support from Data I/O (ABEL™ design software and programmers), and Viewlogic Systems (design software). Other vendors are developing support, and an up-to-date of tools that support the H-Series is available from the Atmel EPLD applications department.

Summary

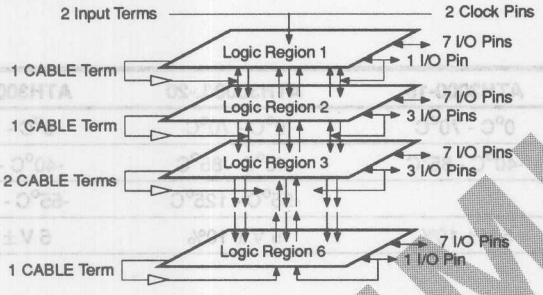
The H-Series is a complex PLD family designed for high throughput: fast propagation with high I/O count. It achieves fast propagation times over a wide range of applications by using a regionalized interconnect and an innovative logic cell that allows high logic utilization.

PAL™ and ABEL ™ may be registered trademarks of others.

Features

- High Through-Put Programmable Logic Device
- High Speed - 83.3 MHz System Clock Rate Operation
- Low Power - 0.5 mA Typical (ATH3000L)
- Flexible Interconnect Architecture - Universal Routing
- 56 Logic Cells - 56 Flip-Flops - 56 I/O Pins
- Multiple Flip-Flop Types - Synchronous or Asynchronous Registers
- Complete Third Party Software Support
  - No Placement, Routing or Layout Software Required
- Proven and Reliable High Speed CMOS EPROM Process
  - 2000 V ESD Protection
  - 200 mA Latchup Immunity
- Reprogrammable - Tested 100% for Programmability
- Commercial, Industrial and Military Temperature Grades

Block Diagram



Description

The Atmel ATH3000/L is an easy to use, high through-put programmable logic device. Its simple, regular architecture translates into increased utilization and high performance.

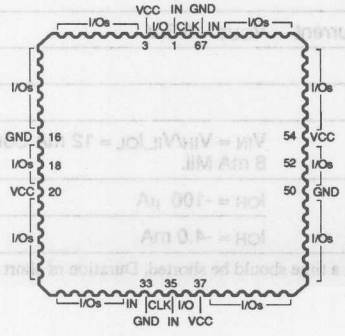
The Atmel ATH3000/L has one programmable combinatorial logic array. This guarantees easy interconnection of and uniform performance from all nodes. Sum terms, which are easy-to-use blocks of gates, provide combinatorial AND-OR logic blocks. Sum terms can be wire-OR'd together to integrate larger logic blocks. To expand the levels of logic, buried sum terms feed back into the logic array. A register or a sum term can drive each of the 56 I/O pins.

All 56 registers are configurable as D- or T-types without using extra logic gates. Individual sum terms and clocks give each flip-flop added flexibility. A direct "clock from pin" option guarantees synchronization and fast clock to output performance.

Standard off-the-shelf third party software tools and programmers support the ATH3000/L. This minimizes startup investment and improves product support.

Chip Carrier Pin Configuration

Pin Name	Function
IN	Logic Inputs
Clk	Register Clocks 1,2
I/O	Bidirectional Buffers
VCC	+5 V Supply



High Throughput UV Erasable Programmable Logic Device

Preliminary

7

PRELIMINARY

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V[1]
Voltage on Input Pins with Respect to Ground During Programming	-2.0 V to +14.0 V[1]
Programming Voltage with Respect to Ground	-2.0 V to +14.0 V[1]
Integrated UV Erase Dose	7258 W·sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC}+0.75 V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

D.C. and A.C. Operating Range

		ATH3000-15	ATH3000/L-20	ATH3000/L-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 10%	5 V ± 10%	5 V ± 10%

D.C. Characteristics

Symbol	Parameter	Condition		Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1 V to V_{CC}+1 V				10	µA
I_{LO}	Output Leakage Current	V_{OUT} =- 0.1 V to V_{CC}+0.1 V				10	µA
I_{CC}	Power Supply Current ATH3000	V_{CC} = MAX, V_{IN} = GND or V_{CC} Outputs Open	Com.		150	225	mA
			Ind.,Mil.		150	270	mA
I_{CC}	Power Supply Current ATH3000L	V_{CC} = MAX, V_{IN} = GND or V_{CC} Outputs Open	Com.		0.5	5	mA
			Ind.,Mil.		0.5	10	mA
I_{CC2}	Clocked Power Supply Current, ATH3000L Only	f = 1 MHz, V_{CC} = MAX Outputs Open	Com.		10	15	mA
			Ind.,Mil.		10	20	mA
I_{OS} [1]	Output Short Circuit Current	V_{OUT} = 0.5 V		-10		-90	mA
V_{IL}	Input Low Voltage			-0.6		0.8	V
V_{IH}	Input High Voltage			2.0		V_{CC}+0.75	V
V_{OL}	Output Low Voltage	V_{IN} = V_{IH}/V_{IL}, I_{OL} = 12 mA Com,Ind; 8 mA Mil.				0.5	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA		V_{CC}-0.3			V
		I_{OH} = -4.0 mA		2.4			V

Note: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 seconds.

Functional Logic Diagram Description

There are 56 identical Input/Ouput logic cells in the ATH3000. Each I/O cell has one flip-flop, six product terms divided into two sum terms, a clock term and one output enable term.

Each logic cell drives one signal (56 total) into the logic array. This signal can come from the pin, the flip-flop or the sum term. Each signal is either regional or universal.

The ATH3000/L has six regions. The Universal Bus routes signals to all six regions. It contains six Complement Array Buried Logic Extender (CABLE) terms, the true and false signals from ten universal I/O pins and the true and false signals from the two input-only pins. Regional buses route regional true and false signals.

Each I/O Logic Cell contains two sum terms, one flip-flop, a feedback buffer and an I/O buffer. Output enable and clock options have one product term each per I/O Cell.

The ATH3000/L has six CABLE terms. These terms provide wide-input NAND gate structures or universal routing.

Register preload simplifies testing. All registers automatically clear at power up.

ATH3000/L Block Diagram

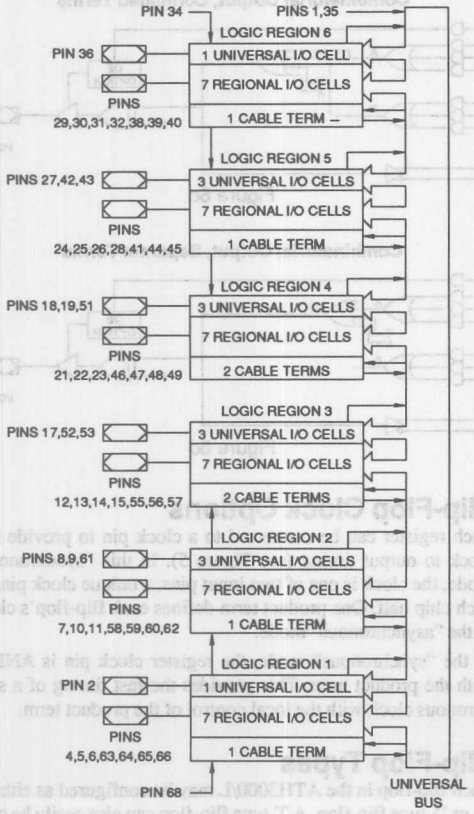


Figure 2

Functional Logic Diagram, ATH3000/L Logic Region

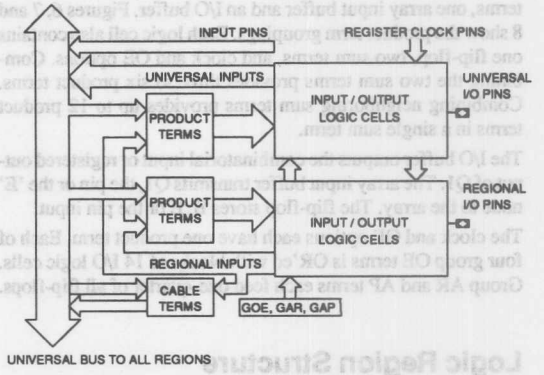


Figure 1

Logic Region Description

The ATH3000/L has six regions containing a total of 56 identical input/output logic cells (figure 2). The Universal Bus routes signals from ten universal I/O logic cells, Pins 1 and 35, and the CABLE terms. Regional buses route the remaining regional I/O logic cell signals.

CABLE Terms

CABLE terms in each ATH3000/L logic block provide a wide-input NAND function. This function is useful for logic expansion and for universal routing. CABLE terms route any signal or product of signals into the universal bus. Universal bus signals are available to every logic cell in the ATH3000/L.

CABLE terms provide two functions: 1) the ability to collect common logical expressions into one gate, and 2) the ability to route this signal to the entire chip. CABLE terms are useful for routing regional signals to the universal bus for use elsewhere.

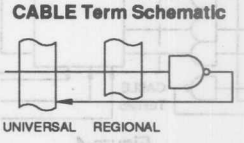


Figure 3

Group Resource Assignments

Regions I/O Pins	1,2,3 2-17	1,2,3 52-66	4,5,6 18-32	4,5,6 36-51
Register Clock Pin	68	68	34	34
Group OE Term	1	4	2	3
Group AR Term	1	4	2	3
Group AP Term	1	4	2	3

Logic Cell Options

The ATH3000/L logic cells contain most of the chip's logic options. The block diagram in figure 4 shows the eight product terms, one array input buffer and an I/O buffer. Figures 6, 7 and 8 show the product term groupings. Each logic cell also contains one flip-flop, two sum terms, and clock and OE options. Combining the two sum terms provides three to six product terms. Combining neighboring sum terms provides up to 12 product terms in a single sum term.

The I/O buffer outputs the combinatorial input or registered output of Q1. The array input buffer transmits Q1, the pin or the 'E' node to the array. The flip-flop stores B, E or the pin input.

The clock and OE options each have one product term. Each of four group OE terms is OR'ed with blocks of 14 I/O logic cells. Group AR and AP terms each feed one-quarter of all flip-flops.

Logic Region Structure

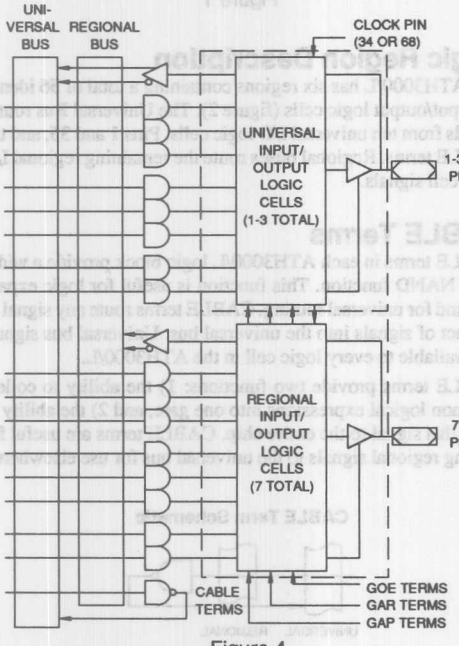


Figure 4

Clock Option

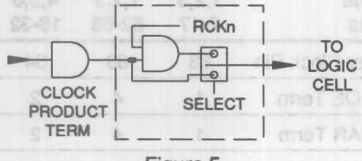


Figure 5

Node Feedbacks

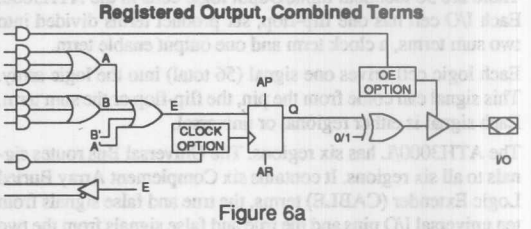


Figure 6a

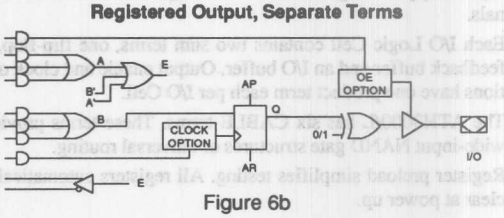


Figure 6b

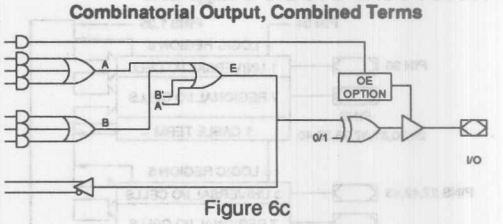


Figure 6c

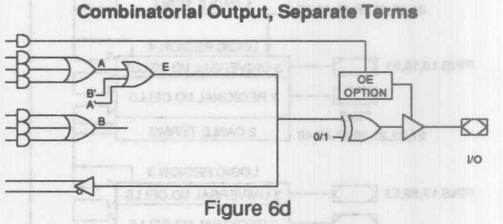


Figure 6d

Flip-Flop Clock Options

Each register can be connected to a clock pin to provide fast clock to output timing (see Figure 5). In this "synchronous" mode, the clock is one of two input pins, a unique clock pin for each chip half. One product term defines each flip-flop's clock in the "asynchronous" mode.

In the "synchronous" mode, the register clock pin is ANDed with the product term. This provides the fast timing of a synchronous clock with the local control of the product term.

Flip-Flop Types

Each flip-flop in the ATH3000/L may be configured as either a T- or D-type flip-flop. A T-type flip-flop can also easily be configured into a JK or SR flip-flop.

Register Feedbacks

Register Output, Combined Terms

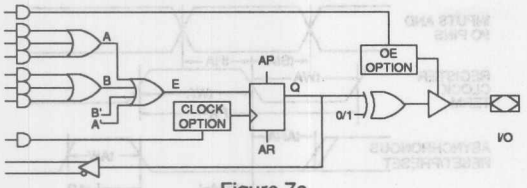


Figure 7a

Register Output, Separate Terms

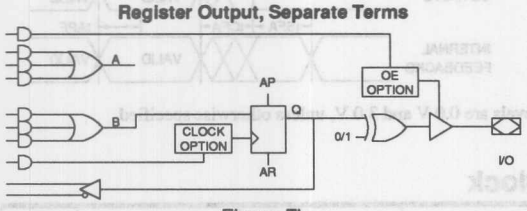


Figure 7b

Combinatorial Output, Combined Terms

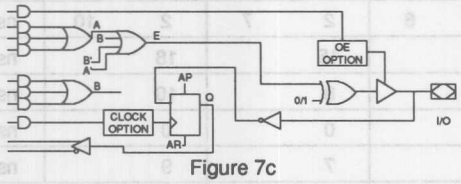


Figure 7c

Combinatorial Output, Separate Terms

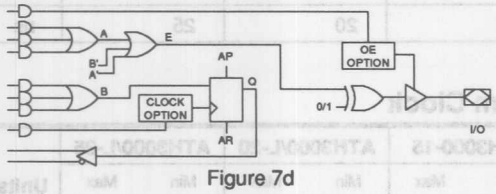


Figure 7d

Pin Feedbacks

Register Output, Combined Terms

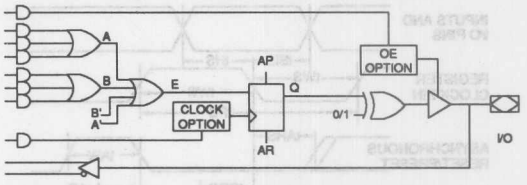


Figure 8a

Register Output, Separate Terms

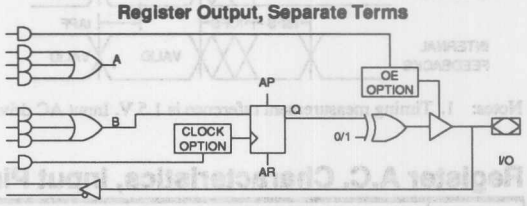


Figure 8b

Combinatorial Output, Combined Terms

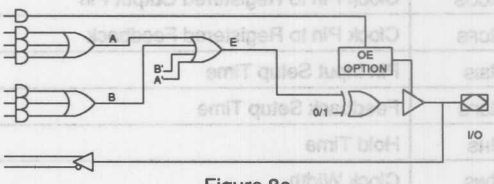


Figure 8c

Combinatorial Output, Separate Terms

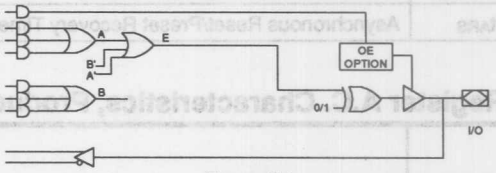


Figure 8d

Output Enable Options

Each output of the ATH3000/L functions as a bidirectional buffer. The OE option in each I/O logic cell controls the signal direction. In the default condition, the output driver is controlled by the product term in each I/O cell (OEPT). When selected, the output control is the logical OR of the product term and a product term from each quadrant of the chip (GOE). I/O pins 2-17 in regions 1, 2, and 3 use group OE term 1. I/O pins 52-66 in regions 1, 2, and 3 use group OE term 4. I/O pins 18-32 in regions 4, 5, and 6 use group OE term 2. I/O pins 36-51 in regions 4, 5, and 6 use group OE term 3.

OE Option

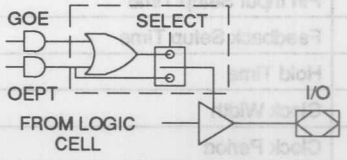
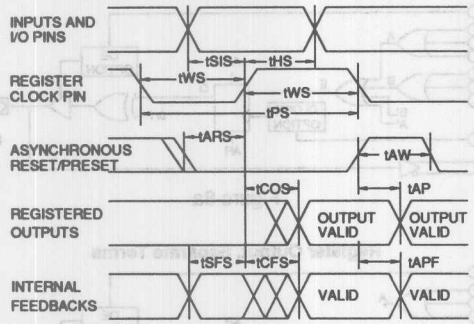
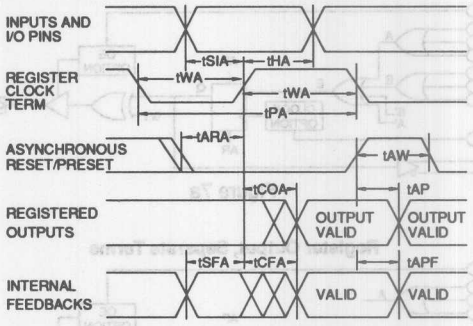


Figure 9

A.C. Waveforms [1] Input Pin Clock



A.C. Waveforms [1] Product Term Clock



Notes: 1. Timing measurement reference is 1.5 V. Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.

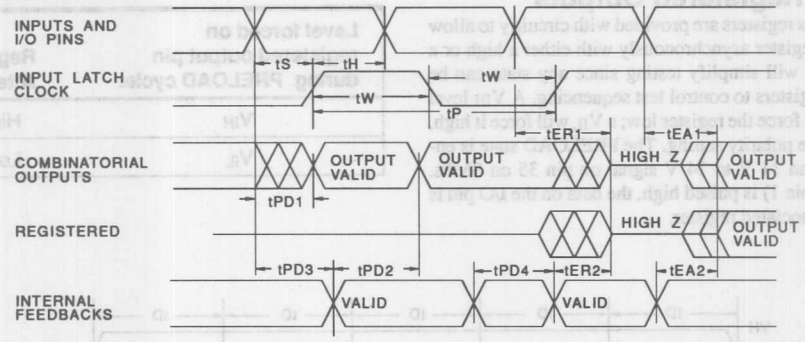
Register A.C. Characteristics, Input Pin Clock

Symbol	Parameter	ATH3000-15 Min	ATH3000-15 Max	ATH3000/L-20 Min	ATH3000/L-20 Max	ATH3000/L-25 Min	ATH3000/L-25 Max	Units
t_{COS}	Clock Pin to Registered Output Pin	4	12	4	15	4	20	ns
t_{CFS}	Clock Pin to Registered Feedback	2	6	2	7	2	10	ns
t_{SIS}	Pin Input Setup Time	12		15		18		ns
t_{SFS}	Feedback Setup Time	6		8		10		ns
t_{HS}	Hold Time	0		0		0		ns
t_{WS}	Clock Width	6		7		9		ns
t_{PS}	Clock Period	12		15		20		ns
F_{MAXS}	Maximum Frequency 1/(t_{CFS}+ t_{SFS})		83.3		66.7		50	MHz
t_{ARS}	Asynchronous Reset/Preset Recovery Time	15		20		25		ns

Register A.C. Characteristics, Product Term Clock

Symbol	Parameter	ATH3000-15 Min	ATH3000-15 Max	ATH3000/L-20 Min	ATH3000/L-20 Max	ATH3000/L-35 Min	ATH3000/L-35 Max	Units
t_{COA}	Clock Input to Registered Output Pin	5	15	5	20	5	25	ns
t_{CFA}	Clock Input to Registered Feedback	2	9	5	12	5	15	ns
t_{SIA}	Pin Input Setup Time	10		12		15		ns
t_{SFA}	Feedback Setup Time	5		6		10		ns
t_{HA}	Hold Time	2		5		5		ns
t_{WA}	Clock Width	7		9		12		ns
t_{PA}	Clock Period	14		18		25		ns
F_{MAXA}	Maximum Frequency 1/(t_{CFA}+ t_{SFA})		71		55		40	MHz
t_{ARA}	Asynchronous Reset/Preset Recovery Time	15		20		25		ns

A.C. Waveforms [1]

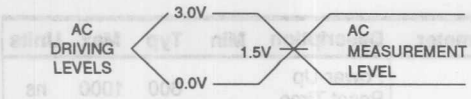


Notes: 1. Timing measurement reference is 1.5 V. Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.

A.C. Characteristics

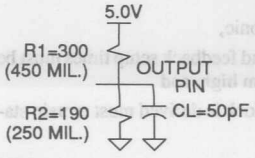
Symbol	Parameter	ATH3000-15 Min	ATH3000-15 Max	ATH3000/L-20 Min	ATH3000/L-20 Max	ATH3000/L-25 Min	ATH3000/L-25 Max	Units
t_{PD1}	Input to Non-Registered Output		15		20		25	ns
t_{PD2}	Feedback to Non-Registered Output		12		15		20	ns
t_{PD3}	Input to Non-Registered Feedback		12		15		20	ns
t_{PD4}	Feedback to Non-Registered Feedback		10		12		17	ns
t_{EA1}	Input to Output Enable		15		20		25	ns
t_{ER1}	Input to Output Disable		15		20		25	ns
t_{EA2}	Feedback to Output Enable		12		15		20	ns
t_{ER2}	Feedback to Output Disable		12		15		20	ns
t_S	Input Latch Setup Time	5		6		7		ns
t_H	Input Latch Hold Time	5		5		5		ns
t_W	Input Latch Clock Width	6		7		9		ns
t_P	Input Latch Clock Period	12		15		20		ns
F_{MAX}	Maximum Frequency ($1/t_P$)		83.3		66.7		50	MHz
t_{AW}	Asynchronous Reset/Preset Width	15		20		25		ns
t_{AP}	Asynchronous Reset/Preset to Registered Output		20		25		30	ns
t_{APF}	Asynchronous Reset/Preset to Registered Feedback		15		20		25	ns

Input Test Waveforms and Measurement Levels



t_R, t_F < 5 ns (10% to 90%)

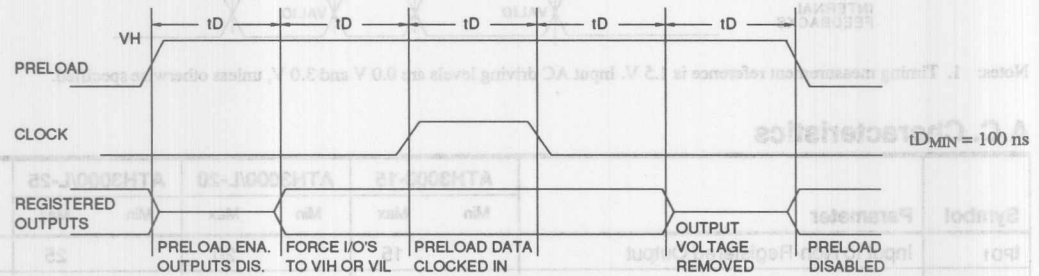
Output Test Load



Preload of Registered Outputs

The ATH3000/L's registers are provided with circuitry to allow loading of each register asynchronously with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A V_{IH} level on the I/O pin will force the register low; a V_{IL} will force it high, independent of the polarity setting. The PRELOAD state is entered by placing an 11 V to 14 V signal on pin 35 on SMPs. When the clock (pin 1) is pulsed high, the data on the I/O pin is placed into the associated register.

Level forced on registered output pin during PRELOAD cycle.	Register state After Cycle
V_{IH}	High
V_{IL}	Low



Operating Modes

	68 Lead LCC Pin							
Mode	1	2	36	34	68	35	Vcc (3,20,37,54)	I/Os
"EPLD"	X (1)	X	X	X	X	X	5V	I/O
Program	V_{PP}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	6V	ADD/D_{IN}
PGM Verify	V_{PP}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	X	6V	ADD/D_{OUT}
PGM Inhibit	V_{PP}	V_{IH}	V_{IH}	V_{IH}	V_{IH}	X	6V	High Z
Preload	⎍	X	X	X	X	V_H (2)	5V	D_{IN}

Notes: 1. X can be V_{IL} or V_{IH}. 2. V_H = 11.0 V to 14.0 V

Power Up Reset

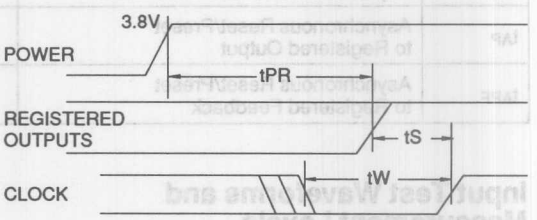
The registers in the ATH3000/L are designed to reset during power up. At a point delayed slightly from V_{CC} crossing 3.8 V, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1) The V_{CC} rise must be monotonic,

2) After reset occurs, all input and feedback setup times must be met before driving the clock term high, and

3) The signals from which the clock is derived must remain stable during t_{PR}.



Parameter	Description	Min	Typ	Max	Units
t_{PR}	Power-Up Reset Time		600	1000	ns

ATH3000 PLCC/PGA Pin Assignments

PLCC Pin #	PGA Pin #	Name	PLCC Pin #	PGA Pin #	Name	PLCC Pin #	PGA Pin #	Name	PLCC Pin #	PGA Pin #	Name
1	B6	IN	18	F2	I/O	35	K6	IN	52	F10	I/O
2	A6	I/O	19	F1	I/O	36	L6	I/O	53	F11	I/O
3	B5	VCC	20	G2	VCC	37	K7	VCC	54	E10	VCC
4	A5	I/O	21	G1	I/O	38	L7	I/O	55	E11	I/O
5	B4	I/O	22	H2	I/O	39	K8	I/O	56	D10	I/O
6	A4	I/O	23	H1	I/O	40	L8	I/O	57	D11	I/O
7	B3	I/O	24	J2	I/O	41	K9	I/O	58	C10	I/O
8	A3	I/O	25	J1	I/O	42	L9	I/O	59	C11	I/O
9	A2	I/O	26	K1	I/O	43	L10	I/O	60	B11	I/O
10	B2	I/O	27	K2	I/O	44	K10	I/O	61	B10	I/O
11	B1	I/O	28	L2	I/O	45	K11	I/O	62	A10	I/O
12	C2	I/O	29	K3	I/O	46	J10	I/O	63	B9	I/O
13	C1	I/O	30	L3	I/O	47	J11	I/O	64	A9	I/O
14	D2	I/O	31	K4	I/O	48	H10	I/O	65	B8	I/O
15	D1	I/O	32	L4	I/O	49	H11	I/O	66	A8	I/O
16	E2	GND	33	K5	GND	50	G10	GND	67	B7	GND
17	E1	I/O	34	L5	CLK	51	G11	I/O	68	A7	CLK

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	6	8	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATH3000/L fuse patterns. Once programmed, all outputs appear programmed during verify. The security fuse should be programmed last.

The security fuse inhibits Preload.

Erasure Characteristics

The entire memory array of an ATH3000/L is erased after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 μW/cm^2 intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 W·sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPLD which will be subjected to continuous fluorescent indoor lighting or sunlight.

Ordering Information

t_{PD} (ns)	t_{COS} (ns)	f_{MAXS} (MHz)	Ordering Code	Package	Operation Range
15	12	83.3	ATH3000-15JC ATH3000-15KC ATH3000-15UC	68J 68KW 68UW	Commercial (0°C to 70°C)
			ATH3000-15JI ATH3000-15KI ATH3000-15UI	68J 68KW 68UW	Industrial (-40°C to 85°C)
20	15	66.7	ATH3000-20JC ATH3000-20KC ATH3000-20UC	68J 68KW 68UW	Commercial (0°C to 70°C)
			ATH3000-20JI ATH3000-20KI ATH3000-20UI	68J 68KW 68UW	Industrial (-40°C to 85°C)
			ATH3000-20KM ATH3000-20UM	68KW 68UW	Military (-55°C to 125°C)
			ATH3000-20KM/883 ATH3000-20UM/883	68KW 68UW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
25	20	50	ATH3000-25JC ATH3000-25KC ATH3000-25UC	68J 68KW 68UW	Commercial (0°C to 70°C)
			ATH3000-25JI ATH3000-25KI ATH3000-25UI	68J 68KW 68UW	Industrial (-40°C to 85°C)
			ATH3000-25KM ATH3000-25UM	68KW 68UW	Military (-55°C to 125°C)
			ATH3000-25KM/883 ATH3000-25UM/883	68KW 68UW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
68J	68 Lead, Plastic J-Leaded Chip Carrier (PLCC)
68KW	68 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
68UW	68 Pin, Windowed, Ceramic Pin Grid Array (PGA)

Ordering Information

t_{PD} (ns)	t_{COS} (ns)	f_{MAXS} (MHz)	Ordering Code	Package	Operation Range
20	15	66.7	ATH3000L-20JC ATH3000L-20KC ATH3000L-20UC	68J 68KW 68UW	Commercial (0°C to 70°C)
			ATH3000L-20JI ATH3000L-20KI ATH3000L-20UI	68J 68KW 68UW	Industrial (-40°C to 85°C)
25	20	50	ATH3000L-25JC ATH3000L-25KC ATH3000L-25UC	68J 68KW 68UW	Commercial (0°C to 70°C)
			ATH3000L-25JI ATH3000L-25KI ATH3000L-25UI	68J 68KW 68UW	Industrial (-40°C to 85°C)
			ATH3000L-25KM ATH3000L-25UM	68KW 68UW	Military (-55°C to 125°C)

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Package Type	
68J	68 Lead, Plastic J-Leaded Chip Carrier (PLCC)
68KW	68 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
68UW	68 Pin, Windowed, Ceramic Pin Grid Array (PGA)

EPLD Software Tools Overview

Atmel's philosophy is that you should be able to use standard tools you already have to design with our programmable logic devices. For those users that do not currently have such a tool, or who wish to augment tools they already own, we have Atmel-specific versions of standard tools available at very reasonable costs.

With the tools Atmel has available, we can serve the needs of beginning users as well as more experienced users. Based on the background of the user, we can make recommendations on the most cost effective solution (see Table 1). If you have any questions regarding which package is best suited to a particular set of needs, please contact the Atmel EPLD Technical Support Hotline at (408) 436-4333.

General

Atmel offers versions of standard third-party PLD design tools that are limited to only Atmel EPLD devices at a reduced cost compared to the normal versions. These systems are based on software licensed from Data I/O Corporation and Viewlogic Systems, Inc.

Under the terms of our agreements with Data I/O and Viewlogic Systems, Atmel may sell these systems and their options only to users of these limited systems. If a customer already has the full function version from Data I/O and/or Viewlogic Systems, they can purchase upgrades or options from the original company, not from Atmel.

This document outlines general system configurations required to use the various systems, details each package including ordering information, and includes a section with suggested systems for various types of users.

Required System Configurations

At the present time, all of the EPLD systems described are available only on PC386/486 platforms running DOS with the system requirements indicated in Table 2. Contact the Atmel EPLD Hotline at (408) 436-4333 for further information on system configurations

Systems

Atmel offers several levels of systems to meet the various needs of our customers. The systems are described on the following pages, along with a brief description of their function. For further information, contact your local Atmel sales representative or the Atmel EPLD Hotline at (408) 436-4333.

Table 1. Software System Recommendations

User	Experience	Recommended System
New PLD User	No prior PLD experience. Wants basic support for devices like ATV750 and ATV2500 and is willing to do manual pin assignment.	Atmel-ABEL-4
Atmel-ABEL-4.0 User	Knows Atmel parts, wants to use the ATV5000/ ATV5100 and wants to use automatic fitting.	Atmel-FIT5000 Upgrade
PAL-type Device User	Knows ABEL, CUPL, or PALASM, and is familiar with 22V10 design. Wants to move up in density, and wants automatic fitting to reduce need to learn detailed internals of each device.	Atmel-ABEL V-Series Kit
	If user wants H-Series automatic fitting as well...	V-Series/H-Series Kit
Complex EPLD User or TTL Designer	Uses complex PLDs from Altera or AMD. Wants state-of-the-art tools for Atmel's V- and H-Series to take advantage of their speed and density. Wants schematic capture, simulation, and multiple design entry modes.	Atmel-ViewPLD (includes one year of maintenance)
FPGA User	Uses FPGAs from Xilinx, Actel, or others with Viewlogic CAE tools for schematic capture and simulation. Wants to add capability for Atmel's V- and H-Series to take advantage of their speed and density for control and timing applications.	Atmel-ViewPLD Intermediate Upgrade

Note: 1. For proper ordering codes, consult the Atmel EPLD Software Tools Product Description List

Table 2. EPLD System Configuration Requirements

	Atmel-ABEL [1]	Atmel-ViewPLD
Platform:	PC386/486	PC386/486
Operating System:	DOS 3.0 or greater	DOS 3.0 or greater
Display Adaptor:	CGA, EGA, Hercules, VGA or SVGA	EGA, Hercules, VGA, or SVGA
System Memory:	4 Mbytes total	6 Mbytes total min. 12 Mbytes total recommended
Hard Disk: Space required: Disk Size Recommended:	5 Mbytes 40 Mbytes min.	26 Mbytes 80 Mbytes min.
I/O Ports required:	1 parallel	1 parallel 1 serial (for mouse)
Mouse:	not required	Mouse systems or compatible

Note: 1. Atmel-ABEL can be run on 8086 and 80286 systems but it must be installed in "standard" mode. Atmel-ABEL "standard" mode does not support any of Atmel's high density devices such as ATV5000, ATV51000 and the H-Series family.

EPLD Software Tools Product Description List

Atmel-ABEL-4
Ordering Code: ATABEL-4

Basic ABEL support for Atmel V-Series and H-Series devices. Does not include any automatic device fitters, which are optional and priced separately or available in packages called Atmel-ABEL Kits. Current users of Atmel-ABEL-4.0 do not get an automatic upgrade to this version, however a reduced cost upgrade is available when purchased together with the ATV5000 device fitter (see below).

A user purchasing this package now will receive basic ATH3000 support and additional H-Series device support as each device is released.

Atmel-FIT2500
Ordering Code: ATFIT2500-4

Automatic ATV750/ATV2500 device fitter for Atmel-ABEL-4. Requires Atmel-ABEL version 4.2 or greateer in order to run.

Atmel-ABEL V5000 Fitter
Ordering Code: ATFIT5000

Automatic ATV5000/ATV5100 device fitter for Atmel-ABEL-4. Requires Atmel-ABEL version 4.2 or greater in order to run. Current Atmel-ABEL-4.0 users may purchase this fitter together with an upgrade to Atmel-ABEL-4 for $100 additional (see Atmel-ABEL V5000 Fitter Upgrade).

Atmel-ABEL V5000 Fitter Upgrade
Ordering Code: ATFIT5000-UP

Package consisting of FIT5000 fitter plus an upgrade from Atmel-ABEL version 4.0 to Atmel-ABEL-4. The user is required to return their original Atmel-ABEL version 4.0 master disks to the Atmel EPLD marketing department to be eligible for the upgrade.

Atmel-ABEL H-Series Fitter
Ordering Code: (Contact Factory)

Automatic device fitter for Atmel-ABEL-4. Requires Atmel-ABEL version 4.2 or greater in order to run.

Atmel-ABEL V-Series Kit
Ordering Code: ATABEL-KITV

A package consisting of Atmel-ABEL-4 together with fitters for the ATV750/ATV2500, and ATV5000/ATV5100. A complete development package for the V-Series with fitters, that offers a savings to the user over the components purchased separately.

Atmel-ABEL V-Series/H-Series Kit
Ordering Code: ATABEL-KITVH

A package consisting of Atmel-ABEL-4 together with fitters for the ATV750/ATV2500, and ATV5000/ATV5100, and H-Series. A complete package with all fitters, that offers a savings to a user over the components purchased separately. If a user purchases this package now, they will receive the H-Series fitter as soon as it is available.

Atmel-ABEL to ViewPLD Upgrade
Ordering Code: ATABEL2VIEW

Upgrade package to upgrade an Atmel-ABEL-4 user to an Atmel-ViewPLD system. A user must have purchased Atmel-ABEL-4 and all three fitters (or an Atmel-ABEL Kit) in order to purchase this upgrade.

Atmel-ViewPLD
Ordering Code: ATVIEWPLD-4

A complete stand-alone ViewPLD system with all ABEL functions plus Viewlogic schematic capture, simulation (unit delay and timing) as well as modeling and partitioning functions plus utilities. Includes all fitters. Price includes one year of maintenance/updates. Maintenance is optional after the first year.

A user purchasing this package now will receive basic ATH3000 support and additional H-Series device support as each device is released and the H-Series fitter as soon as it is available.

Atmel-ViewPLD Maintenance
Ordering Code: ATVIEWPLD-MAINT

One year of updates and maintenance for the ViewPLD software. Maintenance for one year is included with the purchase of Atmel-ViewPLD, and it is optional after the first year. Maintenance is not required for the purchase of an Atmel-ViewPLD Intermediate Upgrade, but is available if the user wishes to purchase their updates from Atmel.

Atmel-ViewPLD Intermediate Upgrade
Ordering Code: ATVIEWPLD-INT

A ViewPLD system sold as an add-on for users with an existing vendor-specific (SDA) Viewlogic seat. Examples of SDA seats are Viewlogic front-end systems sold by Xilinx and Actel for use with their place-and-route tools. Adds Atmel EPLDs to the system. Includes all Atmel-ABEL files and fitters plus access to the appropriate Viewlogic libraries. May not be sold to a user with a full Viewlogic seat purchased from Viewlogic. Those users must purchase ViewPLD directly from Viewlogic.

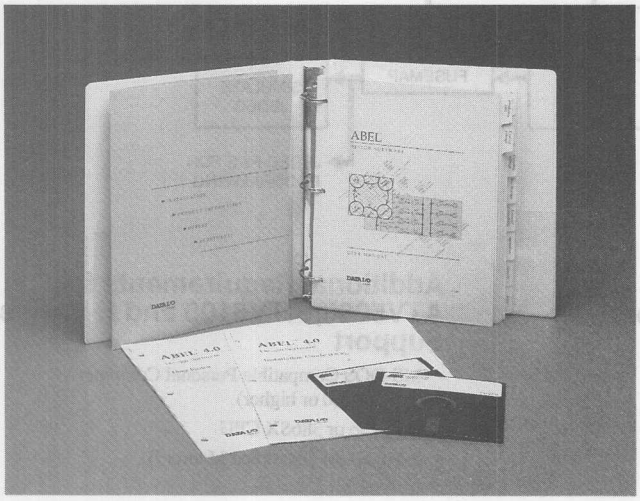
A user purchasing this package now will receive basic ATH3000 support and additional H-Series device support as each device is released and the H-Series fitter as soon as it is available.

Ordering Information

Ordering Code	Description
ATABEL-4	High-Level Design Tool for Atmel Programmable Logic Devices: ATV750, ATV2500, ATV5000, ATV5100, and H-Series
ATABEL-KITV	Atmel-ABEL-4 Kit with V-Series Fitters
ATABEL-KITVH	Atmel-ABEL-4 with V-Series and H-Series Fitters
ATABEL-2VIEW	Atmel-ABEL-4 to Atmel-ViewPLD Upgrade Kit (requires previous purchase of Atmel-ABEL 4.2 and all fitters before purchasing upgrade kit)
ATFIT2500-4	Atmel-ABE-4 Custom Logic Fitter for ATV750 and ATV2500
ATFIT5000-4	Atmel-ABEL-4 Custom Logic Fitter for ATV5000 and ATV5100
ATFIT5000-UP	FIT5000 Package Together with Upgrade from Atmel-ABEL 4.02 to Latest Version
C/F	Atmel-ABEL-4 Custom Logic Fitter for Atmel H-Series Devices
ATVIEWPLD-4	Atmel-ViewPLD-4 Stand-Alone System (Includes One Year Maintenance)
ATVIEWPLD-INT	Atmel-ViewPLD-4 Intermediate Upgrade
ATVIEWPLD-MAINT	Atmel-ViewPLD Maintenance (One Year)

Features

- **Atmel-ABEL-4 Uses the Industry-Standard ABEL Hardware Description Language**
- **Multiple Input Methods :**
  - **Boolean Equations, Truth Tables and State Diagrams**
  - **Optional Schematic Entry Available**
- **Automatic Logic Reduction, Simulation, Error Checking, and Generation of Design Documentation**
- **Optional Device Fitters Peform Automatic Pin/Node Assignment and Logic Syntheseis**
- **Automatically Takes Advantage of Atmel's EPLD Architecture, Joining Sum Terms When Extra Product Terms are Needed**
- **Runs on MS-DOS™ Compatible Personal Computers**
- **This Inexpensive Package Includes:**
  - **Atmel-ABEL-4 Software which Supports ATV750, ATV2500, ATV5000, ATV5100, and H-Series**
  - **Complete ABEL Manual**
  - **Logic Diagrams for ATV750, ATV2500, ATV5000, ATV5100, and H-Series**
  - **Design Examples**
  - **Special Offers and Coupons**



High-Level Design Tool for Atmel Programmable Logic Devices:

ATV750

ATV2500

ATV5000

ATV5100

H-Series

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Description

Atmel Programmable Logic Devices (PLDs) offer powerful solutions for logic design. Atmel-ABEL-4, developed by Data I/O Corporation, is a software package specifically designed to support development with Atmel Programmable Logic Devices.

Atmel-ABEL-4 offers all of the function and features of Data I/O's standard ABEL-4 software package while supporting Atmel's high-density PLDs: the ATV750, ATV2500, ATV5000, ATV5100 and H-Series devices. Support for other manufacturer's PLDs is not provided.

Atmel-ABEL-4 automatically takes advantage of Atmel's innovative multiple sum term PLD architecture. When your reduced equations require more product terms than anticipated, the software automatically allocates the next available block of product terms to your equation.

Continued on next page

Desciption (Continued)

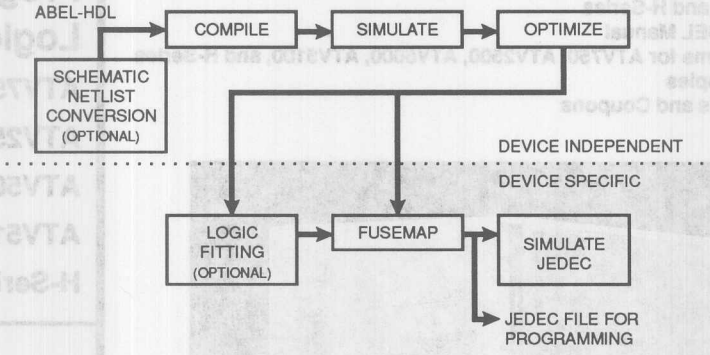
Atmel-ABEL-4 automatically reduces your logic equations to near minimal form. Depending on your requirements, you can choose among several reduction algorithms. The result is a more efficient, cost-effective design.

Behavioral simulation is an integral part of the Atmel-ABEL-4 design package. Simulation may be performed on either the design equations as entered, or after device selection, pin and node assignment, and option selection. This way you can verify that the completed design matches your design input.

Atmel-ABEL-4 uses the Open ABEL format which allows the use of optional logic fitters. These logic fitters perform automatic device pin and node assignment and macrocell option selection to make maximum use of device resources, speeding up the design process.

Once your design is ready, Atmel-ABEL-4 generates standard JEDEC files which can be downloaded to your programmer with the terminal emulation software included with the package.

Design Flow Diagram



Requirements for ATV750 and ATV2500 Support

- MS-DOS Compatible Personal Computer (version 3.0 or higher)
- 5 1/4" High Density Floppy Disk Drive (low density disks available on request)
- 640K RAM

Additional Requirements for ATV5000, ATV5100 and H-Series Support

- MS-DOS Compatible Personal Computer (version 3.0 or higher)
- 486, 386 or 386SX CPU
- 2 MB RAM (Extended Memory)

Ordering Information

Ordering Code	Description
ATABEL-4	High-Level Design Tool for Atmel Programmable Logic Devices: ATV750, ATV2500, ATV5000, ATV5100 and H-Series
ATABEL-KITV	Atmel-ABEL-4 Kit with V-Series Fitters
ATABEL-KITVH	Atmel-ABEL-4 with V-Series and H-Series Fitters

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Atmel-ABEL-4 Custom Logic Fitter:

ATV750

ATV2500

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Features

- **Works with Atmel-ABEL-4 PLD Design System**
- **Allows Device-Independent Design**
- **Optimizes Resource Utilization**
- **Assigns Signals to Pins and Nodes**
- **Utilizes Atmel's Unique Product Term Joining/Sharing**
- **Performs Logic Synthesis**

Description

ATFIT2500 is a custom logic fitter for Data I/O's ABEL-4 PLD design system which supports both the ATV750 and the ATV2500 PLDs. FIT2500 was written by Data I/O with Atmel's cooperation and approval. This fitter will work with Atmel-ABEL-4, the special version of ABEL-4 available from Atmel which supports only the ATV750, ATV2500, ATV5000, ATV5100 and H-Series complex PLDs.

The fitter performs pin/node signal assignment, performs macrocell option selection, takes advantage of Atmel's shared product term architecture where possible, and maximizes resource utilization. This allows a user to do device-independent design and still get maximum utilization for Atmel's ATV750 and ATV2500 PLD without needing to know all internal details of the device.

Pin/node assignments may be made by the user, assigned by the fitter, or a combination of both. Optionally, all pin/node assignments can be ignored and the fitter will attempt to fit the design into the target device automatically.

Requirements

- ATFIT2500 requires Atmel-ABEL version 4.2 or higher running under MS-DOS, version 3.00 or higher, with extended memory support (2 Mbyte minimum).

Ordering Information

Ordering Code	Description
ATFIT2500-4	Atmel-ABEL-4 Custom Logic Fitter for ATV750 and ATV2500

ABEL™ and MS-DOS™ may be trademarks of others.

Atmel-ABEL-4
Custom
Logic Fitter:
ATV750
ATV2500

Features

- Works with Atmel-ABEL-4 PLD Design System
- Allows Device-Independent Design
- Optimizes Resource Utilization
- Assigns Signals to Pins and Nodes
- Utilizes Atmel's Unique Product Term Sharing Structure
- Performs Logic Synthesis

Description

ATF1T2500 is a custom logic fitter for Data I/O's ABEL-4 PLD design system which supports both the ATV750 and the ATV2500 PLDs. FIT2500 was written by Data I/O with Atmel's cooperation and approval. This fitter will work with Atmel-ABEL-4, the special version of ABEL-4 available from Atmel which supports only the ATV750, ATV2500, ATV5000, ATV5100 and H-Series complex PLDs.

The fitter performs pin/node signal assignment, performs macrocell option selection, takes advantage of Atmel's shared product term architecture where possible, and maximizes resource utilization. This allows a user to do device-independent design and still get maximum utilization for Atmel's ATV750 and ATV2500 PLD without needing to know all internal details of the device.

Pin/node assignments may be made by the user, assigned by the fitter, or a combination of both. Optionally, all pin/node assignments can be ignored and the fitter will attempt to fit the design into the target device automatically.

Requirements

- ATF1T2500 requires Atmel-ABEL version 4.2 or higher running under MS-DOS, version 3.00 or higher, with extended memory support (2 Mbyte minimum).

Ordering Information

Ordering Code	Description
ATF1T2500-4	Atmel-ABEL-4 Custom Logic Fitter for ATV750 and ATV2500

ABEL™ and MS-DOS™ may be trademarks of others.

Atmel-ABEL-4 Custom Logic Fitter: ATV5000, ATV5100

Features

- **Works with Atmel-ABEL-4 PLD Design System**
- **Allows Device-Independent Design**
- **Optimizes Resource Utilization**
- **Assigns Signals to Pins and Nodes**
- **Utilizes Atmel's Unique Product Term Joining/Sharing**
- **Performs Logic Synthesis**

Description

ATFIT5000 is a custom logic fitter for Data I/O's ABEL-4 PLD design system which supports both the ATV5000 and the ATV5100 PLDs. FIT5000 was written by Data I/O with Atmel's cooperation and approval. This fitter will work with Atmel-ABEL-4, the special version of ABEL-4 available from Atmel which supports only the ATV750, ATV2500, ATV5000, ATV5100 and H-Series complex PLDs.

The fitter performs pin/node signal assignment, performs macrocell option selection, takes advantage of Atmel's shared product term architecture where possible, and maximizes resource utilization. This allows a user to do device-independent design and still get maximum utilization for Atmel's ATV5000/ATV5100 PLDs without needing to know all internal details of the devices.

Pin/node assignments may be made by the user, assigned by the fitter, or a combination of both. Optionally, all pin/node assignments can be ignored and the fitter will attempt to fit the design into the target device automatically.

Requirements

- ATFIT5000 requires Atmel-ABEL version 4.2 or higher running under MS-DOS, version 3.00 or higher, with extended memory support (2 Mbyte minimum).

Ordering Information

Ordering Code	Description
ATFIT5000-4	Atmel-ABEL-4 Custom Logic Fitter for ATV5000, ATV5100
ATFIT5000-UP	FIT5000 Package Together with Upgrade from Atmel-ABEL 4.02 to Latest Version

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Atmel-ABEL-4 Custom Logic Fitter: ATV5000, ATV5100

Features

- Works with Atmel-ABEL-4 PLD Design System
- Allows Device-Independent Design
- Optimizes Resource Utilization
- Assigns Signals to Pins and Nodes
- Utilizes Atmel's Unique Product Term Joining/Sharing
- Performs Logic Synthesis

Description

ATF/T5000 is a custom logic fitter for Data I/O's ABEL-4 PLD design system which supports both the ATV5000 and the ATV5100 PLDs. F/T5000 was written by Data I/O with Atmel's cooperation and approval. This fitter will work with Atmel-ABEL-4, the special version of ABEL-4 available from Atmel which supports only the ATV750, ATV2500, ATV5000, ATV5100 and II-Series complex PLDs.

The fitter performs pinNode signal assignment, performs maxcocll option selection, takes advantage of Atmel's shared product term architecture where possible, and maximizes resource utilization. This allows a user to do device-independent design and still get maximum utilization for Atmel's ATV5000/ATV5100 PLDs without needing to know all internal details of the devices.

PinNode assignments may be made by the user, assigned by the fitter, or a combination of both. Optionally, all pinNode assignments can be ignored and the fitter will attempt to fit the design into the target device automatically.

Requirements

- ATF/T5000 requires Atmel-ABEL version 4.2 or higher running under MS-DOS, version 3.00 or higher, with extended memory support (2 Mbyte minimum).

Ordering Information

Ordering Code	Description
ATF/T5000-4	Atmel-ABEL-4 Custom Logic Fitter for ATV5000, ATV5100
ATF/T5000-UP	F/T5000 Package Together with Upgrade from Atmel-ABEL 4.02 to Latest Version

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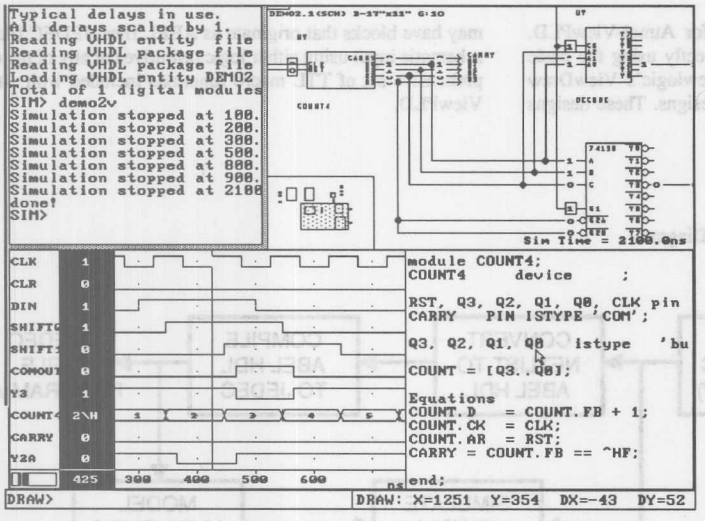
Reduce your time to market with the fastest, easiest to use, most complete set of tools for programmable logic design available: Atmel-ViewPLD. This fully integrated system supports Atmel's V-Series and H-Series of complex PLDs.

Benefits

- **Allows design specification with schematic entry or the ABEL hardware description language and accepts existing designs with JEDEC files and TTL logic in any arbitrary design hierarchy.**
- **Allows the retargeting of older designs into new technologies, and new functions can be easily merged and enhanced.**
- **Utilizes intelligent device fitters for automatic logic synthesis and device resource assignment.**
- **Saves design iterations by generating accurate full VHDL timing models for simulating and debugging PLD designs in the system context.**
- **Optimizes designs requiring multiple devices with automatic user-guided partitioning and device fitting.**

Integrated Programmable Logic Design System

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Atmel-ViewPLD is a Complete Set of Tools for Programmable Logic Design

Through a partnership with Data I/O and Viewlogic Systems, Atmel has developed Atmel-ViewPLD, bringing together the best programmable device knowledge and fitting capabilities with the best engineering environment for schematic entry and verification. Atmel-ViewPLD is a complete set of tools for PLD design which will get you from concept to finished product faster than you ever thought possible. Atmel-ViewPLD contains every tool you will ever need, from schematic entry and device fitting to automatic partitioning — even waveform analysis and full timing simulation.

Atmel-ViewPLD is available either as an add-on product to users with other vendor-specific Viewlogic front-end systems (intermediate upgrade), or as a stand-alone product offering unmatched capabilities and value in PLD design.

ViewPLD Works From Multiple Input Formats/Sources

All of Atmel-ViewPLD's capabilities operate from a design database which is created from several sources which can be freely intermixed. The ABEL language can be used to easily specify Boolean operations, truth tables, and state machines. Schematics can be created using basic logic functions or TTL macro functions, and existing PLD designs in JEDEC format can be used as well. Once the design database is created, Atmel-ViewPLD can automatically produce a schematic of the design for use in system schematics for functional simulation before any implementation is started.

Comprehensive Device Support

Atmel-ViewPLD offers complete support for Atmel's two families of high density PLDs, the V-Series and the H-Series. The V-Series, designed for high density timing and control applications, includes the ATV750/L, ATV2500H/L, ATV5000/L and ATV5100/L. The H-Series, designed for high speed interface and decoding applications, includes the ATH3000/L, ATH4000/L, ATH4500/L, and ATH5500/L. Atmel-ViewPLD automatically produces optimized JEDEC files for each PLD created with are ready to be downloaded to device programmers.

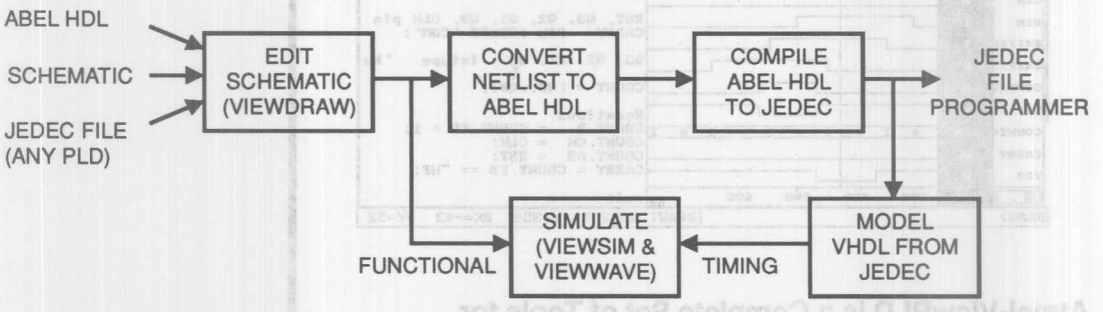
Although JEDEC file generation and timing modeling is limited to the Atmel devices, JEDEC file design input into the design database is accepted for any PLD device supported by ABEL, including all PAL and GAL devices.

Atmel-ViewPLD includes device fitters for all supported devices. These fitters, developed by Data I/O with Atmel's support and cooperation, perform logic synthesis and device resource assignment automatically, allowing efficient designs to be created with minimum effort.

Design Flow

Figure 1 shows the basic design flow for Atmel-ViewPLD. ABEL source files can be processed directly using the basic technology supplied by Data I/O, or Viewlogic's ViewDraw tool may be used to enter hierarchical designs. These designs may have blocks that originate as ABEL files, JEDEC files, or schematic input using either logic primitives or any of the comprehensive set of TTL macro functions included with Atmel-ViewPLD.

Figure 1. Atmel-ViewPLD Design Flow Diagram



Atmel-ViewPLD Offers Interactive Partitioning

The design database can be automatically partitioned into multiple PLDs. Using ViewDraw, Viewlogic's schematic capture tool, constraints are specified graphically, such as device pin sizes, signal grouping, and register and pin spares.

After partitioning, schematic symbols are automatically created for the devices and the partitioned schematic is automatically drawn. This can then be used to add additional constraints and iterate the partitioning process. Once partitioning is completed, each partition is then "fitted" into the best device as controlled by the designer.

VHDL Models Automatically Generated

Once the design has been fitted into the PLD(s), Atmel-ViewPLD generates simulation models for each PLD in VHDL for design verification. These models can be used with the automatically generated schematic interconnecting the PLD(s) to perform full timing simulation at the system level using ViewSim and ViewWave, Viewlogic's full function simulator and graphic waveform analyzer. ViewSim and ViewWave are included as a part of Atmel-ViewPLD.

Functional VHDL models can also be produced for use in migrating a design to ASIC technology using the optional ViewSynthesis and ViewRetargeter tools.

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Ordering Information

Ordering Code	Description
ATVIEWPLD-4	Atmel-ViewPLD-4 Stand-Alone System (Includes One Year Maintenance)
ATVIEWPLD-INT	Atmel-ViewPLD-4 Intermediate Upgrade
ATVIEWPLD-MAINT	Atmel-ViewPLD Maintenance (One Year)
ATABEL-2VIEW	Atmel-ABEL-4 to Atmel-ViewPLD Upgrade Kit (requires previous purchase of Atmel-ABEL-4 and all fitters before purchasing upgrade kit)

ABEL and ViewPLD may be trademarks of others.

Software Support Information

Software	Software Versions				
	AT22V10	ATV750	ATV2500	ATV5000	ATV5100
Data I/O ABEL™	1.3,2.0,3.0	3.0	3.2	4.02	4.3
Logical Devices CUPL™	2.0	2.15b	3.2A	4.3	
ISDATA LOG/iC	2.3	3.0	3.4(1)		
Atmel-ABEL™		1.01	1.01	4.02	4.3
ViewPLD Atmel-ViewPLD		4.2	4.2	4.2	
ViewLogic WorkView 4.1.2 ViewPLD	1.2	1.2	1.2	1.2	
Minc PLDesigner	1.5	3.0(1,2)	3.0(1,2)		

Notes: 1. Qualification in progress during printing of data book. Please call Atmel EPLD Hotline at (408) 436-4333 for updated information.
2. Supported in Minc PLDesigner - XL product only.

Programming Software Companies

ACCEL Technologies, Inc.
6825 Flanders Drive
San Diego, CA 92121
(800) 433-7801

Data I/O Corporation (ABEL™)
10525 Willows Rd. N.E.
P.O. Box 97046
Redmond, WA 98073-9746
(206) 881-6444
(800) 247-5700

ISDATA Gmbh (LOG/IC)
Haid-und-Neu- Str. 7
D-7500 Karlsruhe 1
West Germany
0721 / 69309
US:(510) 531-8553

Logical Devices (CUPL™)
692 S. Military Trail
Deerfield Beach, Florida 33442
(305) 428-6868

Minc, Inc.
6755 Earl Drive
Colorado Springs, CO 80918
(719) 590-1155

Viewlogic Systems, Inc.
293 Boston Road West
Marlboro, MA 01752
(508) 480-0881

New Programmer Support Information

Company	Model	Programmer Versions							
		AT22V10	AT22LV10 AT22LV10L	AT22V10B	ATV750	ATV2500	ATV5000	ATV5100	ATH3000
Advin Systems	Sailor-PAL	9.72			9.71				
	Pilot-U40	10.05			10.05	10.05			
	Piolt-U84	10.05			10.05	10.05	10.32(1)		
BP Microsystems	PLD1100	1.11			1.85				
	PLD1100 (at 15 ns)	1.54							
CEIBO	MP-51(1)	1.07			1.07	1.07	1.07	1.07	
Data I/O	Unisite 48	1.7	4.0	4.1	2.2	2.45	3.4	3.9	3.9
	29B	04			04				
	DIP Module 303A011A	13			05				
	PLCC Module	06			06				
	60A	11							
	3900	1.4	1.5	1.6	1.3	1.4	1.4	1.4	1.4
	2900	1.0	2.0	2.2	1.0	1.4			
Inlab/ProLogic	28A(2)	10.03g			10.03g				
Logical Devices	AllPro40	1.49C			1.48C	1.49C			
	AllPro88	2.00D			2.00D	2.00D			
Microprоss	ROM 3000U	3.48			3.48				
Owen	AP-II	1.73A							
PistoHI	PET100	PP61			PP61	PP62			
SMS	Sprint Plus	3.2H			3.2H				
	Sprint Expert	3.2K			3.2J3	3.2J3			
Stag	ZL30A	30A26			30A30				
System General	SGUP-85	2.1			3.1				
	TURPRO-1	1.22			1.22	1.22	1.60(1)		

Notes: 1. No vectors.

2. Versions 12.0 through 13.01 don't work for ATV750.

Programming Hardware Companies

Advin Systems, Inc.
1050-L East Duane Ave.
Sunnyvale, CA 94086
(408) 243-7000

BP Microsystems
10681 Haddington #190
Houston, TX 77043
(713) 461-9430

CEIBO
Merkazim Building
1 Maskit St.
P.O. Box 2106
Herzelia 46120
Israel
(972) 52-555387
US: (617) 863-9927

Data I/O Corporation
10525 Willows Rd. N.E.
P.O. Box 97046
Redmond, WA 98073-9746
(206) 881-6444
(800) 247-5700

Elan Digital Systems Ltd.
Elan House
Little Park Farm Road
Segensworth West
Fareham, Hants
U.K. PO15-5SJ
(0489) 579799

Inlab / ProLogic
2150 IW 6th Ave
Broomfield, CO 80020
(800) 237-6759

Logical Devices
1201 N.W. 65 Place
Ft. Lauderdale, FL 33309
(305) 974-0967
(800) 331-7766

Microprogs
5 Rue Denis Papin
59650 Villeneuve D'Ascq
France
(011) 33204-79040

Owen
Ringstr. 11
Postfach 1104
D-6798 Kusel
Germany
(011) 49-6381-5085

SMS SPRINT International
PO Box 3159
Redmond, WA 98052-3159
US: (206) 883-8447

Stag Microsystems
1600 Wyatt Dr.
Santa Clara, CA 95054
(408) 988-1118

System General
510 S. Park Victoria Drive
Milipitas, CA 95035
(408) 263-6667
Tiawan: (886) 2-9173005

Using Programmable Logic Devices

Introduction

This application note covers three areas:

- Where and *why* do I use Programmable Logic Devices (*PLDs*)?
- *How* do I use PLDs?
- Software and hardware *support* for Atmel PLDs.

Where Do I Use PLDs?

Any digital logic design can be done using PLDs. If you normally begin your design by:

- Using AND and OR functions
- Thinking of 7400 series components
- Using truth tables, or
- State diagrams

you are already on the path to using PLDs.

Designing a microprocessor based system, with memory and I/O? How about all that "glue" logic you use to interface with the bus, provide chip selects, and any unusual signals required by special chips? Most of these functions are currently done with 7400 series TTL. *How about using a PLD instead?*

Designing a stand-alone PC board which uses a state machine to control multiple output signals? Using latches to synchronize signals? Using counters to divide down master clock frequencies? Converting parallel-to-serial and back again? All of these functions fit easily in modern PLDs. *Most anything found in your TTL Databook can be replaced with your own, PERSONALIZED, programmable logic device.*

PLD Applications

- **Glue Logic**
- **State Machines**
- **Synchronization**
- **Decoders**
- **Counters**
- **Bus Interfaces**
- **Parallel-to-Serial**
- **Serial-to-Parallel**
- **Subsystems**
- **and Many Others**

Why PLDs?

Maybe you have already heard all the wonderful reasons for using PLDs. Well, they're true! First, let's review some of the more important ones:

- **Increased Integration.** You can reduce the package count of your designs while simultaneously increasing the features offered by your product.
- **Lower Power.** CMOS and fewer packages combine to reduce power consumption.
- **Improved Reliability.** Lower power plus fewer interconnections and packages translate into greatly improved system reliability.
- **Lower Cost.** PLDs reduce inventory costs, too.
- **Easier To Use!** Yes, believe it or not, once you get past the initial learning period, PLDs are easier to use than discrete logic functions.
- **Easier to Change.** Oops! Need to make a change? You won't need "blue wire" when you use a PLD— all changes are internal, and can be done quickly. ECNs are a snap— and system reliability is maintained!

Let's Get Started!

Figure 1 describes the PLD design process. After having read the first part of this application note, you now have the perfect application for a PLD, right? So here you go!

How do you translate your idea into a working prototype? *First, you need a computer with an editor of some kind.* If you have a workstation with a schematic editor, you may input your design using familiar logic blocks. Otherwise, a line or full screen text editor, used in the non-document mode will do. An example of an ABEL™ text file is on the next page.

Next, turn the **logic compiler** loose on your design. First it will *check for typographical errors* and any inconsistencies in your specification. Most compilers then attempt to *reduce your logic* using standard logic reduction theory. Then, a **simulator** will check the test vectors you input, comparing your logic description against the predicted responses. This is an excellent way to verify your design. Check with the appropriate software manuals for more information.

At the end of the compilation process, a *JEDEC* file is output. This file is a standard format accepted by most programming hardware. Next *download this file* to your chosen programmer.

At this point you are ready to "build" your **prototype**. Make sure the programmer has the correct information to program the device you have chosen (an Atmel PLD, of course), plug in your device, and go! Most programmers will even functionally test your prototype for you if you include test vectors in your JEDEC file.

Take your configured PLD, and *plug it into your system.* If you find any errors, just use your editor to make the necessary changes, and repeat the process. It's easy!

Example Design

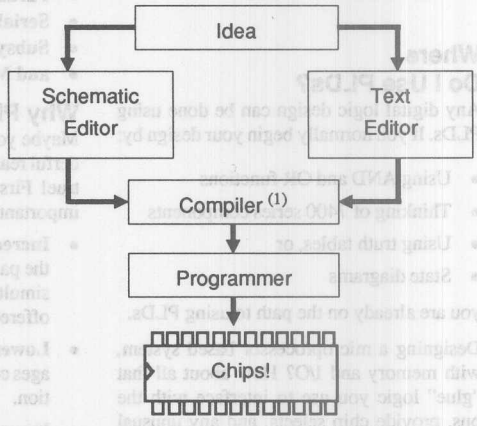
The following design is a simple example using ABEL™ to process the logic description file and an AT22V10 as the target device. The equations are on the next page, and are a direct reproduction of the actual ABEL input file.

Each of the three allowable input formats are shown. A truth table is used to describe a simple 2-to-4 decoder, as is often used to decode chip selects in a microprocessor system. Next, the state machine format is used to describe a divide-by-4 counter. And finally, Boolean equations are used to describe some random logic.

Note the test vectors used to test the device. The "c" nomenclature means that this pin has a low to high to low series of transitions for this vector. Each time this happens, the counter should increment. Also note that the counter starts in the reset condition, which is both outputs "1" for an active low output.

Now you're ready to go - Have fun!

Figure 1. PLD Design Process



Note: 1. Examples of compilers are ABEL™, CUPL™, and LOG/iC. Each of these products contains modules which allow simulation of your design. They also minimize your logic equations, which gives you flexibility in describing your design.

Example ABEL™ Description File

```
module X3 flag'-r3';
title 'Example using 22V10 - KHG 1/6/88';
X310 device 'P22V10';
"
Clk,A12,A13     pin    1,2,3;
CE0,CE1,CE2,CE3 pin    20,21,22,23;
Q1,Q2,CarOut    pin    17,18,14;
CarEn,A,B,C,D   pin    6,7,8,9,10;
Out1,Out2       pin    15,16;
"
X,Z,c     =  .X. , .Z. , .C.;
"
"Counter States
State1    =  ^b00;     State2    =  ^b01;
State3    =  ^b10;     State4    =  ^b11;
"
"The following truth table defines the 2 to 4 decoder, which decodes
"  A13 and A12 into CE0, CE1, CE2, and CE3.
truth_table ([A13,A12] -> [CE0,CE1,CE2,CE3])
[ 0, 0 ]  ->  [ 0, 1, 1, 1 ];
[ 0, 1 ]  ->  [ 1, 0, 1, 1 ];
[ 1, 0 ]  ->  [ 1, 1, 0, 1 ];
[ 1, 1 ]  ->  [ 1, 1, 1, 0 ];
"The following state description defines the divide by 4 counter
state_diagram [Q2,Q1]
State State1:   GOTO   State2;
State State2:   GOTO   State3;
State State3:   GOTO   State4;
State State4:   GOTO   State1;
"  The following equations are general in nature to illustrate Boolean input
"  format.  The CarOut equation uses state 4 above to produce a carry.
Equations
CarOut=  Q2  &  Q1  &  CarEn;     "& = AND
Out1   =  A &  B +  C &  D;   "+ = OR, AND takes precedence
Out2   =  A &  C +  B &  D;
"The following are the appropriate test vectors
test_vectors
"
([Clk, CarEn, A13,A12, A, B, C, D]- > [CE0,CE1,CE2,CE3,Q2,Q1,CarOut,Out1,Out2]);
[ 0, 0, 0, 0, 0, 0, 0, 0 ] - > [ 0, 1, 1, 1, 1, 1, 0, 0, 0 ];
[ c, 0, 0, 1, 1, 1, 0, 0 ] - > [ 1, 0, 1, 1, 0, 0, 0, 1, 0 ];
[ c, 0, 1, 0, 1, 0, 1, 0 ] - > [ 1, 1, 0, 1, 0, 1, 0, 0, 1 ];
[ c, 0, 1, 1, 0, 0, 1, 1 ] - > [ 1, 1, 1, 0, 1, 0, 0, 1, 0 ];
[ c, 0, 0, 0, 0, 1, 0, 1 ] - > [ 0, 1, 1, 1, 1, 1, 0, 0, 1 ];
[ 0, 1, 0, 1, 1, 1, 1, 1 ] - > [ 1, 0, 1, 1, 1, 1, 1, 1, 1 ];

end X3;
```



Example ABEL™ Description File

```
module X3 flag 'x3';
title 'Example using 22V10 - RHD 1/e/88';
X310 device 'P22V10';
"
Clk,A12,A13     pin   1,2,3;
CE0,CE1,CE2,CE3 pin   20,21,22,23;
Q1,Q2,CarOut    pin   17,18,14;
CarIn,A,B,C,D   pin   6,7,8,9,10;
Out1,Out2       pin   15,16;
"
X,Z,C =  .X. , .Z. , .C.;
"
"Counter States
State1  = ^b00;   State2  = ^b01;
State3  = ^b10;   State4  = ^b11;
"
"The following truth table defines the 2 to 4 decoder, which decodes
"  A12 and A13 into CE0, CE1, CE2, and CE3.
truth_table ([A13,A12] -> [CE0,CE1,CE2,CE3])
[ 0, 0 ] -> [ 0, 1, 1, 1 ];
[ 0, 1 ] -> [ 1, 0, 1, 1 ];
[ 1, 0 ] -> [ 1, 1, 0, 1 ];
[ 1, 1 ] -> [ 1, 1, 1, 0 ];
"The following state description defines the divide by 4 counter
state_diagram [Q2,Q1]
State State1:  GOTO  State2;
State State2:  GOTO  State3;
State State3:  GOTO  State4;
State State4:  GOTO  State1;
"  The following equations are general in nature to illustrate Boolean input
"  format.  The CarOut equation uses state 4 above to produce a carry.
Equations
CarOut= Q2 & Q1 & CarIn;    "& = AND
Out1  = A & B + C & D;  "+ = OR, AND takes precedence
Out2  = A & C + B & D;
"The following are the appropriate test vectors
test_vectors
"
([Clk, CarIn, A13,A12, A, B, C, D]- > [CE0,CE1,CE2,CE3,Q2,Q1,CarOut,Out1,Out2]);
[ 0, 0, 0, 0, 0, 0, 0, 0 ] - > [ 0, 1, 1, 1, 1, 1, 1, 0, 0, 0 ];
[ c, 0, 0, 1, 1, 0, 0, 0 ] - > [ 1, 0, 1, 1, 1, 0, 0, 1, 0, 0 ];
[ c, 0, 1, 0, 1, 0, 0, 0 ] - > [ 1, 1, 0, 1, 1, 0, 0, 1, 0, 0 ];
[ c, 0, 1, 1, 0, 0, 1, 1 ] - > [ 1, 1, 1, 0, 1, 1, 0, 0, 1, 1 ];
[ c, 0, 0, 0, 0, 1, 0, 1 ] - > [ 0, 1, 1, 1, 1, 1, 0, 0, 1, 1 ];
[ 0, 1, 0, 1, 1, 1, 1 ] - > [ 1, 0, 1, 1, 1, 1, 1, 1, 1, 1 ];

end X3;
```

Selecting Decoupling Capacitors For Atmel's EPLDs

Introduction

This application note provides a summary of information needed when selecting decoupling capacitors for Atmel Programmable Logic Devices. A 0.22-µF, multi-layer ceramic or plastic dielectric capacitor is recommended for such use. Either surface-mount (SMD) or radial-leaded devices should be used. Because of their high parasitic resistance and/or inductance, tantalum, aluminum electrolytic, and axially leaded capacitors are not recommended.

When is a Capacitor Not a Capacitor

Unfortunately, capacitors are not the perfect charge storage devices we would like them to be. Their lead wires and internal construction create parasitic resistance and inductance in series with the capacitance. These parasitics are usually referred to as ESR (equivalent series resistance) and ESL (equivalent series inductance), respectively. As will be shown, these parasitics can seriously reduce the ability of many types of capacitors to decouple supply noise in high-speed systems. Table 1 gives typical ESR and ESL values for various types of capacitors.

As shown, ESR values range from 0.01 ohm to as high as 9 ohms. ESL varies from 2 nH for typical surface mount devices to 20 nH for electrolytic capacitors. These numbers are typical values, taken from data from several manufacturers. As expected, there is some variation between manufacturers. Also, worst case specification values will be significantly higher, especially for ESR values.

How ESR and ESL can Affect High Speed Operation

The effects of these parasitics may be best illustrated by a simple example. Consider the case of a 22V10L. In the standby mode, Icc current is typically only 5 mA. When an input switches, Icc may temporarily go as high as 100 mA. This increase in current draws charge from the local decoupling capacitor. This capacitor current will create voltage drops across the ESR and ESL parasitic elements. To see how these voltage drops can cause problems in a system, look at a typical decoupling application.

In this example the design goal of the capacitor is to keep local supply noise below 0.2 volts, a reasonable expectation. This immediately sets an upper limit on ESR of 2 ohms.

$ESR_{max} = V_{noise} / I_{max}$

Imax= Highest Expected Capacitor Current

The upper limit on ESL is determined by how quickly the capacitor's current must change, as well as how much supply noise will be tolerated during that change. For high-speed logic devices, Icc must be able to switch from standby to active levels within 2 to 3 nanoseconds.

$ESL_{max} = V_{noise} \cdot I_{max} / \Delta t;$

Δt = Time allowed for capacitor current to switch

In this example, an upper limit on ESL of 4 to 6 nH is set.

Consider what can happen if these limits are exceeded. If an axially leaded multi-layer ceramic capacitor with ESR of 0.15 ohm is used, the resistance drop in our application

will not be significant (100 mA X .15 Ohm = 15 mV). However, the inductance will not allow the current to reach 100 mA in 6 nanoseconds. This can slow the logic device switching by several nanoseconds.

What Types to Use: Multi-layered Ceramic and Plastic Dielectrics

From this example, it is apparent that the parasitic elements on capacitors can easily limit their decoupling ability. Therefore, users of high-speed logic need to pick their capacitors with care. The data in Table 1 shows that the best bets are surface-mount, multi-layered ceramic (MLC) or plastic dielectrics. Of the leaded devices, only radial types are recommended.

Within the MLCs, there are different classes of dielectric. Class I has the best characteristics, but its small dielectric constant makes it impractical for decoupling values. Class II is highly recommended, as it has good temperature stability (percent variation -55°C to 125°C) and aging characteristics (10 percent in ten years). Class III, on the other hand, drops to less than 50 percent of its rated capacitance at 85°C, and to only 25 percent at -55°C. Class III dielectric also loses 20 percent of its rated value in ten years. Therefore, Class III MLCs are only recommended for applications where temperature excursions are minimal.

Plastic dielectric capacitors in general offer performance as good as Class II MLCs. Among the dielectrics available today are polypropylene, polyester, polycarbonate, polystyrene and teflon. Capacitance variation with temperature depends on the particular material, but is generally less than ±20 percent from -55°C to 125°C. Aging is minimal, usually less than 2 percent in 10 years. Unfortunately, not many manufacturers make surface-mount plastic dielectric capacitors. That should change soon, as surface-mount technology advances and becomes more common.

When using radial leaded cases, be sure to minimize lead lengths, as ESL increases quickly with longer leads. For example, if a capacitor has 6 nH of inductance with 2 mm leads, extending leads to 5 mm will increase ESL to 10 nH.

What Types Not to Use: Aluminum Electrolytic, Tantalum, and Anything Axial

The design example above together with the numbers given in Table 1 show that some types are not suitable at all for decoupling high-speed devices. Specifically, the high inductance of axially leaded capacitors puts them on the "don't use" list. Also, tantalum and aluminum electrolytic devices are generally not recommended, as they have high ESR and/or ESL, even in radial and surface-mount configurations.

In Any Case, Know Your ESL and ESR

ESR data is often found in catalogs. However, this will normally be only low-frequency data, and ESR is frequency dependent (dropping at higher f). ESL data is not usually given in catalogs. The best thing to do is get Z versus frequency data from the manufacturer. From such a graph (with frequency up to at least 10 MHz), you can extract high frequency ESR and ESL.

How Much Capacitance Do You Need

For decoupling Atmel's EPLDs a 0.22-µF capacitor is recommended. In many cases, this will be overkill. However, determining how much less you could get by with for a particular application is dependent upon several factors. The number of PC board supply planes, the board's dielectric thickness and dielectric constant, the value (*and* ESR *and* ESL!) of power entry decoupling capacitors, among other things, will determine just how much is really needed. The best bet is to use a good 0.22-µF and be safe. Besides, the more decoupling is taken care of by local capacitors, the lower the board's HF emissions will be.

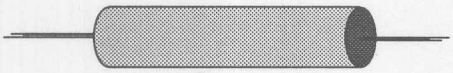
Summary

Choosing the right decoupling capacitor is an important part of high-speed circuit design. Choosing the wrong one can introduce supply noise that can slow down signal switching or even end up giving incorrect data. For decoupling Atmel EPLDs, 0.22-µF capacitors are recommended. These should be of either multi-layer ceramic or plastic dielectric type. Surface-mount devices are best, with radial leaded cases also being acceptable.

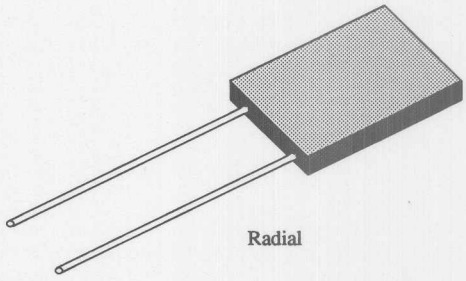
Table 1. Capacitor Types and Recommendation Ratings

Dielectric	Body	L (nH,typ)	R (ohm,typ)	Rating	Comments
Ceramic II	SMD	2	.02	E	Highly recommended
	Radial	6	.07	G	Keep leads short
	Axial	12	.07	S	Axial always = Higher L
Ceramic III	SMD	2	.04	G	C loss hot/cold/old
	Radial	6	.15+	S	
	Axial	12	.15+	X	
Plastics	SMD	2	.03	E	Hard to find
	Radial	5+	.01+	G	Get R and L data
	Axial	12+	.01+	X	
Aluminum Electrolytic	SMD	13	9.0	X	Forget it
	Radial	15+	1.5+	X	
	Axial	20	1.5	X	
Tantalum	SMD	?	3.0	X	
	Radial	10+	1.0	X	
	Axial	15+	1.0	X	

Ratings code:
E Excellent; highly recommended
G Good; will perform well in most applications
S Satisfactory; be aware of specific vendor's device performance
X Not recommended



Axial



Radial



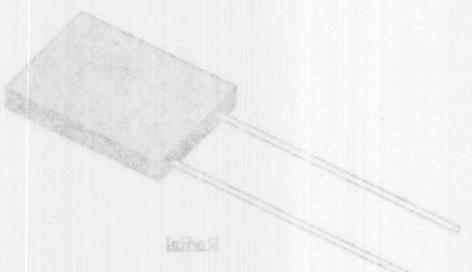
SMD

Table 1. Capacitor Types and Recommendation Ratings

Dielectric	Body	L (nH,typ)	R (ohm,typ)	Rating	Comments
Ceramic II	SMD	2	.02	E	Highly recommended
	Radial	6	.07	G	Keep leads short
	Axial	12	.07	S	Axial always = Higher L
Ceramic III	SMD	2	.04	G	C loses hot/cold/old
	Radial	8	.15+	S	
	Axial	12	.15+	X	
Plastics	SMD	2	.03	E	Hard to find
	Radial	8+	.01+	G	Get R and L data
	Axial	12+	.01+	X	
Aluminum Electrolytic	SMD	13	9.0	X	Forget it
	Radial	15+	1.5+	X	
	Axial	20	1.5	X	
Tantalum	SMD	7	5.0	X	
	Radial	10+	1.0	X	
	Axial	15+	1.0	X	

Ratings code:

E Excellent; highly recommended
G Good; will perform well in most applications
S Satisfactory; be aware of specific vendor's device performance
X Not recommended



Radial



Axial



SMD

Using a Programmable Logic Device As a System Controller In an I/O Bus Based System [1]

Summary

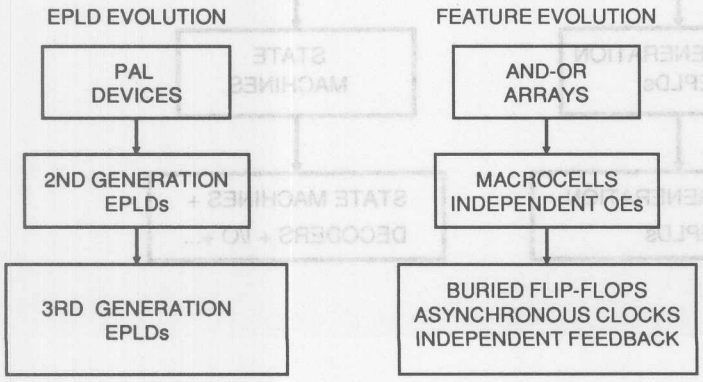
As Programmable Logic Devices (PLDs) become more complex, the amount of logic that can be placed in one device is rapidly increasing. Complete controllers and subsystems now fit into one or two PLDs. As a result, the PLD may now be connected directly to the system bus as an independent peripheral. First generation PAL® devices are difficult to use in these applications. However, recent innovations in PLD architecture enable them to be easily designed into bus-based systems.

PLD Evolution

The driving force behind PLD usage has been to integrate as much of the Small Scale Integration (SSI) logic on a packed PC board as possible. The first level of integration was made possible by the invention of the PAL device. First generation products were usually in 20-pin packages with a typical device having nine dedicated inputs and eight dedicated outputs. One input pin was a dedicated output enable, and one pin a dedicated, common clock for up to eight flip-flops. Making one of these devices work on an I/O bus was difficult and typically was used as little more than a simple latch.

In the mid-eighties, second generation devices appeared. These PLDs are generally in 24 or more pins, have independent output enable controls and *output macrocells*. The macrocells allow the designer to configure each output independently as registered or combinatorial. However, there are still too few registers in these devices to allow the design of complex state machines. Also, these circuits lack independent feedback paths, which further reduce the usable number of registers. This also complicates the use of the output pins as true I/O structures.

Note: 1. This article originally appeared in Northcon '86
®PAL is the registered trademark of Monolithic Memories



UV Erasable Programmable Logic Device

Application Note

7

Recently several third generation devices (such as the Atmel ATV750) have appeared. These devices are differentiated by the following features:

- **Extra Registers**

Up to twice the usual number. The ATV750 has 20 flip-flops.

- **Independent Feedbacks**

Feedback paths for the registers are independent of the output configuration. In addition, there are separate input paths from the I/O pads.

- **Asynchronous Clocks**

Product terms for each flip-flop's clock allows the designer to break up the registers into different functional blocks.

Control function outputs that have no other use than to manage the other resources inside the PLD need not be brought outside the device, allowing implementation of complex state machines internally.

As PLDs have evolved, so have the applications for them. Initially, PLDs could only integrate a few SSI functions. A typical application was a special-purpose decoder or encoder. With the introduction of more flip-flops, Medium Scale Integration (MSI) functions such as state machines could be designed. Third generation devices are the first true Large Scale Integration (LSI) devices, and are capable of integrating several of the previous generation devices into one package. Now state machines can be combined with an output decoder to control peripheral functions, and still have adequate resources to interface directly to the microprocessor.

System Application

The following example is an application of the Atmel ATV750 as a peripheral resource controller. The design required a state machine, a bus interface unit and a peripheral control interface. All ten outputs of the ATV750 are used, most in the combinatorial mode. However, the 17 required flip-flops were still available to latch the address and data buses, provide a status register, and a two-bit counter. This design would require three second generation, 24-pin PLDs, or five first generation 20-pin devices and at least two other discrete devices. In all, more than 80 percent of the ATV750 is utilized. The number of gates alone integrated into the ATV750 in this application is more than other 24-pin PLD's have to offer.

- **The System**

The system described is a peripheral controller/bus interface for connecting a special-purpose, custom encryption / exponentiation chip to an 80186 microprocessor (Figure 1). The custom chip has a serial interface, and only one bi-directional pin to indicate its "busy" status. All chip functions are controlled with a set of single-purpose input pins. While simple, this interface is not directly compatible with a modern microprocessor, such as the 80186. The PLD system described not only combines the required glue logic, but also off-loads the parallel-to-serial conversion from the processor. This application note will only touch on the salient features of the design, and why a third generation device is so useful.

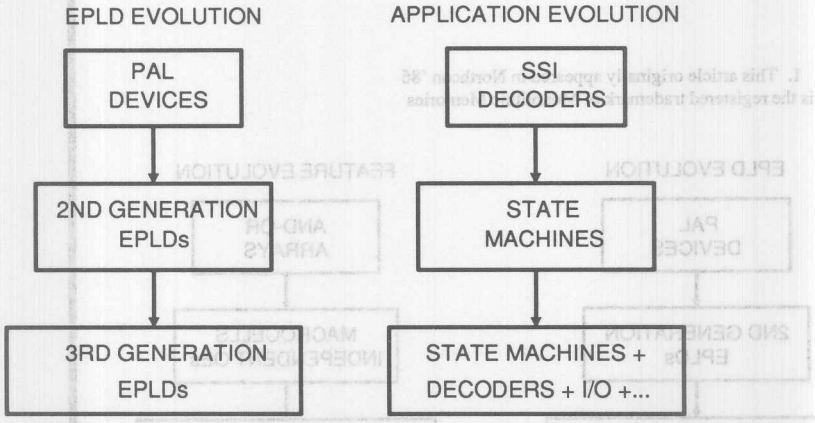
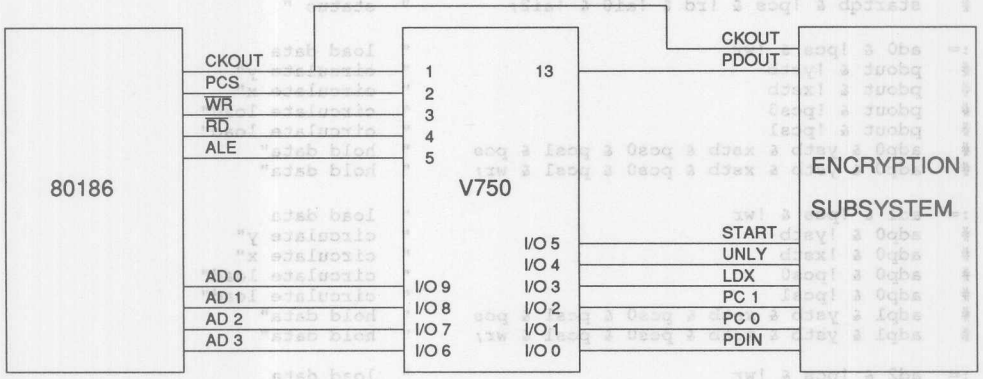


Figure 1. System Diagram



• The Microprocessor Bus

The 80186 uses a multiplexed address and data bus. Several control signals, such as ALE, $\overline{RD}$ and $\overline{WR}$ tell the system when to get what type of data from the bus. The 80186 also has some internally decoded chip selects, and one is used here for convenience. The system clock is an 8-MHz signal, which is appropriate for the encryption chip and well within this PLD's timing specification. The lower four bits of the address are latched into the PLD to define the upcoming operation, which then allows the PLD to output the requested data in one read cycle of the microprocessor. These address bits are decoded to define the instruction to be executed by the PLD subsystem.

• Tackling the I/O Bus

Using first and second generation PLDs, the equations for the I/O bus interface are shown in Figure 2. These equations consume twelve sum terms, eight flip-flops, and twelve output pins. Since this requires two PLDs, another ten input pins are required as well. When rewritten for the ATV750, only four macrocells are required, and eight sum terms and flip-flops. No extra inputs are required, as the ATV750's I/Os are true input/output pins.

The equations for the ATV750 are in Figure 3. This compaction is possible for three reasons:

1. The individual product terms for OE permit the pin to be used as both an input and output.

2. The three feedback paths allow both registers to be used while the pin status is still available to the array.

3. The product term for the flip-flop clock means that the sum term for one of the flip-flops can be shared between the D input and the output pin. A single ATV750 macrocell can incorporate logic which would require up to three output pins and one input pin in other PLDs.

Figure 2.

```
ad0   =   adp0 & !pcs & !rd & ai0 & !ai2              " output data
      #   !pc0 & !pcs & !rd & !ai0 & !ai2             " status "
      #   yst & !pcs & !rd & !ai0 & !ai2;             " status unly

ad1   =   adp1 & !pcs & !rd & ai0 & !ai2              " output data
      #   !pc1 & !pcs & !rd & !ai0 & !ai2;            " status "

ad2   =   adp2 & !pcs & !rd & ai0 & !ai2              " output data
      #   xst & !pcs & !rd & !ai0 & !ai2              " status "
      #   !pc0 & !pcs & !rd & !ai0 & !ai2             " status  "
      #   !pc1 & !pcs & !rd & !ai0 & !ai2;            " status  "

ad3   =   adp3    & !pcs & !rd & ai0 & !ai2           "  output data
      #   startqb & !pcs & !rd & !ai0 & !ai2;         "  status "

adp0  :=  ad0 & !pcs & !wr                            "  load data
      #   pdout & !ystb                               "  circulate y"
      #   pdout & !xstb                               "  circulate x"
      #   pdout & !pcs0                               "  circulate load"
      #   pdout & !pcs1                               "  circulate load"
      #   adp0 & ystb & xstb & pcs0 & pcs1 & pcs      "  hold data"
      #   adp0 & ystb & xstb & pcs0 & pcs1 & wr;      "  hold data"

adp1  :=  ad1 & !pcs & !wr                            "  load data
      #   adp0 & !ystb                                "  circulate y"
      #   adp0 & !xstb                                "  circulate x"
      #   adp0 & !pcs0                                "  circulate load"
      #   adp0 & !pcs1                                "  circulate load"
      #   adp1 & ystb & xstb & pcs0 & pcs1 & pcs      "  hold data"
      #   adp1 & ystb & xstb & pcs0 & pcs1 & wr;      "  hold data"

adp2  :=  ad2 & !pcs & !wr                            "  load data
      #   adp1 & !ystb                                "  circulate y"
      #   adp1 & !xstb                                "  circulate x"
      #   adp1 & !pcs0                                "  circulate load"
      #   adp1 & !pcs1                                "  circulate load"
      #   adp2 & ystb & xstb & pcs0 & pcs1 & pcs      "  hold data"
      #   adp2 & ystb & xstb & pcs0 & pcs1 & wr;      "  hold data"

adp3  :=  ad3 & !pcs & !wr                            "  load data
      #   adp2 & !ystb                                "  circulate y"
      #   adp2 & !xstb                                "  circulate x"
      #   adp2 & !pcs0                                "  circulate load"
      #   adp2 & !pcs1                                "  circulate load"
      #   adp3 & ystb & xstb & pcs0 & pcs1 & pcs      "  hold data"
      #   adp3 & ystb & xstb & pcs0 & pcs1 & wr;      "  hold data"

ai0   :=  ad0 & pcs                                   "  idle state "
      #   ad0 & ale                                   "  idle state "
      #   ai0 & !pcs & !ale;                          "  hold instruction"

ai1   :=  ad1 & pcs                                   "  idle state "
      #   ad1 & ale                                   "  idle state "
      #   ai1 & !pcs & !ale;                          "  hold instruction"

ai2   :=  ad2 & pcs                                   "  idle state "
      #   ad2 & ale                                   "  idle state "
      #   ai2 & !pcs & !ale;                          "  hold instruction"

ai3   :=  ad3 & pcs                                   "  idle state "
      #   ad3 & ale                                   "  idle state "
      #   ai3 & !pcs & !ale;                          "  hold instruction"
```

Figure 3.

```
ai0.ck    =   clk2 & !ale;  ai2.ck   =   clk2 & !ale;  "clock instruction
ai1.ck    =   clk2 & !ale;  ai3.ck   =   clk2 & !ale;  "clock instruction

ai0       =   ad0 & !pcs & ale                         "load instruction"
          #   adp0 & !pcs & !rd & ai0 & !ai2           "output data
          #   !pc0 & !pcs & !rd & !ai0 & !ai2          "status "
          #   yst & !pcs & !rd & !ai0 & !ai2           "status unly

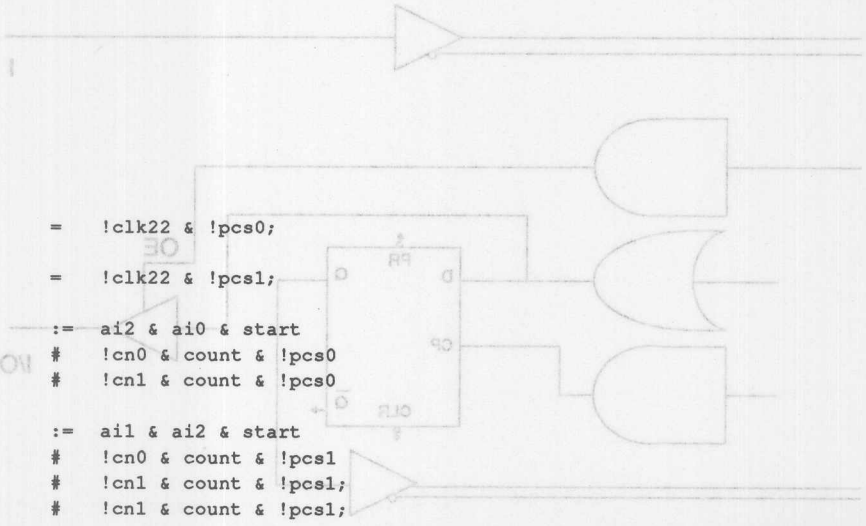
ai1       =   ad1 & !pcs & ale                         "load instruction"
          #   adp1 & !pcs & !rd & ai0 & !ai2           "output data
          #   !pc1 & !pcs & !rd & !ai0 & !ai2;         "status "

ai2       =   ad2 & !pcs & ale                         "load instruction"
          #   adp2 & !pcs & !rd & ai0 & !ai2           "output data
          #   xst & !pcs & !rd & !ai0 & !ai2           "status "
          #   !pc0 & !pcs & !rd & !ai0 & !ai2          "status "
          #   !pc1 & !pcs & !rd & !ai0 & !ai2;         "status "

ai3       =   ad3 & !pcs & ale                         "load instruction"
          #   adp3 & !pcs & !rd & ai0 & !ai2           "output data
          #   startqb & !pcs & !rd & !ai0 & !ai2;      "status "

enable ad0 =  !pcs & !rd;   enable ad2  =       !pcs & !rd;
enable ad1 =  !pcs & !rd;   enable ad3  =       !pcs & !rd;
(adp equations remain the same as before, but are now buried in the macrocell)
```

Figure 4.



```
!pc0      =   !clk22 & !pcs0;

!pc1      =   !clk22 & !pcs1;

!pcs0     :=  ai2 & ai0 & start
          #   !cn0 & count & !pcs0
          #   !cn1 & count & !pcs0

 !pcs1    :=  ai1 & ai2 & start
          #   !cn0 & count & !pcs1
          #   !cn1 & count & !pcs1;
          #   !cn1 & count & !pcs1;
```

• The Chip Interface

The encryption chip is loaded and unloaded serially, four bits at a time in this design. The equations for the interface logic are in Figure 4. Also in this figure is a simple state diagram for the two-bit counter required for this design. This state machine is buried, and its decoded outputs are used to control the serial transfers.

• Starting the Peripheral Chip

To begin execution in the peripheral chip, a bi-directional signal named *start* is asserted. This is an active low signal. The controller must assert this signal low for four clock cycles. Then the exponentiation chip will hold this line low until it has completed its operations. An external pull up resistor is required. The internal flip-flop, whose output is named *stint*, contains the state of the peripheral. This is used to signal the microprocessor that the subsystem is busy when the processor reads the ATV750's status.

• Multiplexing Flip-Flop Inputs and I/O Pins

One I/O pin / flip-flop combination can be used to store the state of the encryption chip and to output this to the peripheral. This is accomplished by multiplexing the sum term output between the flip-flop's D input and the output buffer. The sum term and the OE product term are active to begin the encryption chip's exponentiation cycle. After the state machine counter finishes counting, the output is put into the high impedance state. If the external chip has begun its operation correctly, it will then hold the pin low. Now the state of the I/O pin is used as the D input to the flip-flop, but not output because the OE term is off. The multiplexed macrocell is in Figure 7. The following simple equations are all that is required to implement this logic:

```
enable start    =      !count;
stint           :=     !coun
# !start & count;
start.c         =      clk2;
```

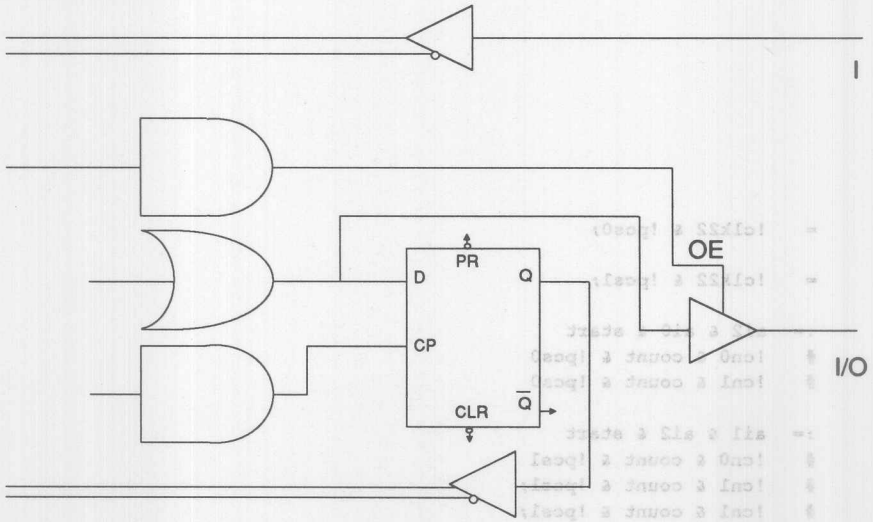
Conclusion

The application of a third generation EPLD in an I/O bus based system demonstrates the usefulness of the following features:

- **Buried Registers**
- **Independent Feedback Paths**
- **Asynchronous Register Clocks.**

This design consists of roughly 600 gates, which fit into a ATV750 gate complexity EPLD with an 80 percent utilization factor. Due to the usefulness of the new features and their implementation in the macrocell of the ATV750, this design, which would have required three second generation devices, could easily fit into one ATV750.

Mulitplexed "D" Input

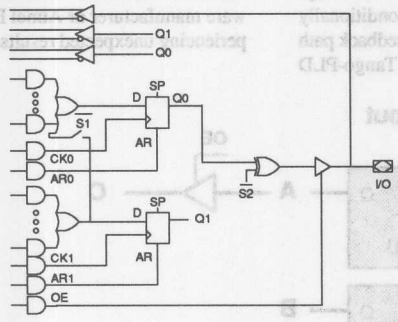


Using the Buried Nodes and Feedbacks

Introduction

Conventional EPLD I/O pin logic forces you to choose either a dedicated output pin or a dedicated input pin. This renders the output register unusable. Multiple feedback paths and individual product term controlled output enables (OEs) make the ATV750 I/O pins truly bi-directional. An ATV750 I/O pin can be configured as a dedicated input, a dedicated output, or an input and output bus interface pin. No registers are sacrificed in the process. All registers can be buried.

Registered Output



Buried Registers

To use the buried register outputs, they must have a unique name. The compilers need to know which register to associate with each signal name. Each compiler uses a different method for assigning node numbers to signal names. Table 1 shows how to assign these names for each compiler. Table 2 lists node names for each compiler. Note: Q1 need not be defined if Q0 is sharing Q1's product terms.

ABEL™, Atmel-ABEL™, CUPL™, and Tango-PLD: If the output is combinatorial or if Q0 shares the product terms of Q1 in a registered output, the Q1 node does not need a name. Name Q1 nodes with the proper node numbers and refer to Feedback Options on how to access Q0s and Q1s.

LOGiC: LOGiC requires you to name the Q0 nodes if you are using the pin as an input and still using Q0, or if you are using OE to make the pin an input and an output.

PistoHl: No node numbers are necessary. Q0 nodes are named by declaring

```
: nodename0 Q0! pinname;
```

Q1 nodes are named by declaring

```
: nodename1 Q1! pinname;
```

Table 1. ATV750 Node Declaration

Product	Example	Node	Declaration	Comments
ABEL™	anyname	node	26;	
Atmel-ABEL™	anyname	node	26;	
CUPL™	pinnode	25 =	anyname;	
LOGiC	anyname	=	1;	Following key word *NODE
PistoHl	anyname	Q0!	pinname;	Use Q1! for Q1 declaration
TangoPLD	anyname			In PUTPART place "anyname" as the 25th signal

Table 2. ATV750 Node Numbers

ATV750 Pin Numbers	ABEL™ Q1	Atmel-ABEL™ Q1	CUPL™ Q1	LOGIC Q0	LOGIC Q1	TangoPLD Q1
14	26	26	25	2	1	25
15	27	27	26	4	3	26
16	28	28	27	6	5	27
17	29	29	28	8	7	28
18	30	30	29	10	9	29
19	31	31	30	12	11	30
20	32	32	31	14	13	31
21	33	33	32	16	15	32
22	34	34	33	18	17	33
23	35	35	34	20	19	34

ATV750 Feedbacks

Each third party product uses a slightly different syntax for accessing the feedback paths (refer to Table 3). Whenever the Q0 register is used and the OE term is disabled or conditionally disabled, care must be taken to ensure the correct feedback path is referred to in your equations. Version 1.11 of Tango-PLD does not support the Q0 feedback. This syntax may change with each new software revision. Please check with the specific software manufacturer or Atmel EPLD Applications if you are experiencing unexpected results.

Feedback Options: Registered Output

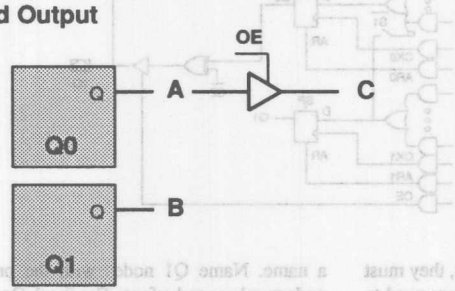


Table 3. ATV750 Feedback Paths

	A	B	C
ABEL™	pinname.FB	nodename	pinname
Atmel-ABEL™	pinname.FB	nodename	pinname
CUPL™	pinname	nodename	pinname.IO
LOGiC	nodename0	nodename1	pinname
PistoHI	nodename0	nodename1	pinname
TangoPLD	no support	nodename	pinname

ATV2500 Node Numbering

With an additional OR, the ATV2500 logic cell becomes even more versatile than the ATV750 logic cell. Under certain situations, an additional set of buried registers must be defined. The same syntax used for ATV750 (Table 3) can be used to name the ATV2500 buried registers. The node numbers are listed in Table 4.

ABEL™, Atmel-ABEL™, CUPL™, and TangoPLD: Q1 need not be named when the output logic cell is configured as 8- or 12-term combinatorial output. Q2 need not be named when output logic cell is configured as 12-product term combinatorial or registered output. Name Q1 and Q2 nodes with the proper node numbers and refer to Feedback Options for selecting the correct feedback paths.

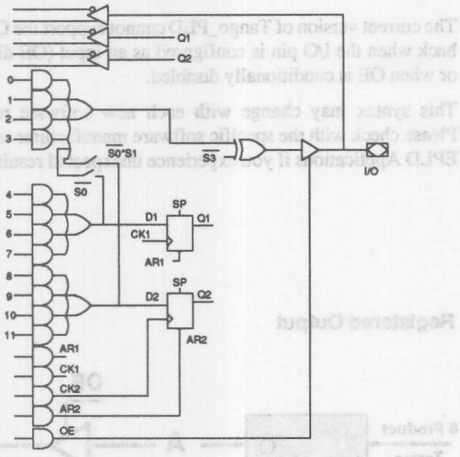
PistoHI: No node numbers are necessary.
Q1 nodes are named by declaring

```
: nodename1 Q1! pinname;
```

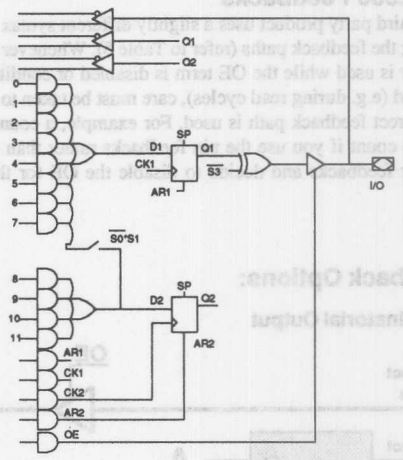
Q2 nodes are named by declaring

```
: nodename2 Q2! pinname;
```

Combinatorial Output



Registered Output



7

Table 4. ATV2500 Node Numbers

ATV2500 Pin Numbers	ABEL™		Atmel-ABEL™		CUPL™		TangoPLD	
	Q1	Q2	Q1	Q2	Q1	Q2	Q1	Q2
4(1)	217	41	217	41	65	41	41	65
5(1)	218	42	218	42	66	42	42	66
6(2,3)	219	43	219	43	67	43	43	67
7(3)	220	44	220	44	68	44	44	68
8	221	45	221	45	69	45	45	69
9	222	46	222	46	70	46	46	70
11	223	47	223	47	71	47	47	71
12	224	48	224	48	72	48	48	72
13	225	49	225	49	73	49	49	73
14	226	50	226	50	74	50	50	74
15	227	51	227	51	75	51	51	75
16	228	52	228	52	76	52	52	76
24	229	53	229	53	77	53	53	77
25	230	54	230	54	78	54	54	78
26	231	55	231	55	79	55	55	79
27	232	56	232	56	80	56	56	80
28	233	57	233	57	81	57	57	81
29	234	58	234	58	82	58	58	82
31	235	59	235	59	83	59	59	83
32	236	60	236	60	84	60	60	84
33	237	61	237	61	85	61	61	85
34	238	62	238	62	86	62	62	86
35	239	63	239	63	87	63	63	87
36	240	64	240	64	88	64	64	88

Notes: 1. Due to the memory limitations of PC/MS DOS, ABEL™ PC versions 3.0 to 3.2 and Atmel-ABEL™ version 1.01 do not support the macrocells associated with pin 4 and 5. These pins can only be used as inputs.

2. These same versions of ABEL™ and Atmel-ABEL™ (see above) do not support the AR terms of Q2 associated with pin 6.
3. These same versions of ABEL™ and Atmel-ABEL™ (see above) do not support the Synchronous Preset of pin 6 and 7.

ATV2500 Feedbacks

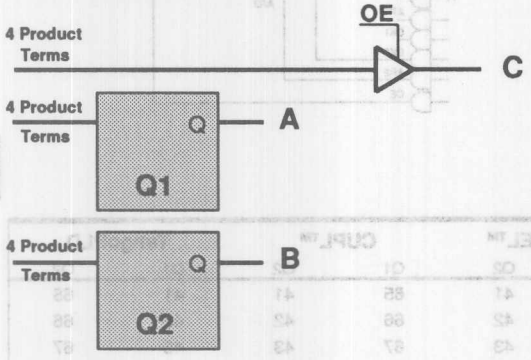
Each third party product uses a slightly different syntax for accessing the feedback paths (refer to Table 5). Whenever the Q1 register is used while the OE term is disabled or conditionally disabled (e.g. during read cycles), care must be taken to ensure the correct feedback path is used. For example, a counter can lose its count if you use the pin feedbacks rather than the Q1 register feedbacks and decide to disable the OE for the read cycle.

The current version of Tango_PLD cannot support the Q1 feedback when the I/O pin is configured as an input (OE disabled) or when OE is conditionally disabled.

This syntax may change with each new software revision. Please check with the specific software manufacturer or Atmel EPLD Applications if you experience unexpected results.

Feedback Options:

Combinatorial Output



Registered Output

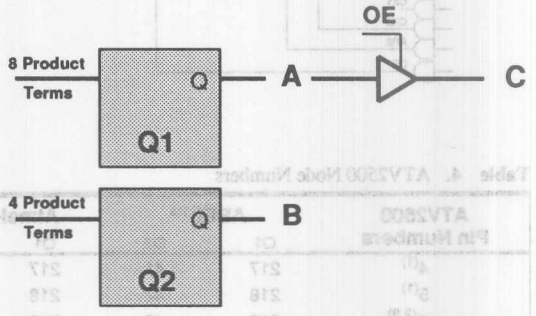


Table 5. ATV2500 Feedback Paths

		A	B	C
ABEL™	Registered	pinname.FB	nodename2	pinname
	Combinatorial	nodename1	nodename2	pinname,
CUPL™	Registered	pinname	nodename2	pinname.IO
	Combinatorial	nodename1	nodename2	pinname
Tango-PLD	Registered	no support	nodename2	pinname
	Combinatorial	nodename1	nodename2	pinname

Testing Non-Windowed CMOS PLDs

Atmel's testing of non-windowed CMOS PLDs is comprehensive and thorough. It is sufficient to guarantee programmability and performance. The wafer-probe test checks one-hundred percent of all memory elements for programmability. Final test of packaged units checks programming a second time. Performance testing on the *Quality Test Array* (QTA) guarantees AC test parameters. This data shows a high degree of correlation with standard array performance data.

Introduction

Atmel's corporate goal is to meet or exceed our customers' requirements one-hundred percent of the time. This means we must prove to ourselves that each product shipped will perform as specified or better.

PLDs must meet two different device requirements: they must program as a memory device, and they must function as a logic device. This requires testing all devices in two very different ways.

The programmable elements in Atmel's CMOS PLDs are UV EPROM memory cells. The AND array programs like an EPROM. UV light cannot penetrate non-windowed packages (e.g., any plastic package or solid lid ceramic package). Erasing a non-windowed EPROM element is not possible. Any testing by Atmel before shipment cannot program the main AND array or the customer cannot enter his own pattern.

Atmel's test methodology guarantees our PLDs will program and perform to the data sheet, even without programming this main AND array.

Figure 1. Non-Windowed PLD Test Flow

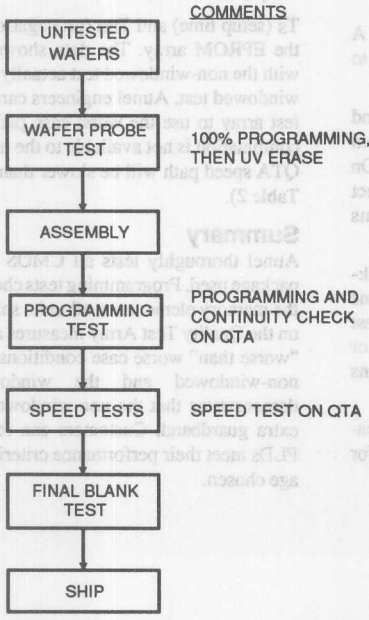
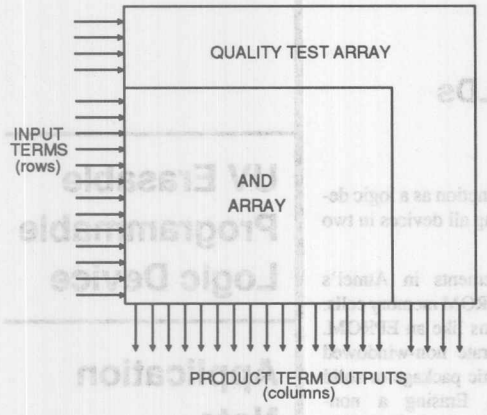


Figure 2. PLD Topography



Programming

After wafer fabrication, the first test is wafer-probe (Figure 1). All PLD dice manufactured by Atmel use a similar wafer test program. This test programs one-hundred percent of the memory bits used to implement the AND array in our PLDs. This programming algorithm is more aggressive than that implemented by programming manufacturers. After verifying all bits, the wafer is then UV erased before proceeding further.

Package assembly is next. If the packaging used does not have a UV translucent window, the customer is the only one who can program the device. Atmel must guarantee performance and programming by testing other EPROM cells in the device.

These other EPROM cells are next to the main AND array. A discussion of the PLD AND array topography clarifies how to test the extra EPROM cells (Figure 2).

Product term inputs enter the AND array from one end, and form the *rows* of the matrix. Product term outputs leave from the bottom— product terms form the *columns* of the matrix. On the far right of Figure 2 are the Quality Test Array product terms (columns). At the top of the array are the QTA input terms (rows).

Even though wafer-probe tests all units' programming, packaged units also have their QTA terms tested. Since these terms are physically at the ends of the inputs and outputs, this test checks the integrity of these lines. The test detects any shorts or opens on the inputs or outputs. Programming these locations also provides a thorough test of the programming circuitry.

The wafer-probe test programs one-hundred percent of all locations, and the package test checks the programming circuitry for continuity and programmability.

Performance Testing

The logic test parameters divide into two groups: DC and AC test values. All of the DC test parameter tests are independent of the logic programmed into the device. This means that DC testing is the same for every PLD sold by Atmel, independent of the package used.

Every different logic implementation results in different AC performance. Atmel measures AC performance using a "worst case" pattern. This pattern is slightly different in nature for each PLD. This pattern uses every resource available in the device. Outputs can be made to switch in the same direction at the same time. The test program applies worst case combinations of input term and product term patterns to the device. Atmel collects AC data with this pattern on each UV erasable device shipped.

Non-erasable devices cannot use their main array for this test. Atmel programs a special speed test pattern into the QTA. Tests on this array measure all of the same AC characteristics as those done on erasable units. Correlations between the main array and the QTA follow.

Correlation

Three parameters measured on 26 units show a high degree of correlation between windowed PLD testing and non-windowed PLD testing. Measurements of T_{CO}, T_S, and T_{PD} show little difference between performance testing on the standard array versus performance testing on the QTA.

T_{CO} (clock to output) is independent of the memory array. The signal path is directly from the clock input buffer to all ten flip-flops in the AT22V10, and then straight to the output buffer. The data shows a very tight distribution, and the difference in the two measurement techniques is within the accuracy of the setup (see Table 1).

T_S (setup time) and T_{PD} (propagation delay) are dependent on the EPROM array. The data shows an excellent correlation, with the non-windowed test actually measuring slower than the windowed test. Atmel engineers carefully designed the quality test array to use the worst case paths for all conditions. This combination is not available to the user, but guarantees that the QTA speed path will be slower than the user's speed path (see Table 2).

Summary

Atmel thoroughly tests all CMOS PLDs independent of the package used. Programming tests check one-hundred percent of the memory elements on all units shipped. Performance testing on the Quality Test Array measures all AC test parameters with "worse than" worse case conditions. Data taken with both the non-windowed and the windowed performance tests demonstrates that the non-windowed test is accurate and has extra guardband. Customers can feel confident that Atmel's PLDs meet their performance criteria independent of the package chosen.

Table 1. T_{CO} Performance Testing Comparison

Parameter Test	T_{CO} Window	T_{CO} Non-Window	Delta
Average	8.91 ns	8.68 ns	+0.23 ns
Std. Dev.	0.18 ns	0.15 ns	0.06 ns

Table 2. T_S and T_{PD} Performance Testing Comparison

Parameter Test	T_S Window	T_S Non-Window	Delta	T_{PD} Window	T_{PD} Non-Window	Delta
Average	6.80 ns	6.97 ns	-0.17 ns	13.92 ns	14.17 ns	-0.25 ns
Std. Dev.	0.09 ns	0.11 ns	0.09 ns	0.25 ns	0.25 ns	0.18 ns

Parameter Test	Tco Window	Tco Non-Window	Delta
Average	8.87 ns	8.62 ns	+0.23 ns
Std. Dev.	0.18 ns	0.15 ns	0.06 ns

Parameter Test	Ts Window	Ts Non-Window	Delta	Tpd Window	Tpd Non-Window	Delta
Average	6.80 ns	6.97 ns	-0.17 ns	13.92 ns	14.17 ns	-0.25 ns
Std. Dev.	0.09 ns	0.11 ns	0.09 ns	0.25 ns	0.25 ns	0.18 ns

Designing with the Atmel-ViewPLD Development Tool

Like the Atmel-ABEL™ software, the Atmel-ViewPLD development tool uses a popular industry-standard CAE development system. The development tool integrates the Viewlogic Workview software as the design environment with Data I/O's back-end technology of device fitting and fusemapping. With this development tool, a designer can use schematic capture and/or the ABEL™ Hardware Description Language (ABEL HDL) to functionally describe his or her design requirements. Additionally, the development tool also allows the designer's previous PLD designs in the form of JEDEC files to be read and modelled so that the schematic representations of the designs can be generated.

In this application note, the Atmel-ViewPLD features developed specifically for Atmel EPLDs are discussed. Also included are the design hints which allow your designs to be efficiently fitted into your favorite Atmel EPLD, and the Schematic-to-JEDEC and ABEL-to-JEDEC compilation process flows. Below is a listing of the topics covered in this application note:

- The Atmel-ViewPLD Menu Commands "Schematic → JEDEC," "ABEL → JEDEC," and "Prep WIR (Device)"
- The DIO and DSTD symbols
- Using the IN.1 and OUT.1 symbols for your design input and output pins
- Setting your input signal to a constant logic level
- Applying the D_LATCH.1 and IN_LATCH.1 symbols for the ATV5000 or ATV5100 devices
- What to do with the unused pins of a DSTD symbol
- Creating a Viewdraw schematic from an ABEL™ or a JEDEC file
- Simulating your design using worst-case timing values

For your reference, the DIO primitive and DSTD symbols are listed at the end of this application note.

The Atmel-ViewPLD Menu Commands

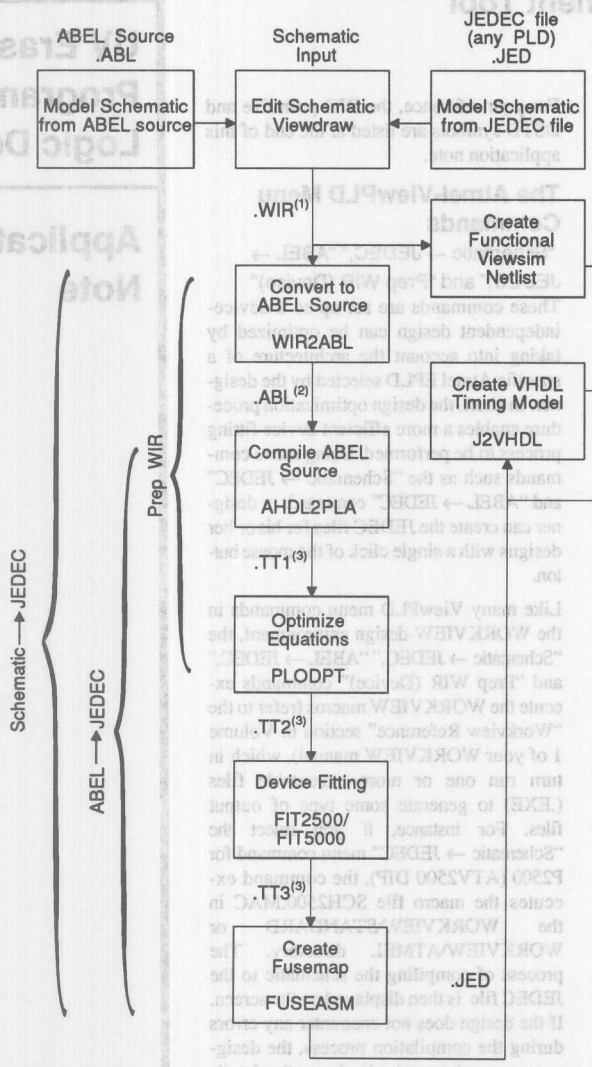
"Schematic → JEDEC," "ABEL → JEDEC," and "Prep WIR (Device)"

These commands are set up so a device-independent design can be optimized by taking into account the architecture of a specific Atmel EPLD selected by the designer. In short, the design optimization procedure enables a more efficient device fitting process to be performed. Using menu commands such as the "Schematic → JEDEC" and "ABEL → JEDEC" commands, a designer can create the JEDEC files for his or her designs with a single click of the mouse button.

Like many ViewPLD menu commands in the WORKVIEW design environment, the "Schematic → JEDEC," "ABEL → JEDEC," and "Prep WIR (Device)" commands execute the WORKVIEW macros (refer to the "Workview Reference" section in Volume 1 of your WORKVIEW manual), which in turn run one or more executable files (.EXE) to generate some type of output files. For instance, if you select the "Schematic → JEDEC" menu command for P2500 (ATV2500 DIP), the command executes the macro file SCH2500.MAC in the WORKVIEW\STANDARD or WORKVIEW\ATMEL directory. The process of compiling the schematic to the JEDEC file is then displayed on the screen. If the design does not encounter any errors during the compilation process, the designer may not be required to know the details of the process. However, it would be advantageous for the designer to understand each process step, especially when the design encounters some compilation errors.

Note that prior to executing the "Schematic → JEDEC" or "Prep WIR (Device)" menu command, you would first need to open your design schematic via Viewdraw. These commands will read in the schematic file name that is currently opened. For the "ABEL → JEDEC" menu command, the design file name will be prompted for immediately after execution of the command.

Figure 1. The Atmel-ViewPLD Compilation Process



Notes:

1. A WIR file is created by Viewdraw only after executing a "File Write" command in Viewdraw.
2. Before generating the ABEL™ (.ABL) file, the WIR2ABL (WIR-to-ABEL) generates an intermediate file with extension .VNT. If an error occurs in the WIR-to-ABEL conversion specifying that there is an intermediate file error, then the error description will listed in this .VNT file.
3. The files .TT1, .TT2, and .TT3 are in the Open ABEL PLA format.

The DIO and DSTD Symbols

Like all other CAE primitive symbols, the DIO primitive symbols provide the building blocks for implementing an Atmel-ViewPLD design. In the Atmel-ViewPLD development tool, all of the functional DIO symbols such as AND2, AND4, DFF, and TFFC, are logically described using Boolean equations in the functional library files. These files, which include V2500.FLB, V5000.FLB, and VIEWLOGI.FLB, are located in the WORKVIEW\STANDARD\LIB4 or WORKVIEW\ATMEL\LIB4 directory. Figure 2 illustrates the AND2 and TFF symbols and their logic representations in the functional library file.

As shown in Figure 2, the architectural capabilities in each Atmel EPLD determine the type of equation in the function library file. In fact, there are some DIO symbols which are not applicable for some of the Atmel EPLDs because of their architecture limitations. For instance, the DFFPC symbol, which is a D-type flip-flop with asynchronous preset and clear controls, is applicable for the ATV5000 and ATV5100 devices, but not for the ATV750 and ATV2500 devices. Please refer to the DIO Library listing (Table 2) at the end of this application note for the complete information on the applicabilities of the DIO symbols.

Table 1 shows the three functional library files included with the Atmel-ViewPLD development tool:

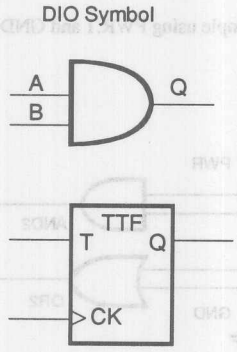
Table 1. Function Library Files

FLB File	Description
V2500.FLB	Logic equations optimized for ATV750 and ATV2500 devices
V5000.FLB	Logic equations optimized for ATV5000 and ATV5100 devices
Viewlogi.FLB	Generic library called by the "PREP WIR" command, not the "Prep WIR (Device)" command

The first two library files are optimized for the ATV750, ATV2500, and ATV5000/5100 device families. The third file, VIEWLOGI.FLB, is used by the "Prep WIR" menu command. This command is designed for use if the designer wishes to partition his or her design into multiple designs which are optimized for the devices selected by the designer. Since each functional library file is in ASCII format, the logic equations representing the DIO symbols can easily be modified by the designer. This flexibility allows the designer to generate his or her own DIO primitive symbols.

For more information on the DIO and DSTD symbols, please refer to the listings found in Table 3 at the end of this application note. Note that the DSTD symbols are the 74-Series TTL symbols which are made up of the DIO primitive symbols.

Figure 2. The AND2 and TFF DIO Symbols and their Logic Equations in the V2500.FLB and V5000.FLB Files



Logic Equation in V2500.FLB

```
Q = A & B;
```

```
Q = (T & !Q)#
    (!T & Q);
Q.ck = CK;
```

Logic Equation in V5000.FLB

```
Q = A & B;
```

```
Q = T;
Q.ck = CK;
```

Using the IN.1 and OUT.1 Symbols for your Design Input and Output Pins

For creating the input and output pins for your design, you would need to add the IN.1 and OUT.1 symbols (see Figure 3) from the DIO library to your design. Simply use the "Add Comp" menu command to add the IN.1 or OUT.1 symbol to the dangling input nodes. Pin labels must also be assigned to these symbols, and not assigned to the nets or nodes. For a design to be compiled successfully, you must have at least one input pin defined. Note that a design will simulate properly via Viewsim without any IN.1 and OUT.1 symbols (see Figures 3-4).

Figure 3. IN.1 and OUT.1 DIO Symbols[1]

Symbols

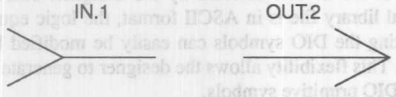
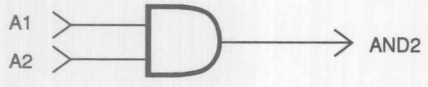


Figure 4. Design Example using IN.1 and OUT.1 Symbols

Schematic



ABEL™ Source File

```
AND2, A2, A1 pin;
AND2 istype 'com';

Equations

AND2 = A1 & A2;
```

Setting your Input Signal to a Constant Logic Level

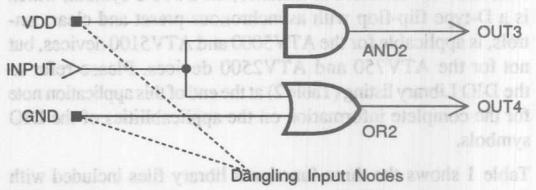
There are two methods which you can use to set your input signals to a constant logic level:

Method 1. Label your input nodes using the VDD and GND labels (see Figure 5).

Method 2. Use the PWR.1 and GND.1 symbols from the DIO library (see Figure 6).

Figure 5. Design Example using VDD and GND Labels[2]

Schematic



ABEL™ Source File

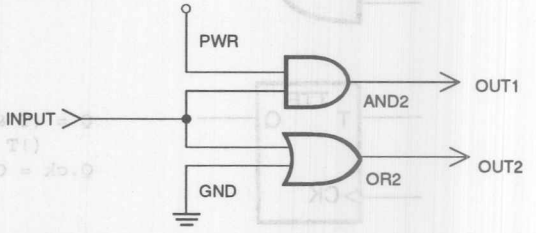
```
OUT3,OUT4,INPUT pin;
OUT3,OUT4 istype 'com';

Equations

OUT3 = 1 & INPUT;
OUT4 = 0 # INPUT;
```

Figure 6. Design Example using PWR.1 and GND.1 DIO Symbols

Schematic



ABEL™ Source File

```
OUT2,OUT1,INPUT pin;
OUT2,OUT1 istype 'com';

Equations

OUT2 = INPUT # 0;
OUT1 = 1 & INPUT;
```

Notes:

1. Please refer to the next section when you are asssigning the VDD and GND labels to the IN.1 and OUT.1 symbols.
2. Do not use the IN.1 and OUT.1 symbols when using the VDD and GND labels to create a constant logic level. If you use these input and output symbols, then the external pins with labels "VDD" and "GND" will be generated.

Applying the D_LATCH.1 and IN_LATCH.1 Symbols for the ATV5000 or ATV5100 Device

The D_LATCH.1 symbol can be used in a design for latching internal or external signals. This symbol uses a D-type flip-flop with asynchronous preset and reset controls to emulate the latch function (the logic equations are specified in the functional library files; refer to "The DIO and DSTD Symbols" section for more information). This symbol can be used as an output or buried latch. The data flows through when $\overline{G}$ is HIGH. Once $\overline{G}$ goes LOW, the data is latched (see Figure 7).

The IN_LATCH.1 symbol is only used for latching inputs in the ATV5000 or ATV5100 design. Unlike the D_LATCH.1 symbol, this symbol is implemented in the ATV5000 or ATV5100 using a real latch circuitry in each I/O pin. The data flows through when C is LOW, and data is captured on the rising edge of the C signal (see Figure 8).

What to Do with the Unused Pins of a DSTD Symbol[1]

For DSTD symbols consisting of combinatorial logic such as the DSTD155 or DSTD156, the unused pins can be left unconnected. The unused logic will be automatically removed from the ABEL™ source file as illustrated by Design Example 1 in Figure 9.

On the other hand, careful attention must be paid to the unused pins if the symbols have registered or latched logic. With symbols that have registered or latched logic, pins and nodes are automatically assigned to the unused inputs and outputs respectively. With the limited number of pins and nodes in the most devices, the assigned pins and nodes may prevent your final design from fitting into the selected device. Design Example 2 in Figure 10 illustrates the problem in which three pins and nodes are unnecessarily created.

In Design Example 2 (Figure 10), a total of three unnecessary pins were assigned and three unnecessary nodes generated.

To eliminate all the unnecessary assigned pins, we recommend grounding the unused inputs. To reduce the unnecessary assigned nodes to a single node, all the unused outputs of the symbol should be connected together to form a single node with an easily identifiable label such as NC or DUMMY. With these modifications implemented, instead of three pins and three nodes wasted as illustrated in Design Example 2, the efficiency of your design improved with:

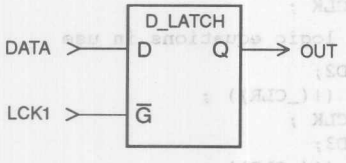
- no additional pins generated, and
- only one additional node created. Usually this single node would not inhibit the design from fitting into the selected device. But if it does, then it can be manually deleted off the ABEL™ source file.

In Design Example 3 (Figure 11), only one node (i.e., node NC1) was created and no additional input pins assigned.

Note:
1. This restriction for the unused pins of the DSTD symbols will be eliminated in the future versions of the Atmel-ViewPLD development tool.

Figure 7. Design Example using D_LATCH.1 DIO Symbol

Schematic



ABEL™ Source File

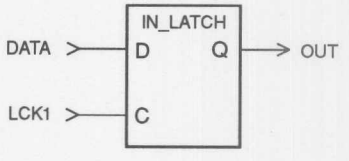
```
OUT1,LCK1,DATA pin;
OUT istype 'buffer,reg_d';

Equations

OUT.D = 1
OUT.AP = (LCK1 & DATA);
OUT.AR = (LCK1 & !DATA);
OUT.C = 1;
```

Figure 8. Design Example using IN_LATCH.1 DIO Symbol

Schematic



ABEL™ Source File

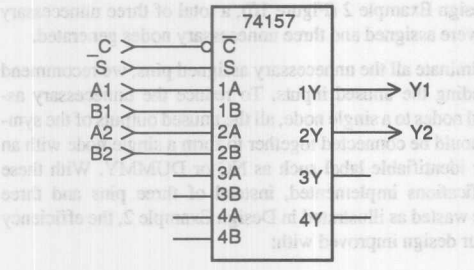
```
OUT,LCK1,DATA pin;
OUT istype 'buffer,reg_d';

Equations

OUT.D = DATA;
OUT.LE = LCK1;
```

Figure 9. Design Example 1, A DSTD Symbol with Combinatorial Logic in which the unused pins are left unconnected.

Schematic

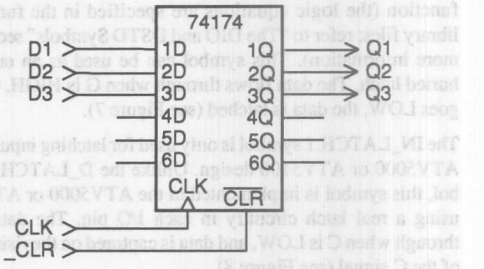


ABEL™ Source File

```
_C,Y2,Y1,S,B2,B1,A2,A1 pin ;
Y1   istype   'com';
Y2   istype   'com';
Equations
Y1 = !((!(A1 & !S) & !(B1 & S)) # _C);
Y2 = !((!(A2 & !S) & !(B2 & S)) # _C);
```

Figure 10. Design Example 2, A DSTD Symbol with Registered Logic in which the unused pins are left unconnected generated.

Schematic

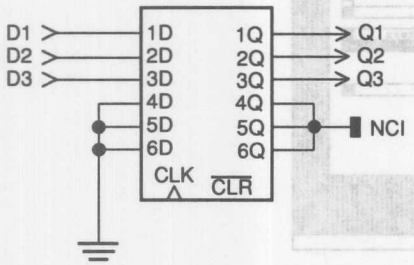


ABEL™ Source File

```
S10,S7,S4 pin ; "Unused inputs
S3,S6,S9 node ; "Unused outputs
_CLR, Q3, Q2, Q1, D3, D2, D1, CLK pin ;
S9,S6,S3 istype 'buffer, reg, reg_d';
Q3,Q2,Q1 istype 'buffer, reg, reg_d';
Equations
"Unnecessary logic equations
S9.d = S10;
S9.ar = (!(_CLR)) ;
S9.c = CLK ;
S6.d = S7;
S6.ar = (!(_CLR)) ;
S6.c = CLK ;
S3.d = S4;
S3.ar = (!(_CLR)) ;
S3.c = CLK ;
"Actual logic equations in use
Q2.d = D2;
Q2.ar = (!(_CLR)) ;
Q2.c = CLK ;
Q3.d = D3;
Q3.ar = (!(_CLR)) ;
Q3.c = CLK ;
Q1.d = D1;
Q1.ar = (!(_CLR)) ;
Q1.c = CLK ;
```

Figure 11. Design Example 3, A DSTD Symbol with Registered Logic (same as in Design Example 2), but with the unused inputs grounded and unused outputs connected together to form a single node.

Schematic



ABEL™ Source File

```
NC1 node ; "Unused node
_CLR,Q3,Q2,Q1,D3,D2,D1,CLK pin ;

NC1   istype   'buffer, reg, reg_d';
Q2    istype   'buffer, reg, reg_d';
Q3    istype   'buffer, reg, reg_d';
Q1    istype   'buffer, reg, reg_d';

Equations

"Unused logic equations

NC1.d = 0;
NC1.ar = (!(_CLR)) ;
NC1.c = CLK ;

"Actual logic equations in use

Q2.d = D2;
Q2.ar = (!(_CLR)) ;
Q2.c = CLK ;
Q3.d = D3;
Q3.ar = (!(_CLR)) ;
Q3.c = CLK ;
Q1.d = D1;
Q1.ar = (!(_CLR)) ;
Q1.c = CLK ;
```

Creating a Viewdraw Schematic from an ABEL™ or a JEDEC File

One of the valuable features of the Atmel-ViewPLD development tool is the ability to generate a Viewdraw schematic from an ABEL™ or a JEDEC file. With this feature, you can use both the schematic capture and ABEL HDL design entries in the same design. In addition, old designs which consist of PLDs or TTL devices that are already in production can easily be integrated into a single design so that it can be compiled to fit into a single PLD like the Atmel ATV5000 or ATV5100 device.

The command for generating a Viewdraw schematic from an ABEL™ or a JEDEC file is the "Window Open ViewPLD Model_Device Schematic" menu command. Once this command is executed, the dialog box shown in Figure 12 will open. After selecting your options, click the middle button of the mouse to begin executing the command.

Use the left button of the mouse to select the options or to enter the project name which is the ABEL™ or JEDEC filename. Note that you must not enter the file extension (.ABL or .JED) when entering the project name.

Figure 13 shows the process flow for generating a schematic from an ABEL™ file or a JEDEC file.

Figure 12. Dialog Box for Modelling an ABEL™, JEDEC, or PLA File to Create a Viewdraw Schematic

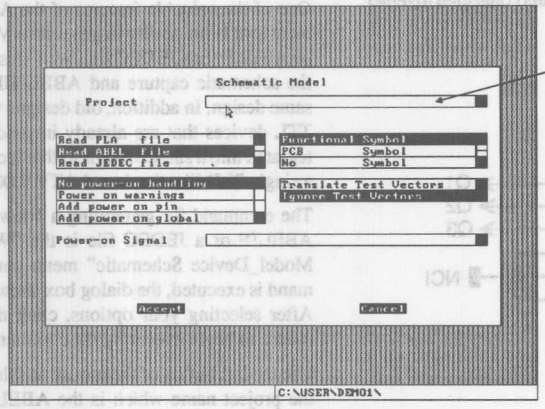
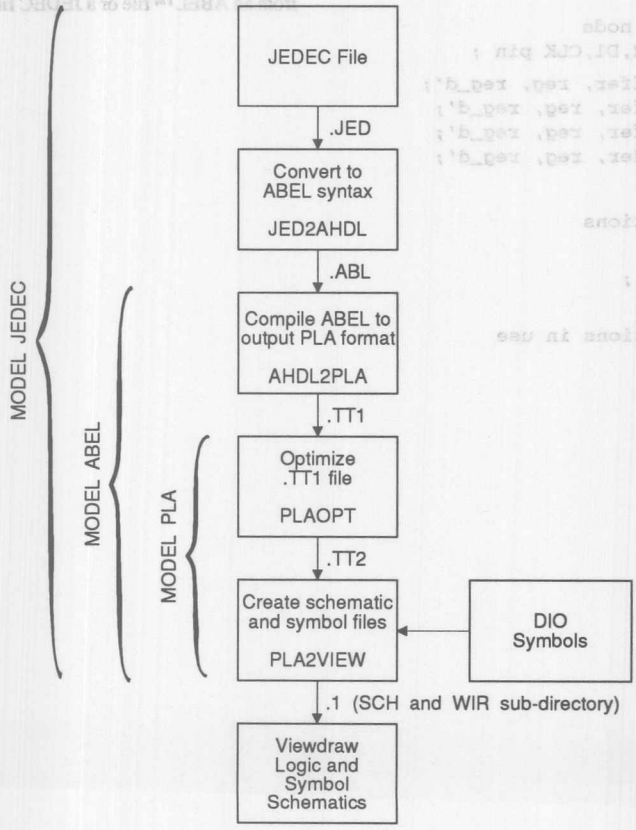


Figure 13. Process Flow for Modelling a Viewdraw Schematic



Simulating Your Design Using Worst-Case Timing Values

After you have created a JEDEC file for your design, you can further verify your design by simulating your design using the worst-case timing values of the selected device. Simulating your design using worst-case timing values provides significant benefits such as predicting the performance of your design, providing information on timing violations, and etc.

Prior to creating a timing model, you must first run the menu command "Window Open ViewPLD Search_TimBase." This command will extract the timing data of the selected device from the global timing database and store them locally in the .TIM file (same filename as your design file but with extension .TIM). Note that the ASCII timing data in the .TIM file can be modified by the users if the new timing data for a new speed version device is available from Atmel.

After creating the local timing database, execute the "Window Open ViewPLD Model_Device Timing_Model" menu command to open the JEDEC Modeller dialog box as shown in Figure 14. Select your options and click the middle button of the mouse to start executing the command (see Figure 15).

Figure 14. JEDEC Modeller Dialog Box for Creating a Timing Model with Worst-Case Timing Values

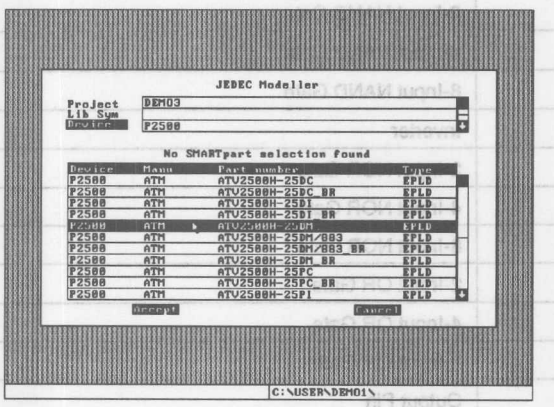
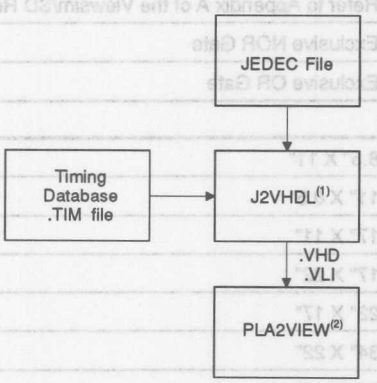


Figure 15. Process Flow for Creating a Timing Model



Notes:
1. Converts the JEDEC file to a timing model in VHDL format. The VHDL Analyzer is then executed to convert the VHDL model to a VLI model which can be read by Viewsim.
2. Creates a symbol schematic of the modelled device, i.e., only used pins will be generated.

Table 2. Atmel-ViewPLD DIO Primitive Symbols

Primitive	Device Supported	Description
Basic Gates		
AND2	All	2-Input AND Gate
AND4	All	4-Input AND Gate
AND8	All	8-Input AND Gate
BUF	All	Buffer
GND	All	Ground
IN	All	Input Pin
NAND2	All	2-Input NAND Gate
NAND4	All	4-Input NAND Gate
NAND8	All	8-Input NAND Gate
NOT	All	Inverter
NOR2	All	2-Input NOR Gate
NOR4	All	4-Input NOR Gate
NOR8	All	8-Input NOR Gate
OR2	All	2-Input OR Gate
OR4	All	4-Input OR Gate
OR8	All	8-Input OR Gate
OUT	All	Output Pin
PWR	All	Power
TRST	All	Tri-State Buffer, Output Enabled on High
TRIBUF	—	Viewlogic Built-in Primitive – DO NOT USE IN SCHEMATIC. Refer to Appendix A of the Viewsim/SD Reference Guide.
XNOR2	All	Exclusive NOR Gate
XOR2	All	Exclusive OR Gate
Block (Sheet) Size		
ASHEET.1	All	8.5" X 11"
ASHEET.2	All	11" X 8.5"
BSHEET	All	17" X 11"
CSHEET.1	All	17" X 22"
CSHEET.2	All	22" X 17"
DSHEET	All	34" X 22"
ESHEET.1	All	34" X 44"
ESHEET.2	All	44" X 34"

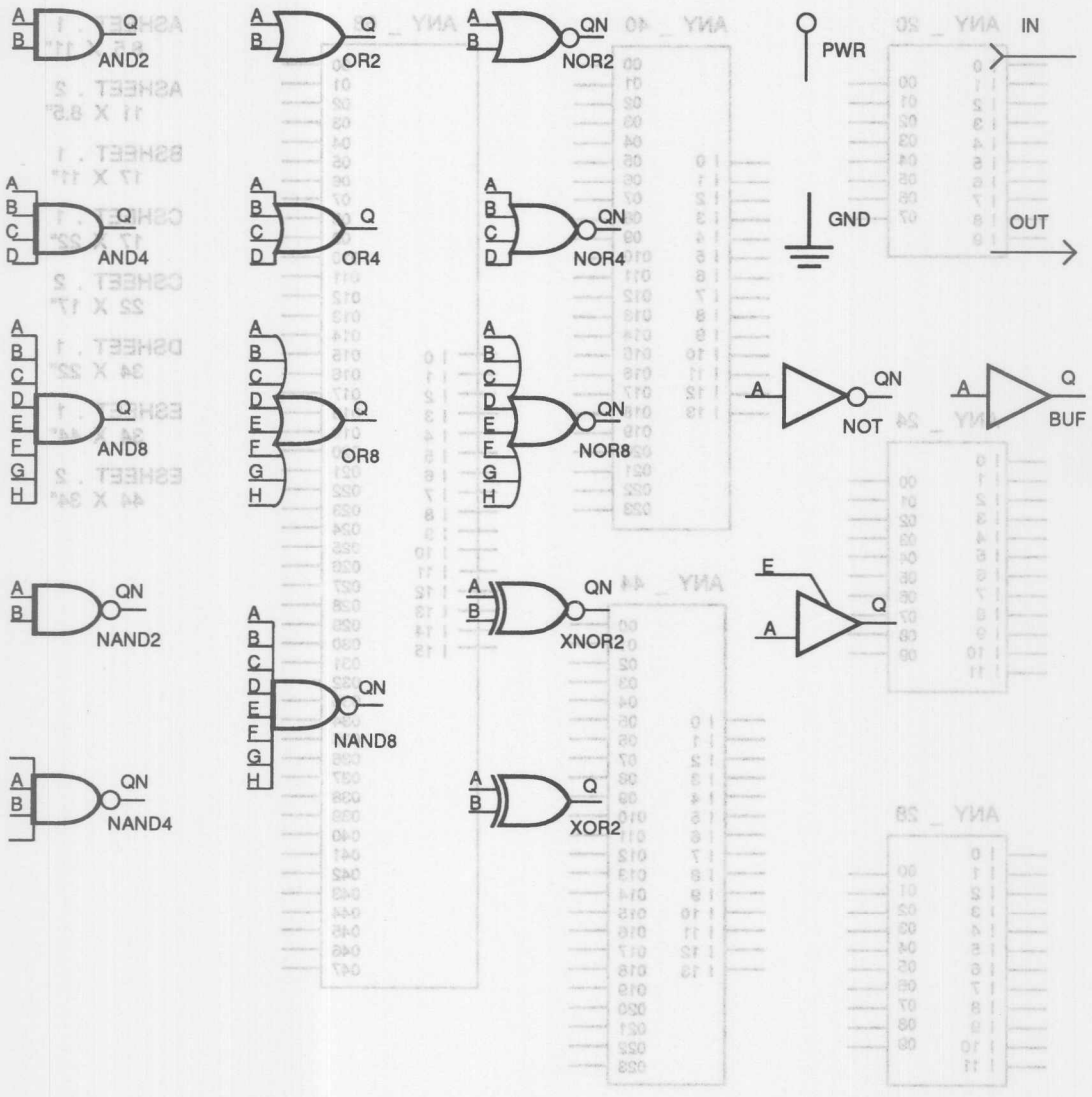
Table 2. Atmel-ViewPLD DIO Primitive Symbols (continued)

Primitive	Device Supported	Description
Generic Device Symbol (For Design Partitioning)		
ANY_20		20-Pin Generic Device
ANY_24		24-Pin Generic Device
ANY_28		28-Pin Generic Device
ANY_40		40-Pin Generic Device
ANY_44		44-Pin Generic Device
ANY_68		68-Pin Generic Device
Latches		
DLATCH	ATV5000 ATV5100	Standard D Latch with Data Flow-Through when G Input is High. Data is latched when G goes LOW. This latch can be used as a buried latch.
IN_LATCH	ATV5000 ATV5100	Input D Latch. The data flow-through occurs when the C input is LOW. Data is latched on the rising edge of C.
RSLATCH	All	RS Latch. In ATV750 and ATV2500 devices, the RS latch is emulated via two cross-coupled NAND gates. In the ATV5000 devices, a flip-flop with asynchronous preset and reset is used.
RS_FF	All	RS Flip-Flop. A D flip-flop is used to emulate the RS flip-flop.
Flip-flops		
DFF	All	D Flip-Flop with no Preset or Reset Function. Flip-flop is reset upon device power-up.
DFFC	All	D Flip-Flop with Asynchronous Reset
DFFP	ATV5000 ATV5100	D Flip-Flop with Asynchronous Preset
DFFPC	ATV5000 ATV5100	D Flip-Flop with Asynchronous Preset and Reset
DFFSP	All	D Flip-Flop with Synchronous Preset
DFFSPC	All	D Flip-Flop with Synchronous Preset and Ssynchronous Reset. In the ATV750 and ATV2500 devices, the synchronous preset is a global preset product term, i.e., a single product term presets a group of flip-flops. In the ATV5000/ATV5100 devices, the preset term can be independently controlled.
JKFF	All	JK Flip-Flop with no Preset or Reset
JKFFC	All	JK Flip-Flop with Asynchronous Reset
JKFFP	ATV5000 ATV5100	JK Flip-Flop with Asynchronous Preset
JKFFPC	ATV5000 ATV5100	JK Flip-Flop with Asynchronous Preset and Reset
JFFSP	All	JK Flip-Flop with Synchronous Preset

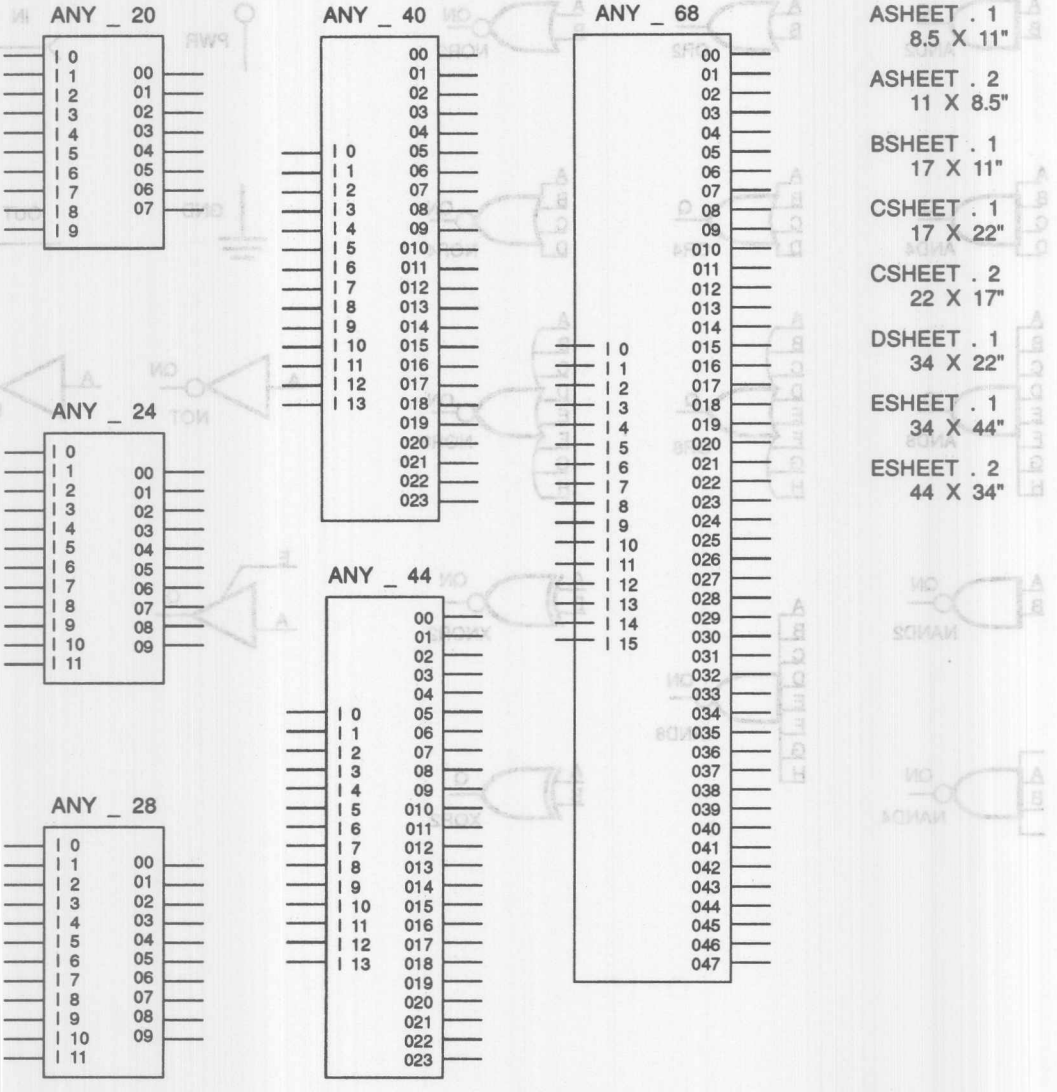
Table 2. Atmel-ViewPLD DIO Primitive Symbols (continued)

Primitive	Device Supported	Description
JKFFSPC	All	JK Flip-Flop with Synchronous Preset and Asynchronous Reset. In the ATV750 and ATV2500 devices, the synchronous preset is a global preset product term, i.e., a single product term presets a group of flip-flops. In the ATV5000/ATV5100 devices, the preset term can be independently controlled.
TFF	All	T Flip-Flop with no Preset or Reset
TFFC	All	T Flip-Flop with Asynchronous Reset
TFFP	ATV5000 ATV5100	T Flip-Flop with Asynchronous Preset
TFFPC	ATV5000 ATV5100	T Flip-Flop with Asynchronous Preset and Reset
TFFSP	ATV750 ATV2500	T Flip-Flop with Synchronous Preset
TFFSPC	ATV750 ATV2500	T Flip-Flop with Synchronous Preset and Asynchronous Reset. In the ATV750 and ATV2500 devices, the synchronous preset is a global preset product term, i.e., a single product term presets a group of flip-flops.
UDFDL	—	Viewlogic Built-In Primitive – DO NOT USE IN SCHEMATIC

Atmel's DIO Primitives, Sheet 1 of 4



Atmel's DIO Primitives, Sheet 2 of 4



ASHEET . 1
8.5 X 11"

ASHEET . 2
11 X 8.5"

BSHEET . 1
17 X 11"

CSHEET . 1
17 X 22"

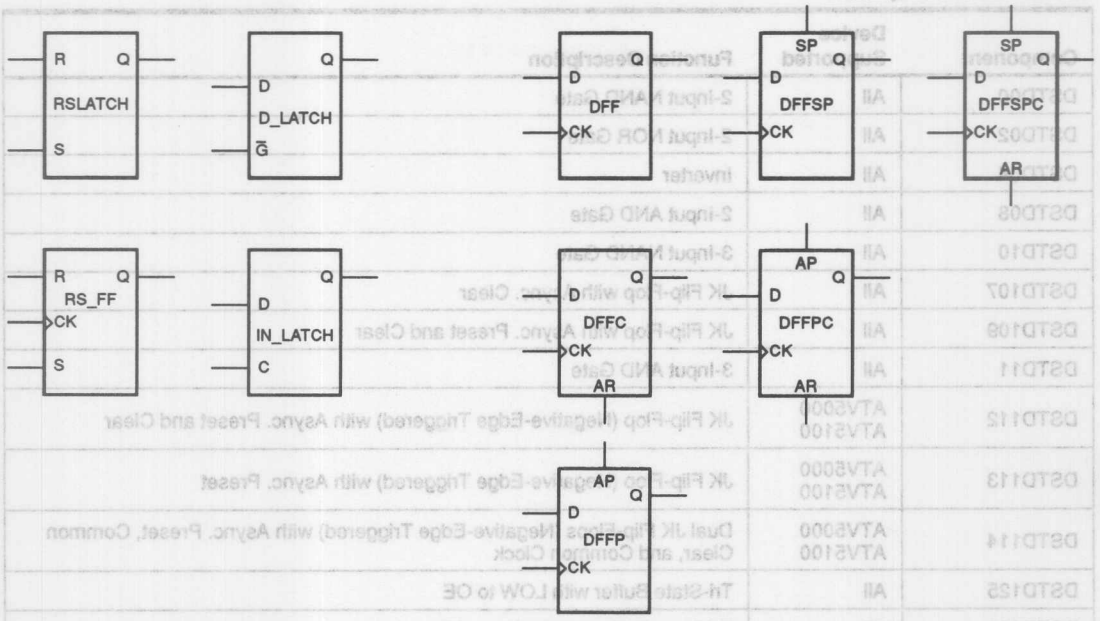
CSHEET . 2
22 X 17"

DSHEET . 1
34 X 22"

ESHEET . 1
34 X 44"

ESHEET . 2
44 X 34"

Atmel's DIO Primitives, Sheet 3 of 4



Atmel's DIO Primitives, Sheet 4 of 4

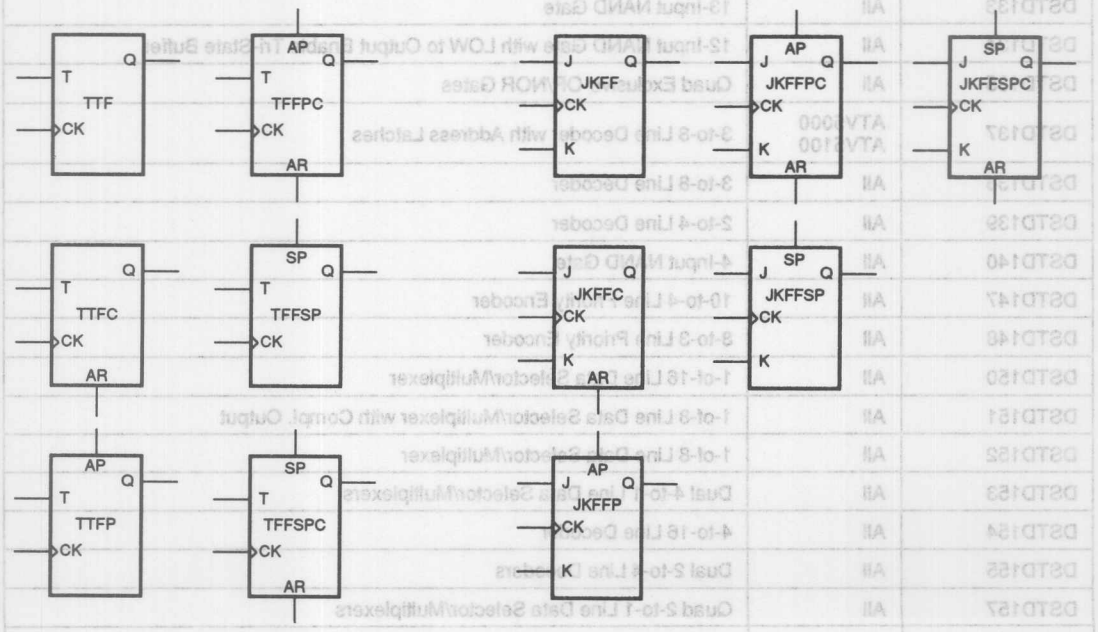


Table 3. DSTD TTL Symbols

Component	Device Supported	Function Description
DSTD00	All	2-Input NAND Gate
DSTD02	All	2-Input NOR Gate
DSTD04	All	Inverter
DSTD08	All	2-Input AND Gate
DSTD10	All	3-Input NAND Gate
DSTD107	All	JK Flip-Flop with Async. Clear
DSTD109	All	JK Flip-Flop with Async. Preset and Clear
DSTD11	All	3-Input AND Gate
DSTD112	ATV5000 ATV5100	JK Flip-Flop (Negative-Edge Triggered) with Async. Preset and Clear
DSTD113	ATV5000 ATV5100	JK Flip-Flop (Negative-Edge Triggered) with Async. Preset
DSTD114	ATV5000 ATV5100	Dual JK Flip-Flops (Negative-Edge Triggered) with Async. Preset, Common Clear, and Common Clock
DSTD125	All	Tri-State Buffer with LOW to OE
DSTD126	All	Tri-State Buffer with HIGH to OE
DSTD128	All	2-Input NOR Gate
DSTD133	All	13-Input NAND Gate
DSTD134	All	12-Input NAND Gate with LOW to Output Enable Tri-State Buffer
DSTD135	All	Quad Exclusive-OR/NOR Gates
DSTD137	ATV5000 ATV5100	3-to-8 Line Decoder with Address Latches
DSTD138	All	3-to-8 Line Decoder
DSTD139	All	2-to-4 Line Decoder
DSTD140	All	4-Input NAND Gate
DSTD147	All	10-to-4 Line Priority Encoder
DSTD148	All	8-to-3 Line Priority Encoder
DSTD150	All	1-of-16 Line Data Selector/Multiplexer
DSTD151	All	1-of-8 Line Data Selector/Multiplexer with Compl. Output
DSTD152	All	1-of-8 Line Data Selector/Multiplexer
DSTD153	All	Dual 4-to-1 Line Data Selector/Multiplexers
DSTD154	All	4-to-16 Line Decoder
DSTD155	All	Dual 2-to-4 Line Decoders
DSTD157	All	Quad 2-to-1 Line Data Selector/Multiplexers
DSTD158	All	Quad 2-to-1 Line Data Selector/Multiplexers with Compl. Output

Table 3. DSTD TTL Symbols (continued)

Component	Device Supported	Function Description
DSTD160	All	Sync. 4-Bit Decade Counter with Async. Clear
DSTD161	All	Sync. 4-Bit Binary Counter with Async. Clear
DSTD162	All	Sync. 4-Bit Decade Counter with Sync. Clear
DSTD163	All	Sync. 4-Bit Binary Counter with Sync. Clear
DSTD164	ATV5000 ATV5100	8-Bit Serial In/Parallel Out Shift Register with Async. Clear
DSTD165	ATV5000 ATV5100	8-Bit Parallel In/Serial Out Shift Register with Compl. Output
DSTD168	All	Synchronous 4-Bit Up/Down Decade Counter
DSTD169	All	Synchronous 4-Bit Up/Down Binary Counter
DSTD174	All	Hex D Flip-Flops with Async. Clear
DSTD175	All	Quad D Flip-Flops with Async. Clear and Compl. Output
DSTD176	ATV5000 ATV5100	4-Bit Presetable Decade Counter
DSTD177	ATV5000 ATV5100	4-Bit Presetable Binary Counter
DSTD180	All	9-Bit Parity Generator/Checker
DSTD181	ATV5000 ATV5100	Arithmetic Logic Unit/Function Generator
DSTD182	All	Look-Ahead Carry Generator
DSTD183	All	Carry-Save Full Address
DSTD190	ATV5000 ATV5100	Sync. 4-Bit Up/Down Decade Counter with Mode Control
DSTD191	ATV5000 ATV5100	Synchronous 4-Bit Up/Down Binary Counter with Mode Control
DSTD192	ATV5000 ATV5100	Synchronous 4-Bit Up/Down Decade Counter with Dual Clock
DSTD194	All	4-Bit Bidirectional Universal Shift Register
DSTD196	ATV5000 ATV5100	4-Bit Presettable Decade Counter
DSTD197	ATV5000 ATV5100	4-Bit Presettable Binary Counter
DSTD198	All	8-Bit Bidirectional Universal Shift Register
DSTD20	All	4-Input NAND Gate
DSTD21	All	4-Input AND Gate
DSTD226	ATV5000 ATV5100	4-Bit Parallel Latched Bus Tranceivers

Table 3. DSTD TTL Symbols (continued)

Component	Device Supported	Function Description
DSTD23	All	Dual 4-Input NOR Gates with Strobe
DSTD237	All	3-to-8 Line Decoder with Address Latches
DSTD240	All	Quad Tri-State Inverting Buffers
DSTD241	All	Octal Tri-State Buffers
DSTD242	All	Quad Tri-State Inverting Bus Transceivers
DSTD243	All	Quad Tri-State Bus Transceivers
DSTD244	All	Octal Tri-State Buffers
DSTD245	All	Octal Tri-State Bus Transceivers
DSTD25	All	4-Input NOR Gate with Strobe
DSTD251	All	Tri-State 1-to-8 Line Data Selector/Multiplexer with Compl. Output
DSTD253	All	Dual Tri-State 1-to-4 Multiplexers
DSTD257	All	Quad Tri-State 2-to-1 Multiplexers
DSTD258	All	Quad Tri-State 2-to-1 Inverting Multiplexers
DSTD260	All	5-Input NOR Gate
DSTD27	All	3-Input NOR Gate
DSTD273	All	Octal D Flip-Flops with Clear and Buffer Outputs
DSTD279	All	Dual SR Latches
DSTD28	All	2-Input NOR Buffer
DSTD280	All	9-Bit Odd/Even Parity Generators/Checkers
DSTD283	All	4-Bit Binary Full Adders with Fast Carry
DSTD290	All	Decade Counter
DSTD293	All	4-Bit Binary Counter
DSTD295	All	4-Bit Right/Left Shift Registers with Tri-State Outputs
DSTD298	All	Quad 2-Input Multiplexers with Storage
DSTD299	All	8-Bit Universal Shift/Storage Registers
DSTD30	All	8-Input NAND Gate
DSTD31	All	Delay Elements
DSTD32	All	2-Input OR Gate
DSTD323	All	8-Bit Universal Shift/Storage Registers
DSTD348	All	8-to-3 Line Priority Encoders with Tri-State Outputs
DSTD353	All	Dual 4-to-1 Line Data Selectors/Multiplexers with Tri-State Outputs
DSTD354	ATV5000 ATV5100	8-to-1 Multiplexer/Register (Transparent)

Table 3. DSTD TTL Symbols (continued)

Component	Device Supported	Function Description
DSTD356	All	8-to-1 Multiplexer/Register (Edge-Triggered)
DSTD365	All	Hex Bus Drivers with Tri-State Outputs
DSTD366	All	Hex Inverting Bus Drivers with Tri-State Outputs
DSTD367	All	Hex Bus Drivers with Tri-State Outputs with Two Tri-State Controls
DSTD368	All	Hex Inverting Bus Drivers with Tri-State Outputs with Two Tri-State Controls
DSTD37	All	2-Input NAND Buffers
DSTD373	ATV5000 ATV5100	Octal Transparent D Latches
DSTD374	All	Octal Edge-Triggered D Flip-Flops
DSTD376	All	Quad JK Flip-Flops
DSTD377	All	Octal D Flip-Flops with Enable
DSTD378	All	Hex D Flip-Flops with Enable
DSTD379	All	Quad D Flip-Flops with Enable
DSTD390	All	4-Bit Decade Counter
DSTD393	All	4-Bit Binary Counter
DSTD398	All	Quad 2-Input Multiplexer with Storage
DSTD399	All	Quad 2-Input Multiplexer with Storage
DSTD40	All	4-Input NAND Buffers
DSTD4002	All	4-Input NOR Gate
DSTD4016	All	Bilateral Switch
DSTD4017	All	Decade Counter/Divider
DSTD4020	All	14-Stage Ripple-Carry Binary Counter/Divider
DSTD4024	All	7-Stage Ripple-Carry Binary Counter/Divider
DSTD4040	All	12-Stage Ripple-Carry Binary Counter/Divider
DSTD4049	All	Inverting Buffer
DSTD4066	All	Bilateral Switch
DSTD4075	All	3-Input OR Gate
DSTD4078	All	8-Input NOR Gate with Compl. Output
DSTD42	All	BCD to Decimal Decoder
DSTD4514	ATV5000 ATV5100	8-Bit Static Shift Register
DSTD51	All	Dual 2-Wide 2-Input AND-OR-INVERT Gates
DSTD520	All	Octal 8-Bit Identity Comparator

Table 3. DSTD TTL Symbols (continued)

Component	Device Supported	Function Description
DSTD521	All	Octal 8-Bit Identity Comparator
DSTD533	ATV5000 ATV5100	Octal Tri-State Inverting Transparent D Latches
DSTD534	All	Octal Tri-State Inverting Edge-Triggered D Flip-flops
DSTD538	All	3-to-8 Line Decoders with Tri-State Outputs
DSTD54	All	4-Wide 2-Input AND-OR-INVERT Gates
DSTD540	All	Octal Buffers with Tri-State Outputs
DSTD541	All	Octal Inverting Buffers with Tri-State Outputs
DSTD55	All	2-Wide 4-Input AND-OR-INVERT Gates
DSTD563	ATV5000 ATV5100	Octal Tri-State Inverting Transparent D Latches
DSTD564	All	Octal Tri-State Inverting Edge-Triggered D Flip-Flops
DSTD568	All	Synchronous 4-Bit Up/Down Decade Counter with Tri-State Outputs
DSTD569	All	Synchronous 4-Bit Up/Down Binary Counter with Tri-State Outputs
DSTD573	ATV5000 ATV5100	Octal Tri-State Transparent D Latches
DSTD574	All	Octal Tri-State Edge-Triggered D Flip-Flops
DSTD575	All	Octal Tri-State Edge-Triggered D Flip-Flops with Sync. Clear
DSTD576	All	Octal Tri-State Inverting Edge-Triggered D Flip-Flops
DSTD580	ATV5000 ATV5100	Octal Tri-State Inverting Transparent D Latches
DSTD623	All	Octal Tri-State Bus Transceivers
DSTD638	All	Octal Inverting Bus Transceivers with Tri-State and Open-Collector Outputs
DSTD64	All	4-2-3-2-Input AND-OR-INVERT Gates
DSTD640	All	Octal Tri-State Inverting Bus Transceivers
DSTD643	All	Octal Tri-State True and Inverting Bus Transceivers
DSTD645	All	Octal Tri-State Bus Transceivers
DSTD646	All	Octal Bus Transceivers and Registers with AllTri-State Outputs
DSTD652	All	Octal Bus Transceivers and Registers
DSTD668	All	Synchronous 4-Bit Up/Down Decade Counters
DSTD669	All	Synchronous 4-Bit Up/Down Binary Counters
DSTD670	ATV5000 ATV5100	4-by-4 Register Files with Tri-State Outputs
DSTD677	All	16-to-4 Bit Address Comparator with Enable
DSTD684	All	8-Bit Magnitude/Identity Comparator

Table 3. DSTD TTL Symbols (continued)

Component	Device Supported	Function Description
DSTD688	All	8-Bit Identity Comparator
DSTD70	ATV5000 ATV5100	AND-Gated Edge-Triggered JK Flip-Flop with Async. Preset and Clear
DSTD73	ATV5000 ATV5100	JK Flip-Flop with Async. Clear
DSTD74	ATV5000 ATV5100	D Flip-Flop (Edge-Triggered) with Async. Preset and Clear
DSTD75	ATV5000 ATV5100	4-Bit Bistable Latches
DSTD76	ATV5000 ATV5100	JK Flip-Flop with Async. Preset and Clear
DSTD77	ATV5000 ATV5100	Dual Transparent D Latches
DSTD78	ATV5000 ATV5100	Dual JK Flip-Flops (Edge-Triggered) with Async. Preset, Common Clear, and Common Clock
DSTD80	All	Gated Full Adders
DSTD804	All	2-Input NAND Line Driver
DSTD805	All	2-Input NOR Line Driver
DSTD808	All	2-Input AND Line Driver
DSTD82	All	2-Bit Binary Full Adders
DSTD83	All	4-Bit Binary Full Adders with Fast Carry
DSTD832	All	2-Input OR Line Driver
DSTD85	All	4-Bit Magnitude Comparators
DSTD857	All	Hex 2-to-1 Universal Multiplexers
DSTD86	All	2-Input Exclusive-OR Gate
DSTD867	All	Synchronous 8-Bit Up/Down Counter with Async. Clear
DSTD869	All	Synchronous 8-Bit Up/Down Counter with Sync. Clear
DSTD874	All	4-Bit Edge-Triggered D Flip-Flop
DSTD878	All	4-Bit Edge-Triggered D Flip-Flop with Tri-State Outputs
DSTD882	All	32-Bit Look-Ahead Carry Generators
DSTD90	All	Decade Counter
DSTD91	All	8-Bit Shift Registers
DSTD92	All	Divide-by-12 Counter
DSTD93	All	4-Bit Binary Counter
DSTD94	ATV5000 ATV5100	4-Bit Shift Registers

Table 3. DSTD TTL Symbols (continued)

Component	Device Supported	Function Description
DSTD96	ATV5000 ATV5100	5-Bit Shift Registers
DSTDK	All	2-Input NAND Gate
DSTDK2	All	2-Input NOR Gate
DSTDK4	All	Inverter
DSTDK8	All	2-Input AND Gate
DSTD34	All	Buffer
DSTDK34	All	Buffer

Glossary

Term	Description
Async.	Asynchronous
Sync.	Synchronous
Compl.	Complementary

ATH3000 Application Example: Registered Bus Multiplexer

Introduction

This application note shows how an ATH3000 programmable logic device can be used to implement a simple, high-speed 16-bit bus multiplexer. It provides an example of how a bus multiplexer can be created and how to use the ATH3000. Included are a description of the bus multiplexer function, the implementation using an ATH3000, and the ABEL™ source code which was created for this application.

In a typical CPU system, multiple peripheral devices, such as floppy disks, keyboard or CRT controllers, printer interfaces, and D/A or A/D converters, are interfaced to the CPU. A bus multiplexer provides a bi-directional interface between a CPU system data bus and peripheral device data buses. In this example, two peripheral device data buses can be interfaced to the CPU data bus. Data can be read from either one of the peripheral device buses onto the CPU bus, or written from the CPU bus to one of the two peripheral device buses. The control signals which are used by the CPU to perform a data transfer are decoded and used to determine which peripheral is being accessed and whether it is a read or write operation.

The ATH3000 is the smallest member of the Atmel H-Series high throughput programmable logic devices. It is a 68-pin device which features 56 I/O logic cells. The architecture is simple and regular, providing predictable, high-speed performance. This application requires a high I/O count and fast timing so that the bus transfers are not hindered by the PLD performance. The ATH3000 offers both.

Bus Multiplexer Description

The bus multiplexer provides an interface between a CPU system data bus and peripheral device data buses. This interface simplifies the timing between the buses and allows the CPU to read data from or to write data to the various peripherals, without requiring those devices to be hooked directly to the CPU data bus. The bus multiplexer is transparent to the CPU. It decodes the control signals which are generated by the CPU to perform a data transfer.

Figure 1 shows the basic block diagram for the bus multiplexer. This example interfaces three 16-bit buses. The Data I/O port is the interface to the CPU system data bus. Port A and Port B are interfaces for two different peripheral devices. The direction and port select are decoded from the CPU control signals which are used to perform a data transfer. This example uses five control signals: CS_ (chip select), RD_ (read), WR_ (write), AB_ (A/B select), and RST (reset). These signals are used to determine whether the bus multiplexer is being addressed, and what type of transfer is requested. Table 1 shows the device functions.

The CS_ signal is used to determine whether the control signals should be decoded by the multiplexer. If the chip select is not asserted, the data bus outputs are tri-stated, so the bus multiplexer will not interfere with other bus activity. Any read or write signals are also ignored if the chip select is not asserted. If both the RD_ and WR_ signals are high, the data bus outputs are also tri-stated.

Figure 1. 16-Bit Bus Multiplexer Block Diagram

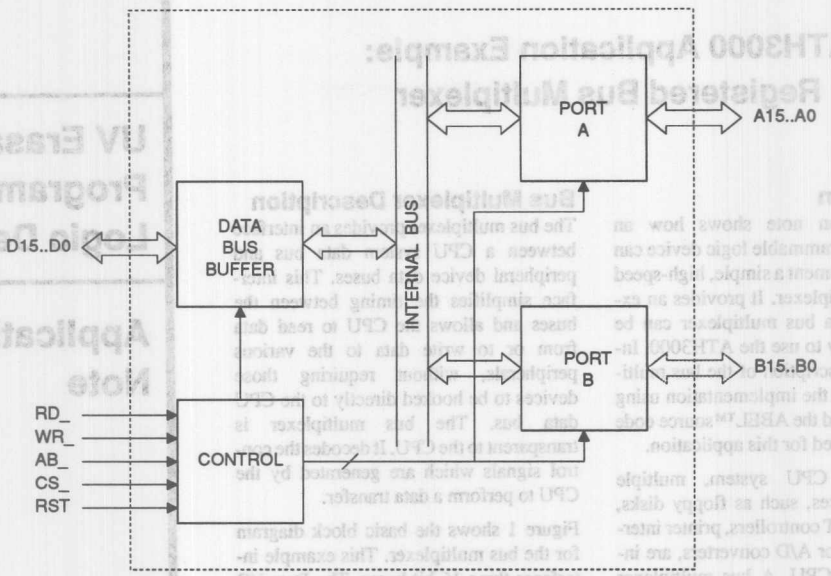


Table 1. Control Signal Functions

CS_	RD_	WR_	AB_	RST	Function
1	X	X	X	X	Data I/O Port Tri-Stated
0	1	1	X	0	Data I/O Port Tri-Stated
0	0	1	1	0	Read – Port A → Data I/O Port
0	0	1	0	0	Read – Port B → Data I/O Port
0	1	0	1	0	Write – Data I/O Port → Port A
0	1	0	0	0	Write – Data I/O Port → Port B
0	0	0	X	X	Not Allowed
0	X	X	X	1	Reset Registers, Disable Ports A and B for Read

Bus Multiplexer Description (continued)

Figure 2 shows the timing for a read operation. In a read mode, data is read from either Port A or Port B, selected by AB_. The outputs of the selected port are tri-stated, so that the peripheral devices may drive the bus. The data is input to the bus-multiplexer and registered using the falling edge of RD_. The data is then available on the data bus until the rising edge of the read signal.

Figure 3 shows the timing for a write operation. In a write mode, data is written to either Port A or Port B from the CPU data bus. The data bus is tri-stated and the port which is selected by AB_ is enabled. The data is input to the bus multiplexer and registered using the rising edge of WR_ signal. The data is available until the next write signal. The outputs of the port will remain enabled until RST is received.

RST will reset all data registers and will disable the Port A and Port B outputs, preparing for the next write cycle.

In this example, general-purpose control signals are used to demonstrate the function. For interface to a specific CPU, the application could be tailored to decode the signals generated by that CPU. For example, an interface to an Intel 386™ processor could be designed by changing the bus multiplexer application to decode the W/R, D/C, M/IO, ADS, and READY signals.

Figure 2. 16-Bit Bus Multiplexer: Read Mode Timing

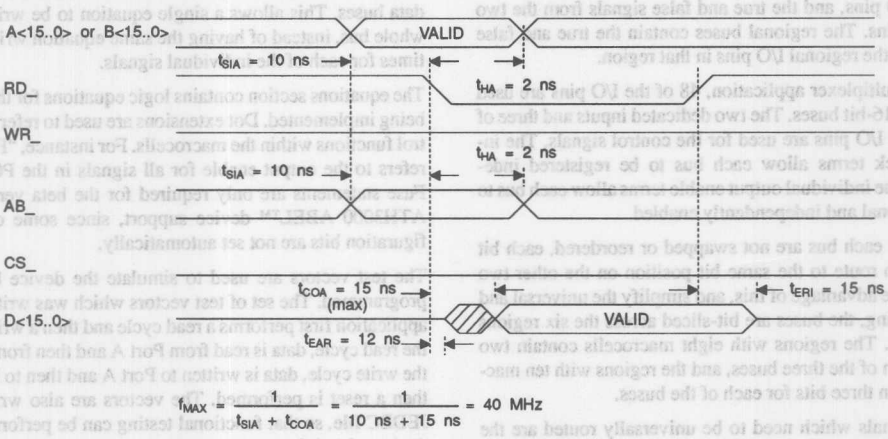
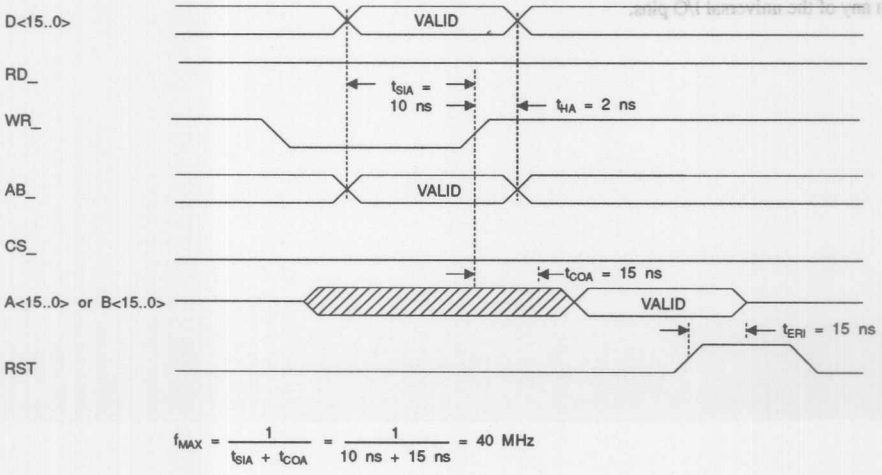


Figure 3. 16-Bit Bus Multiplexer: Write Mode Timing



ATH3000 Description

The ATH3000 is 68-pin high-speed programmable logic device, which features 56 I/O pins and two input-only pins. Each I/O pin can be driven by a logic macrocell which has one flip-flop, six product terms, a clock term, and an output enable term.

The macrocells are divided into six regions – two regions with eight macrocells each, and four regions with ten macrocells each. The regions with eight macrocells have one universal I/O pin each, and the regions with ten macrocells have three universal I/O pins each. An additional eight CABLE (Complement Array Buried Logic Extender) terms are provided, which can be used for logic expansion or routing.

A universal bus routes signals to all six regions, and a regional bus routes signals within each region. The universal bus contains the eight CABLE terms, the true and false signals from universal I/O pins, and the true and false signals from the two input-only pins. The regional buses contain the true and false signals from the regional I/O pins in that region.

In the bus multiplexer application, 48 of the I/O pins are used for the three 16-bit buses. The two dedicated inputs and three of the universal I/O pins are used for the control signals. The individual clock terms allow each bus to be registered independently. The individual output enable terms allow each bus to be bi-directional and independently enabled.

Since bits on each bus are not swapped or reordered, each bit only needs to route to the same bit position on the other two buses. To take advantage of this, and simplify the universal and regional routing, the buses are bit-sliced across the six regions in the device. The regions with eight macrocells contain two bits from each of the three buses, and the regions with ten macrocells contain three bits for each of the buses.

The only signals which need to be universally routed are the control signals. The dedicated input pins are used for the RD_ and WR_ signals, and three universal I/O pins are used for the CS_, AB_, and RST signals. Since they are universally routed, they can go on any of the universal I/O pins.

Because of its simple and regular architecture, the ATH3000 offers predictable, high-speed performance. The application is designed to allow the CPU and peripherals to control the timing. Figures 2 and 3 show the maximum delays for read and write cycles. The ATH3000 will allow a read or write bus cycle rate of up to 40 MHz.

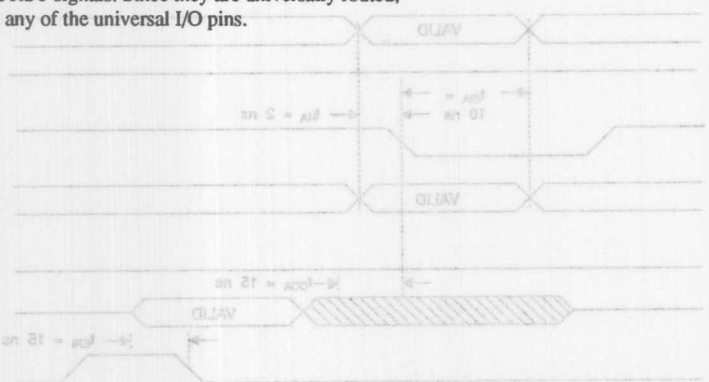
ABEL™ Source Code

A listing of the ABEL™ source code is included for reference, and the file is also available on floppy disk from Atmel. The ABEL™ source code is divided into three basic sections: declarations, equations, and test vectors.

The declarations section includes a device type declaration and the pin and node number assignments. For the ATH3000, the device type is "H3000." The I/O signals are assigned to pins and declared as registered by using an "istype" statement. Also included in the declarations section are set declarations for the data buses. This allows a single equation to be written for the whole bus, instead of having the same equation written sixteen times for each of the individual signals.

The equations section contains logic equations for the functions being implemented. Dot extensions are used to refer to the control functions within the macrocells. For instance, "PORTA.oe" refers to the output enable for all signals in the PORTA bus. Fuse statements are only required for the beta version of the ATH3000 ABEL™ device support, since some of the configuration bits are not set automatically.

The test vectors are used to simulate the device before it is programmed. The set of test vectors which was written for this application first performs a read cycle and then a write cycle. In the read cycle, data is read from Port A and then from Port B. In the write cycle, data is written to Port A and then to Port B, and then a reset is performed. The vectors are also written to the JEDEC file, so that functional testing can be performed on the device when it is programmed.



ABEL™ Source Code

```
module BUSMUX ;
title 'Simple 16-bit Bus Multiplexer - Demo ATH3000
ATMEL Corporation EPLD - Applications Hotline: (408)436-4333
Wendey Mueller - May 1, 1992'

BUSMUX device 'H3000';

RD_,WR_,CS_,AB_      pin 1,35,61,2;
RST                  pin 53;
D0,D1,D2,D3,D4,D5    pin 5,6,7,8,9,12      istype 'reg_d,buffer';
D6,D7,D8,D9,D10,D11  pin 13,14,18,19,21,24 istype 'reg_d,buffer';
D12,D13,D14,D15      pin 25,26,29,30       istype 'reg_d,buffer';
A0,A1,A2,A3,A4,A5    pin 63,64,10,11,58,15 istype 'reg_d,buffer';
A6,A7,A8,A9,A10,A11  pin 17,52,22,23,46,28 istype 'reg_d,buffer';
A12,A13,A14,A15      pin 41,42,31,32       istype 'reg_d,buffer';
B0,B1,B2,B3,B4,B5    pin 65,66,59,60,62,55 istype 'reg_d,buffer';
B6,B7,B8,B9,B10,B11  pin 56,57,47,48,49,43 istype 'reg_d,buffer';
B12,B13,B14,B15      pin 44,45,39,40       istype 'reg_d,buffer';
PORT_OE              pin 51                istype 'reg_d,buffer';

C,K,X,Z,U,D = .C.,.K.,.X.,.Z.,.U.,.D.;


DIO   = [D15..D0];      "Data I/O Port (interface to CPU)
PORTA = [A15..A0];      "Port A (interface to peripheral)
PORTB = [B15..B0];      "Port B (interface to peripheral)

EQUATIONS

"*********************************************************************
"This is an example of a 16-bit bidirectional bus multiplexer.
"It could be used to interface a system data bus to two different
"peripheral devices. Each of the 16-bit ports is bidirectional.
"The functional control is as follows:
"
"  RD_ WR_ AB_ CS_ RST  FUNCTION
"  ----------------------------------------
"   X   X   X   1   0   Data I/O port 3-state
"   1   1   X   0   0   Data I/O port 3-state
"   0   1   1   0   0   port A - Data I/O port (read)
"   0   1   0   0   0   port B - Data I/O port (read)
"   1   0   1   0   0   Data I/O port - port A (write)
"   1   0   0   0   0   Data I/O port - port B (write)
"   X   X   X   X   1   Reset regs, disable ports A and B for read
"*********************************************************************


PORT_OE.d  = 1;             "This bit controls Port A and B output
PORT_OE.ck = !CS_ & !WR_;   "enables. Once write cycle is started,
PORT_OE.ar = RST;           "ports will remain enabled until a RST is
                            "received. RST is required before next read.

DIO.d   = (!RD_ & AB_ & PORTA)   "DIO port data for read is selected
        # (!RD_ & !AB_ & PORTB); "from either Port A or Port B
DIO.oe   = !CS_ & !RD_;        "DIO port is tri-stated except during read
DIO.ck   = !CS_ & !RD_;        "clock Data I/O port for read
DIO.ar   = RST;                "reset registers with RST signal

PORTA.d = DIO ;                "Port A data for write
PORTA.oe = PORT_OE;            "output will remain enabled until reset
PORTA.ck = !CS_ & WR_ & AB_;   "clock port A registers for write to A
PORTA.ar = RST;                "reset registers with RST signal
```

```
PORTB.d = DIO ;                 "Port B data for write
PORTB.oe = PORT_OE;             "output will remain enabled until reset
PORTB.ck = !CS_ & WR_ & !AB_;   "clock port B registers for write to B
PORTB.ar = RST;                 "reset registers with RST signal

"Fuses statements are only required for beta level version of the
"H3000 software support.

FUSES  "These fuses select the feedback/input pin path
       " 0 means register feedback.
       " 1 means pin feedback/input pin.

"pin   2,    4,    5,    6,    7,    8,    9,    10
  [25923,25931,25939,25947,25955,25963,25971,25979]
= [    1,    1,    1,    1,    1,    1,    1,    1];

"pin  11,   12,   13,   14,   15,   17,   18,   19
  [25987,25995,26003,26011,26019,26027,26035,26043]
= [    1,    1,    1,    1,    1,    1,    1,    1];

"pin  21,   22,   23,   24,   25,   26,   27,   28
  [26051,26059,26067,26075,26083,26091,26099,26107]
= [    1,    1,    1,    1,    1,    1,    1,    1];

"pin  29,   30,   31,   32,   36,   38,   39,   40
  [26115,26123,26131,26139,26147,26155,26163,26171]
= [    1,    1,    1,    1,    1,    1,    1,    1];

"pin  41,   42,   43,   44,   45,   46,   47,   48
  [26179,26187,26195,26203,26211,26219,26227,26235]
= [    1,    1,    1,    1,    1,    1,    1,    1];

"pin  49,   51,   52,   53,   55,   56,   57,   58
  [26243,26251,26259,26267,26275,26283,26291,26299]
= [    1,    1,    1,    1,    1,    1,    1,    1];

"pin  59,   60,   61,   62,   63,   64,   65,   66
  [26307,26315,26323,26331,26339,26347,26355,26363]
= [    1,    1,    1,    1,    1,    1,    1,    1];

FUSES  "These fuses select the clock options.
       " 0 means use synchronous chip clock.
       " 1 means use asynchronous clock.
"JLCC pinout
"pin   2,    4,    5,    6,    7,    8,    9,    10
  [25926,25934,25942,25950,25958,25966,25974,25982]
= [    1,    1,    1,    1,    1,    1,    1,    1];

"pin  11,   12,   13,   14,   15,   17,   18,   19
  [25990,25998,26006,26014,26022,26030,26038,26046]
= [    1,    1,    1,    1,    1,    1,    1,    1];

"pin  21,   22,   23,   24,   25,   26,   27,   28
  [26054,26062,26070,26078,26086,26094,26102,26110]
= [    1,    1,    1,    1,    1,    1,    1,    1];

"pin  29,   30,   31,   32,   36,   38,   39,   40
  [26118,26126,26134,26142,26150,26158,26166,26174]
= [    1,    1,    1,    1,    1,    1,    1,    1];

"pin  41,   42,   43,   44,   45,   46,   47,   48
  [26182,26190,26198,26206,26214,26222,26230,26238]
= [    1,    1,    1,    1,    1,    1,    1,    1];
```

```
"pin  49,   51,   52,   53,   55,   56,   57,   58
  [26246,26254,26262,26270,26278,26286,26294,26302]
= [    1,    1,    1,    1,    1,    1,    1,    1];

"pin  59,   60,   61,   62,   63,   64,   65,   66
  [26310,26318,26326,26334,26342,26350,26358,26366]
= [    1,    1,    1,    1,    1,    1,    1,    1];

@RADIX 16;

TEST VECTORS (
 [RST,RD_,WR_,AB_,CS_,PORTA,PORTB ] -> [DIO ]);
 [ 0,   0,   0,   0,   1,   X,     X     ] -> [Z    ]; "dio port disabled
 [ 1,   1,   1,   1,   0,   0000,  0000  ] -> [Z    ]; "reset
 [ 0,   C,   1,   1,   0,   0000,  0000  ] -> [0000]; "read from A port
 [ 0,   C,   1,   1,   0,   1111,  0000  ] -> [1111]; "read from A port
 [ 0,   C,   1,   1,   0,   2222,  0000  ] -> [2222]; "read from A port
 [ 0,   C,   1,   1,   0,   3333,  0000  ] -> [3333]; "read from A port
 [ 0,   C,   1,   0,   0,   0000,  4444  ] -> [4444]; "read from B port
 [ 0,   C,   1,   0,   0,   0000,  5555  ] -> [5555]; "read from B port
 [ 0,   C,   1,   0,   0,   0000,  6666  ] -> [6666]; "read from B port
 [ 0,   C,   1,   0,   0,   0000,  7777  ] -> [7777]; "read from B port
 [ 0,   1,   1,   0,   0,   0000,  0000  ] -> [Z    ]; "dio port disabled

TEST_VECTORS (
 [RST,RD_,WR_,AB_,CS_,DIO  ] -> [PORTA,PORTB])
 [ 1,   1,   1,   1,   0,   0000] -> [Z,     Z     ]; "reset
 [ 0,   1,   K,   1,   0,   0000] -> [0000,  0000  ]; "write to A port
 [ 0,   1,   K,   1,   0,   1111] -> [1111,  0000  ]; "write to A port
 [ 0,   1,   K,   1,   0,   2222] -> [2222,  0000  ]; "write to A port
 [ 0,   1,   K,   1,   0,   3333] -> [3333,  0000  ]; "write to A port
 [ 0,   1,   K,   0,   0,   4444] -> [3333,  4444  ]; "write to B port
 [ 0,   1,   K,   0,   0,   5555] -> [3333,  5555  ]; "write to B port
 [ 0,   1,   K,   0,   0,   6666] -> [3333,  6666  ]; "write to B port
 [ 0,   1,   K,   0,   0,   7777] -> [3333,  7777  ]; "write to B port
 [ 1,   1,   1,   0,   0,   8888] -> [Z,     Z     ]; "reset

END ;
```



ATV5000 Application Example: DMA Controller

UV Erasable Programmable Logic Device

Application Note

7

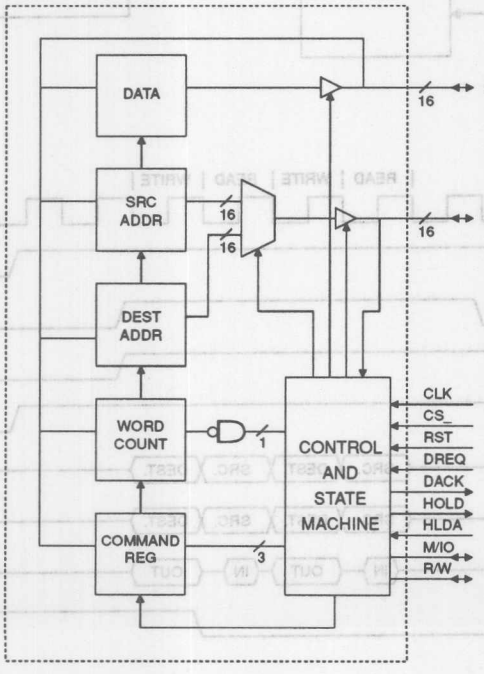
Introduction

This application note shows how the ATV5000 complex programmable logic device can be used to implement a simple DMA Controller. It includes a description of the DMA controller function and the implementation using an ATV5000. The ABEL™ source code is included for reference, and is also available from the factory on floppy disk.

A Direct Memory Access (DMA) controller is a peripheral device used in a CPU system to perform block data transfers between memories and I/O devices. It generates the addresses and control necessary to perform the transfer. The DMA controller improves system performance by transferring data directly between devices instead of using the CPU.

The ATV5000 is a high-density programmable logic device, featuring 52 I/O logic cells and 128 flip-flops. This application takes advantage of the buried registers to store and increment or decrement the addresses and word count. The counters are easily implemented with minimal logic by using T-type registers. The high I/O count can easily accommodate the 16-bit bi-directional data and address buses.

Figure 1. Internal Block Diagram



DMA Controller Description

The DMA controller is used to transfer blocks of data between system memory and other memory or I/O devices. Figure 1 shows the basic block diagram for the DMA controller. The interface to the CPU consists of an address bus, a data bus, and some control signals. These signals are used by the CPU to load initialization data into the DMA controller registers. When the DMA controller is granted control of the buses, the same signals are used to transfer the data. This example uses i386™ type bus control signals. Figure 2 shows how this DMA controller would be used in a CPU system.

The transfer is initiated when the CPU loads the starting source and destination addresses, word count, and control word into the DMA controller registers. The external device asserts the DMA request signal to request a DMA. The DMA controller then requests control of the system buses and control signals. When the CPU grants the bus request, the DMA controller acknowledges the DMA request and starts the DMA.

The data is read in on the data bus and then latched and written back out. The source address or destination address is multiplexed onto the address bus during the read cycle or write cycle. The system bus control signals are used by the DMA controller as control signals for the memory or I/O device. The DMA controller transfers the requested number of words and then relinquishes bus control. The DMA cycle timing is shown in Figure 3.

Figure 2. System Block Diagram

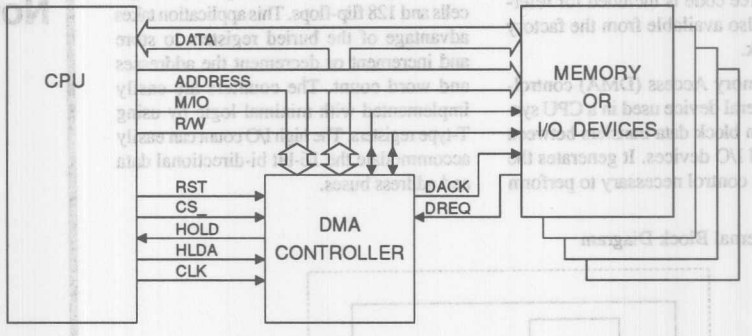
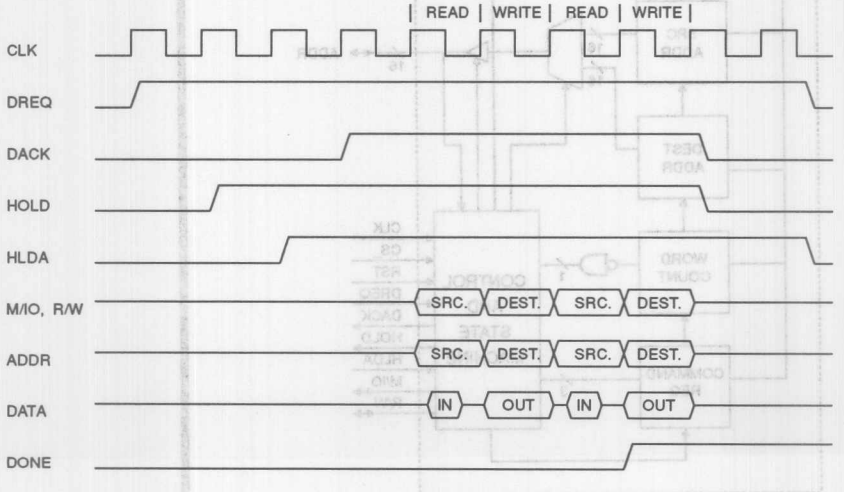


Figure 3. DMA Timing



ATV5000 Description

The ATV5000 is 68-pin high-density programmable logic device, which features 52 I/O pins and eight input-only pins. Each I/O pin is associated with a logic macrocell (see Figures 4, 5, and 6). Each macrocell has an input latch, two flip-flops, 13 product terms which can be split into three separate sum terms, and an output enable term. The I/O pin can be driven with either a combinatorial or registered output. Each flip-flop has a clock term, asynchronous reset term, and asynchronous preset term, and can be configured as either a D-type or T-type flip-flop.

In addition, there are 24 buried logic cells (see Figure 7). Each buried logic cell can be configured as registered or combinatorial. If registered, each flip-flop has a clock term, asynchronous reset term, and synchronous preset term, and can be configured as a D-type or T-type flip-flop.

The ATV5000 is divided into four quadrants with 13 I/O macrocells and six buried logic cells each (see Figure 8). A universal bus routes signals to all four quadrants, and a regional bus routes signals within each quadrant. The regional buses contain the true and false feedback signals from each register, from the buried logic cells, and from the eight input-only pins. The universal bus contains the regional bus inputs plus the true and false signals from each I/O pin.

Figure 4. Logic Cell, Two Buried Registers, Combinatorial to I/O Cell

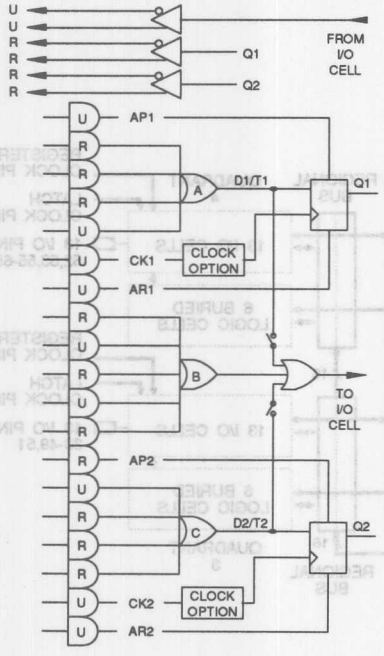
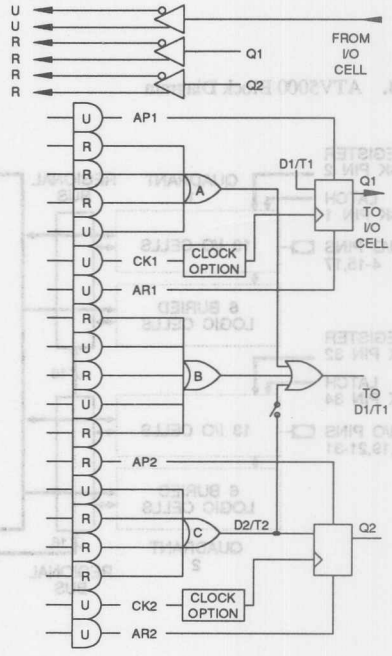


Figure 5. Logic Cell with Combinatorial Sum Terms, Register to I/O Cell



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Figure 6. I/O Pin Logic

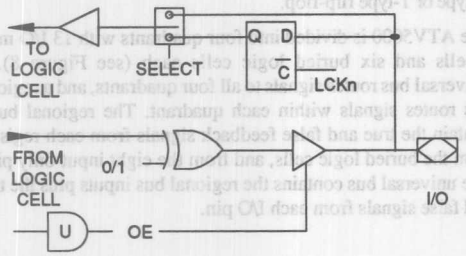


Figure 7. Buried Logic Cells

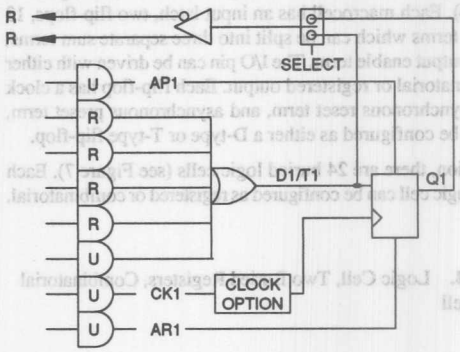
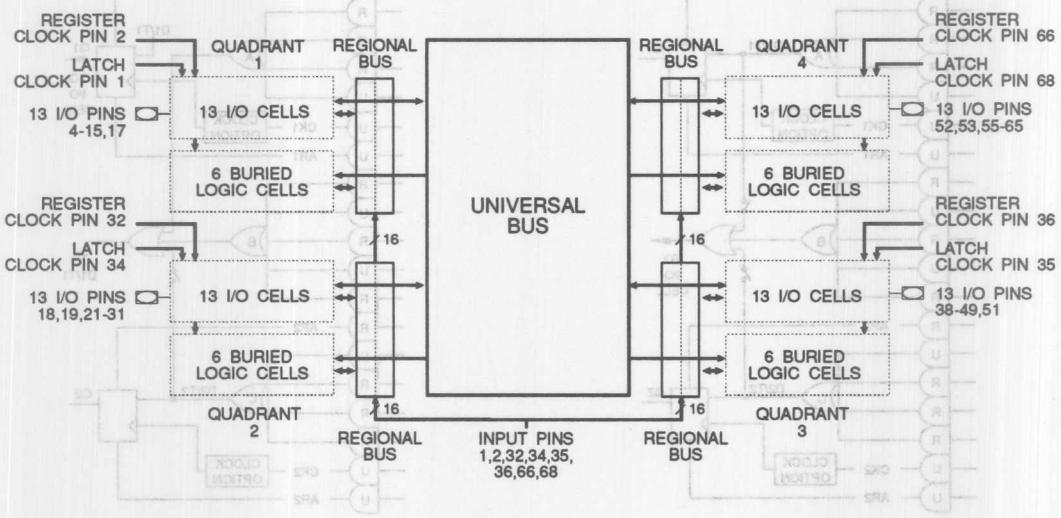


Figure 8. ATV5000 Block Diagram



DMA Controller Implementation

The DMA controller consists of three basic functions: system interface, internal address and word counters, and a state machine controller.

System Interface

The system interface consists of a 16-bit bi-directional data bus, a 16-bit bi-directional address bus, bi-directional bus control signals, and handshaking signals to request bus control.

The data and address buses are assigned to I/O pins in the ATV5000. When the CPU controls the system buses, the buses are used as inputs to receive initialization data. When the DMA controller controls the system buses, the buses are bi-directional. The data bus is tri-stated while the source data is read and registered, and then enabled to write the data to the destination. The address bus outputs are enabled and multiplex the source or destination address onto the bus.

The CLK and RST signals are the CPU system clock and reset signals. The CLK signal is used as the clock for all registers, so that all data transfers are synchronized to the system clock. The CS_ selects whether the DMA controller is being addressed for initialization. Both signals are assigned to input pins in the ATV5000, so that the signals are available on the regional buses in all quadrants.

The M/IO and R/W signals are used to control the bus activity. For initialization, the R/W signal enables a write and the LSB bits of the address bus are decoded to select which register is to be accessed. During a DMA transfer, the M/IO selects the source or destination as an I/O device or a memory and the R/W signal selects either a read or write operation. Both signals are assigned to I/O pins in the ATV5000, since they are used as inputs during initialization and outputs during a DMA cycle.

There are two sets of handshaking signals: the DMA request and acknowledge (DREQ and DACK), and the bus request and acknowledge (HOLD and HLDA). The DREQ and HLDA are assigned to input pins in the ATV5000. The HOLD and DACK signals are assigned to I/O pins in the ATV5000, since they are signals output by the controller.

Address and Word Counters

The address and word counters store the starting addresses, transfer word count, and command word. All use buried registers in the ATV5000, since the data does not need to be directly output. The registers are used as counters which load and then increment or decrement. The load and count functions are controlled by the bus control signals and the state machine.

The registers are configured as T-type flip-flops, so that a minimum number of product terms are required to implement the counter functions. Loading is accomplished by XORing the output of the register with the load data, causing the T flip-flop to toggle if the data does not match.

The outputs of the address registers are multiplexed onto the address bus to provide source and destination addresses for the DMA transfer. After each transfer, the addresses are incremented and the word count is decremented. When the word count reaches zero, the DONE signal is sent to the state machine, indicating that the transfer is complete.

The command word is decoded and used by the state machine to determine what type of DMA will be performed. The data is only used by the state machine, so it can be stored in buried registers in the ATV5000. The word consists of three bits: two bits which indicate whether the source and destination are memory or I/O devices, and a third bit which enables the DMA to start. After the DMA is complete, the enable bit is reset.

State Machine

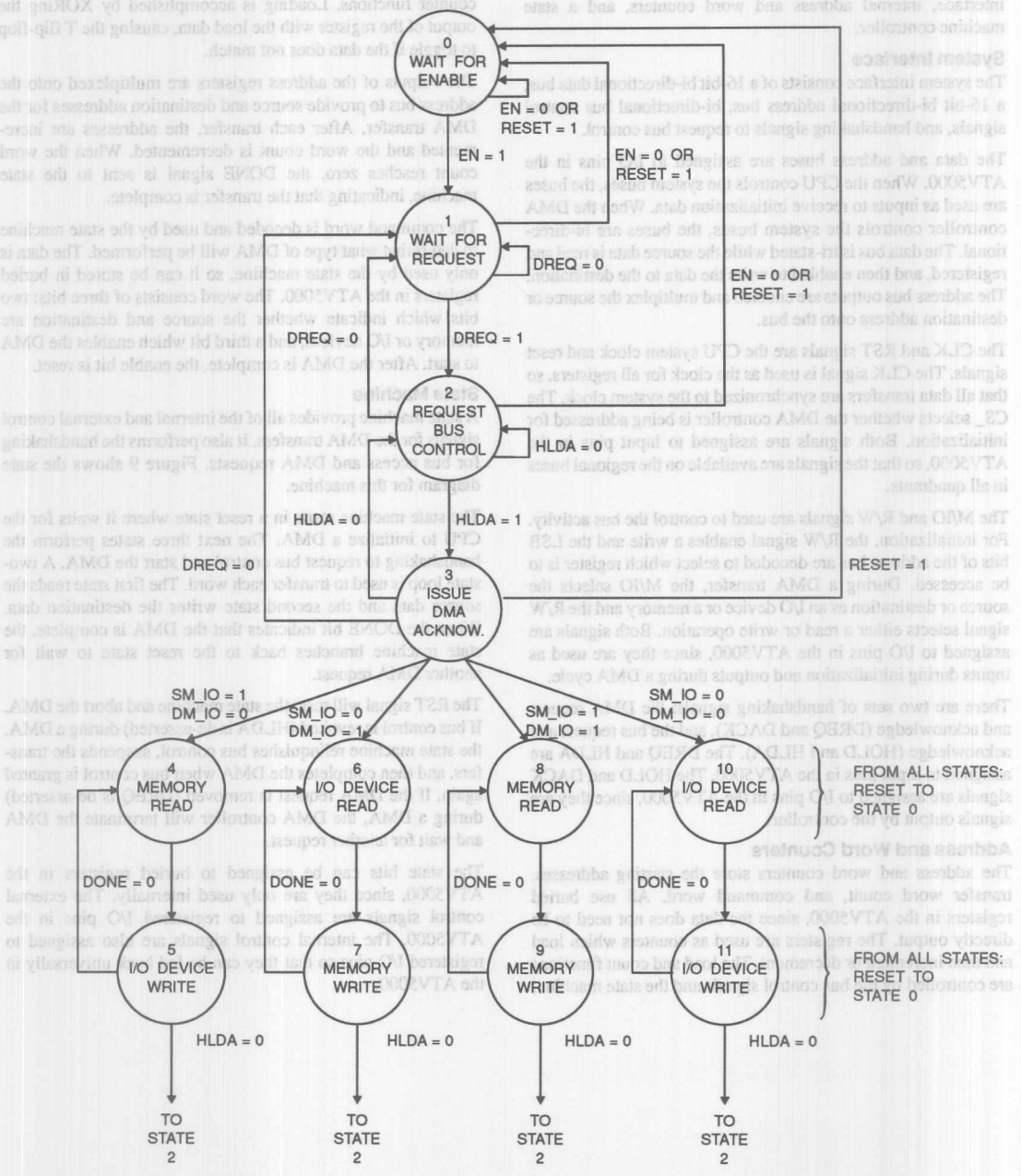
A state machine provides all of the internal and external control signals for the DMA transfers. It also performs the handshaking for bus access and DMA requests. Figure 9 shows the state diagram for this machine.

The state machine starts in a reset state where it waits for the CPU to initialize a DMA. The next three states perform the handshaking to request bus control and start the DMA. A two-state loop is used to transfer each word. The first state reads the source data and the second state writes the destination data. When the DONE bit indicates that the DMA is complete, the state machine branches back to the reset state to wait for another DMA request.

The RST signal will reset the state machine and abort the DMA. If bus control is revoked (HLDA is de-asserted) during a DMA, the state machine relinquishes bus control, suspends the transfers, and then completes the DMA when bus control is granted again. If the DMA request is removed (DREQ is de-asserted) during a DMA, the DMA controller will terminate the DMA and wait for another request.

The state bits can be assigned to buried registers in the ATV5000, since they are only used internally. The external control signals are assigned to registered I/O pins in the ATV5000. The internal control signals are also assigned to registered I/O pins so that they can be fed back universally in the ATV5000.

Figure 9. State Diagram



ATV5000 Resource Allocation

The goal in allocating functions to the available resources in the ATV5000 is to group functions which interface each other into the same quadrant. This will minimize the number of signals which must be routed on the universal bus and minimize the number of universal product terms required for each logic function. Within a quadrant, the I/O pins and associated logic are assigned first, and then any remaining buried resources can be assigned.

In this application, the address and data bus interfaces and the address and word counters would ideally be located in the same quadrant. This would minimize the universal bus routing and allow the counters to use buried registers. Since there are not enough resources in each quadrant to fit that much logic, the functions must be divided into smaller pieces. Figure 10 shows how the logic for this application is divided and allocated into quadrants.

The buses and counters are "bit-sliced" to create logic blocks which fit into each quadrant. The counters are divided by creating stages with a look-ahead carry in between. The first quadrant contains five bits of the data and address buses, five bits of each of the counters, and a carry bit from each counter. The second quadrant contains the next five-bit section and the third quadrant contains the last six-bit section. The carry bits are routed on the universal bus to the next quadrant. The state machine and command register are allocated to the fourth quadrant. The internal control signals generated by the state machine are routed on the universal bus to all quadrants.

Each of the counters would normally require three universal product terms for the load and count functions, since the control signals are universal. This would mean that each of the counters needs two sum terms in each logic cell. To avoid this, a regional load control signal was created in each quadrant for each of the counters, using the buried logic cells. Two of the counters universal product terms then become regional product terms, and the counters only require one sum term.

Each bit of the address bus is assigned to a combinatorial I/O pin. Each of those logic cells has two buried registers available, which are used for the address counters. The logic cell configuration is shown in Figure 4. Each bit of the data bus is assigned to a registered I/O pin. Each of those logic cells has an additional buried register available, which is used for the word counter. The carry bits for the counters are assigned to registered I/O pins so they can be routed universally.

The four state bits required seven, ten, four, and four product terms. In order to provide seven product terms, the first state bit was assigned to a registered I/O pin and allocated two sum terms. The other available register in that logic cell was assigned to one of the state bits which only required four product terms. The logic cell configuration is shown in Figure 5. The state bit which required ten product terms was assigned to a registered I/O pin and allocated all three sum terms. The control signals from the state machine (both internal and external) were assigned to registered I/O cells. The other available buried registers in those logic cells were assigned to the remaining state bit and the command register bits.

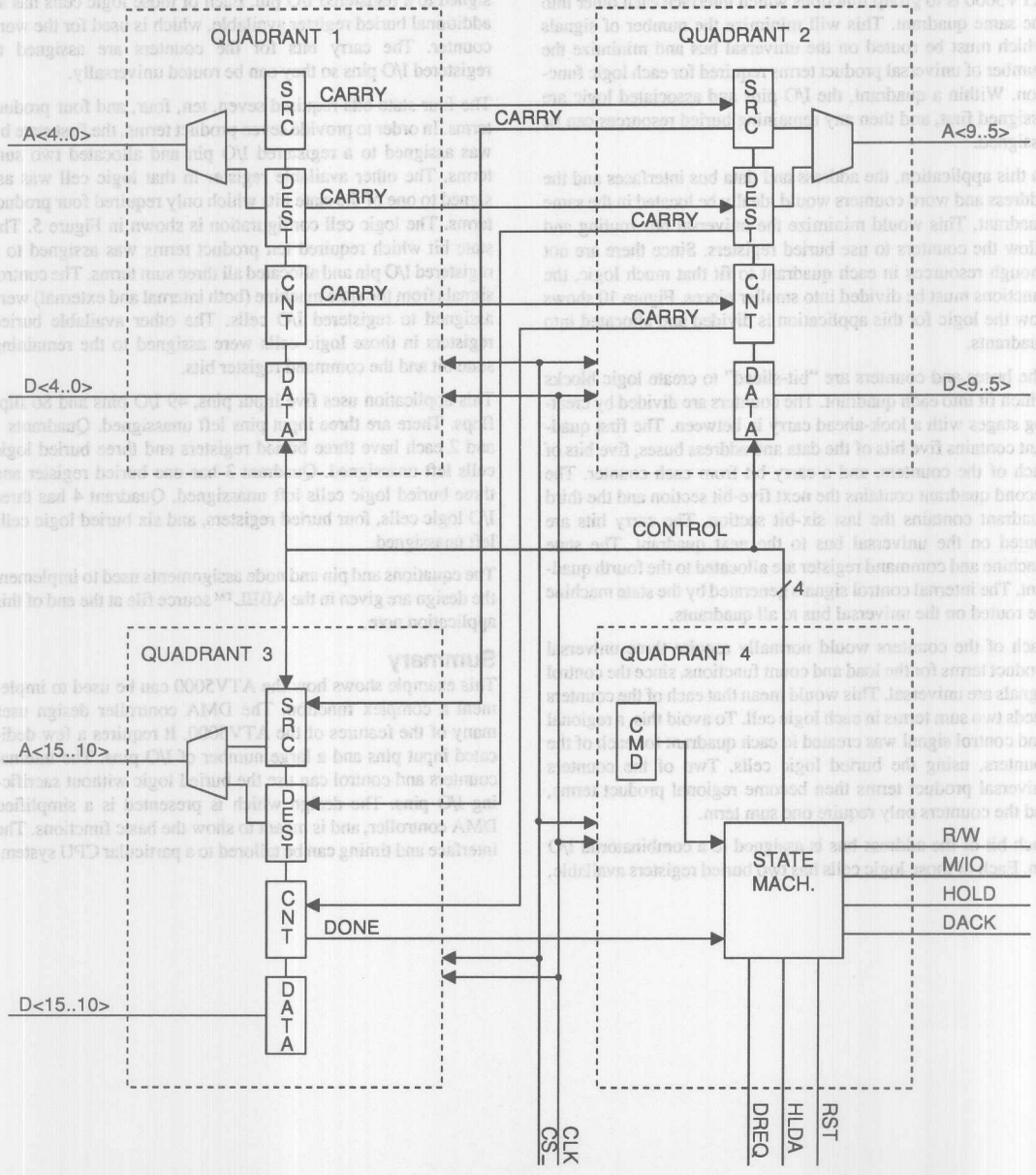
This application uses five input pins, 49 I/O pins and 86 flip-flops. There are three input pins left unassigned. Quadrants 1 and 2 each have three buried registers and three buried logic cells left unassigned. Quadrant 3 has one buried register and three buried logic cells left unassigned. Quadrant 4 has three I/O logic cells, four buried registers, and six buried logic cells left unassigned.

The equations and pin and node assignments used to implement the design are given in the ABEL™ source file at the end of this application note.

Summary

This example shows how the ATV5000 can be used to implement a complex function. The DMA controller design uses many of the features of the ATV5000. It requires a few dedicated input pins and a large number of I/O pins. The internal counters and control can use the buried logic without sacrificing I/O pins. The design which is presented is a simplified DMA controller, and is meant to show the basic functions. The interface and timing can be tailored to a particular CPU system.

Figure 10. Resource Allocation



ABEL™ Source Code

```
module DMAC ;
title 'DMA Controller - Example for the ATV5000
ATMEL Corporation EPLD - (408)436-4333 EPLD Applications Hotline
Wendey Mueller - Sept. 15, 1992'

DMAC device 'P5000';

CLK,CS_,RST                pin 1,2,32;
HLDA,DREQ                  pin 34,35;
D0,D1,D2,D3                pin 4,5,6,7 istype 'reg_d,buffer';
D4,D5,D6,D7                pin 8,18,19,21 istype 'reg_d,buffer';
D8,D9,D10,D11              pin 22,23,38,39 istype 'reg_d,buffer';
D12,D13,D14,D15            pin 40,41,42,43 istype 'reg_d,buffer';
A0,A1,A2,A3                pin 9,10,11,12 istype 'com,buffer';
A4,A5,A6,A7                pin 13,24,25,26 istype 'com,buffer';
A8,A9,A10,A11              pin 27,28,44,45 istype 'com,buffer';
A12,A13,A14,A15            pin 46,47,48,49 istype 'com,buffer';
R_W,M_IO                   pin 55,56 istype 'reg_d,buffer';
HOLD,DACK                  pin 57,58 istype 'reg_d,buffer';

ST0,ST1                    pin 52,53 istype 'reg_d,buffer';
ST2,ST3                    node 160,162 istype 'reg_d,buffer';
EN,SM_IO,DM_IO             node 163,164,165 istype 'reg_d,buffer';
DMA_EN,BUS_OE              pin 59,60 istype 'reg_d,buffer';
CNTEN,LATEN                pin 61,62 istype 'reg_d,buffer';
CNT0,CNT1,CNT2,CNT3        node 121,122,123,124 istype 'reg_t,buffer';
CNT4,CNT5,CNT6,CNT7        node 125,134,135,136 istype 'reg_t,buffer';
CNT8,CNT9,CNT10,CNT11      node 137,138,147,148 istype 'reg_t,buffer';
CNT12,CNT13,CNT14,CNT15    node 149,150,151,152 istype 'reg_t,buffer';
SA0,SA1,SA2,SA3            node 766,767,768,769 istype 'reg_t,buffer';
SA4,SA5,SA6,SA7            node 770,779,780,781 istype 'reg_t,buffer';
SA8,SA9,SA10,SA11          node 782,783,793,794 istype 'reg_t,buffer';
SA12,SA13,SA14,SA15        node 795,796,797,798 istype 'reg_t,buffer';
DA0,DA1,DA2,DA3            node 126,127,128,129 istype 'reg_t,buffer';
DA4,DA5,DA6,DA7            node 130,139,140,141 istype 'reg_t,buffer';
DA8,DA9,DA10,DA11          node 142,143,153,154 istype 'reg_t,buffer';
DA12,DA13,DA14,DA15        node 155,156,157,158 istype 'reg_t,buffer';
SCARRY1,SCARRY2            pin 14,29 istype 'reg_d,buffer';
DCARRY1,DCARRY2            pin 15,30 istype 'reg_d,buffer';
CCARRY1,CCARRY2            pin 17,31 istype 'reg_d,buffer';
DONE                       pin 51 istype 'com,buffer';
LDSRC1,LDSRC2,LDSRC3       node 173,179,185 istype 'com,buffer';
LDDST1,LDDST2,LDDST3       node 174,180,186 istype 'com,buffer';
LDCNT1,LDCNT2,LDCNT3       node 175,181,187 istype 'com,buffer';

C,K,X,Z,U,D,H,L = .C.,.K.,.X.,.Z.,.U.,.D.,1,0;

"CREATE BUSES

DATABUS = [D15..D0];     "data bus
DATA = [D4..D0];  DATB = [D9..D5];  DATC = [D15..D10];
DLSB = [D7..D0];

ADDR = [A15..A0];        "address bus
ALSB = [A7..A0];

WRDCNT = [CNT15..CNT0]; "word count
CNTLSB = [CNT7..CNT0];
CNTA = [CNT4..CNT0];  CNTB = [CNT9..CNT5];  CNTC = [CNT15..CNT10];

SRCADR = [SA15..SA0];    "source address
SRCA = [SA4..SA0];  SRCB = [SA9..SA5];  SRCC = [SA15..SA10];
```

```
SRCLSB = [SA7..SA0];

DSTADR = [DA15..DA0];   "destination address
DSTA = [DA4..DA0];  DSTB = [DA9..DA5];  DSTC = [DA15..DA10];
DSTLSB = [DA7..DA0];

COMMAND = [EN,DM_IO,SM_IO]; "command register

STMACH = [ST3,ST2,ST1,ST0]; "state bits
STDATA = [CNTEN,LATEN,DMA_EN,BUS_OE,M_IO,R_W,DACK,HOLD]; "state machine outputs

"DEFINE STATES

S0  = [0,0,0,0];
S1  = [0,0,0,1];
S2  = [0,0,1,0];
S3  = [0,0,1,1];
S4  = [0,1,0,0];
S5  = [0,1,0,1];
S6  = [0,1,1,0];
S7  = [0,1,1,1];
S8  = [1,0,0,0];
S9  = [1,0,0,1];
S10 = [1,0,1,0];
S11 = [1,0,1,1];

"Register select for initialization
"
" A1  A0  register selected
"--------------------------
" 0   0   Command register
" 0   1   Source address register
" 1   0   Destination address register
" 1   1   Word count register
"

EQUATIONS

M_IO.OE = DMA_EN;  "M_IO and R_W are control outputs during DMA
R_W.OE = DMA_EN;

ADDR = (!BUS_OE & SRCADR.FB)     "Select source or destination address
     # (BUS_OE & DSTADR.FB);
ADDR.OE = DMA_EN;                "Address output during DMA

DATABUS.D = (DATABUS & LATEN)       "Clock in data on input bus if
          # (DATABUS.FB & !LATEN); "LATEN is true
DATABUS.CK = !CLK;
DATABUS.OE = BUS_OE;             "Data output to destination during DMA

COMMAND.D = [D2,D1,D0];          "load command register
COMMAND.CK = CLK & !CS_ & R_W & !A1 & !A0;
COMMAND.AR = DONE;

LDSRC1 = !CS_ & R_W & !A1 & A0; "create regional controls for
LDSRC2 = !CS_ & R_W & !A1 & A0; "source address counter
LDSRC3 = !CS_ & R_W & !A1 & A0;

LDDST1 = !CS_ & R_W & A1 & !A0; "create regional controls for
LDDST2 = !CS_ & R_W & A1 & !A0; "destination address counter
LDDST3 = !CS_ & R_W & A1 & !A0;

LDCNT1 = !CS_ & R_W & A1 & A0;  "create regional load controls for
LDCNT2 = !CS_ & R_W & A1 & A0;  "word counter
```

```
LDCNT3 = !CS_ & R_W & A1 & A0;

"Source address counter - 16-bit up-counter w/ parallel load
"                         3 stages with look-ahead carry in between

SRCC.T = ((SRCC.FB + 1) $ SRCC.FB) & CNTEN & SCARRY2 & SCARRY1  "count
       # (DATC.FB $ SRCC.FB) & LDSRC3;                          "load
SRCB.T = ((SRCB.FB + 1) $ SRCB.FB) & CNTEN & SCARRY1            "count
       # (DATB.FB $ SRCB.FB) & LDSRC2;                          "load
SRCA.T = ((SRCA.FB + 1) $ SRCA.FB) & CNTEN                      "count
       # (DATA.FB $ SRCA.FB) & LDSRC1;                          "load
SRCADR.CK = CLK;

SCARRY1.D = (SRCA.FB == ^h1E) & CNTEN "source address 1st stage carry
          # SCARRY1.FB & !CNTEN;
SCARRY1.CK = CLK;
SCARRY2.D = (SRCB.FB == ^h1F) & CNTEN  "source address 2nd stage carry
          # SCARRY2.FB & !CNTEN;
SCARRY2.CK = CLK;

"Destination address counter - 16-bit up-counter w/ parallel load
"                              3 stages with look-ahead carry in between

DSTC.T = ((DSTC.FB + 1) $ DSTC.FB) & CNTEN & DCARRY2 & DCARRY1  "count
       # (DATC.FB $ DSTC.FB) & LDDST3;                          "load
DSTB.T = ((DSTB.FB + 1) $ DSTB.FB) & CNTEN & DCARRY1            "count
       # (DATB.FB $ DSTB.FB) & LDDST2;                          "load
DSTA.T = ((DSTA.FB + 1) $ DSTA.FB) & CNTEN                      "count
       # (DATA.FB $ DSTA.FB) & LDDST1;                          "load
DSTADR.CK = CLK;

DCARRY1.D = (DSTA.FB == ^h1E) & CNTEN  "destination address 1st stage carry
          # DCARRY1.FB & !CNTEN;
DCARRY1.CK = CLK;
DCARRY2.D = (DSTB.FB == ^h1F) & CNTEN  "destination address 2nd stage carry
          # DCARRY2.FB & !CNTEN;
DCARRY2.CK = CLK;

"Word counter - 16-bit down-counter w/ parallel load
"               3-stages with look-ahead carry in between

CNTC.T = ((CNTC.FB - 1) $ CNTC.FB) & CNTEN & CCARRY2 & CCARRY1  "count
       # (DATC.FB $ CNTC.FB) & LDCNT3;                          "load
CNTB.T = ((CNTB.FB - 1) $ CNTB.FB) & CNTEN & CCARRY1            "count
       # (DATB.FB $ CNTB.FB) & LDCNT2;                          "load
CNTA.T = ((CNTA.FB - 1) $ CNTA.FB) & CNTEN                      "count
       # (DATA.FB $ CNTA.FB) & LDCNT1;                          "load
WRDCNT.CK = CLK;

CCARRY1.D = (CNTA.FB == ^h01) & CNTEN  "word count 1st stage carry
          # CCARRY1.FB & !CNTEN;
CCARRY1.CK = CLK;
CCARRY2.D = (CNTB.FB == ^h00) & CNTEN  "word count 2nd stage carry
          # CCARRY2.FB & !CNTEN;
CCARRY2.CK = CLK;

DONE = (CNTC.FB == 0) & CCARRY1 & CCARRY2; "Detects when DMA is complete

STMACH.CK = CLK;
STDATA.CK = CLK;

"State Machine Controller -
"
"Inputs: RST,EN,SM_IO,DM_IO,DREQ,HLDA,DONE
```

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```
"Outputs: CNTEN,LATEN,DMA_EN,BUS_OE,M_IO,R_W,DACK,HOLD

STATE_DIAGRAM STMACH

STATE S0:                          "Reset, idle state
   IF (EN & !RST) THEN             "If DMA is enabled, go to state 1
      S1 WITH STDATA.D = [0,1,0,0,0,0,0,0]; ENDWITH;
   ELSE                            "else, wait for enable
      S0 WITH STDATA.D = [0,1,0,0,0,0,0,0]; ENDWITH;

STATE S1:                          "DMA enabled, wait for DMA request
   IF (!EN # RST) THEN             "If disabled or reset, return to state 0
      S0 WITH STDATA.D = [0,1,0,0,0,0,0,0]; ENDWITH;
   ELSE IF (DREQ) THEN             "If DMA requested, go to state 2
      S2 WITH STDATA.D = [0,1,0,0,0,0,0,1]; ENDWITH;
   ELSE                            "else, wait for DMA request
      S1 WITH STDATA.D = [0,1,0,0,0,0,0,0]; ENDWITH;

STATE S2:                          "DMA requested, issue bus request
   IF (!EN # RST) THEN             "If disabled or reset, return to state 0
      S0 WITH STDATA.D = [0,1,0,0,0,0,0,0]; ENDWITH;
   ELSE IF (!DREQ) THEN            "If DMA request was removed, return to state 1
      S1 WITH STDATA.D = [0,1,0,0,0,0,0,0]; ENDWITH;
   ELSE IF (HLDA) THEN             "If bus control granted, go to state 3
      S3 WITH STDATA.D = [0,1,0,0,0,0,1,1]; ENDWITH;
   ELSE                            "else, wait for bus control
      S2 WITH STDATA.D = [0,1,0,0,0,0,0,1]; ENDWITH;

STATE S3:                          "Bus granted, issue DMA acknowledge
   IF (!EN # RST) THEN             "If disabled or reset, return to state 0
      S0 WITH STDATA.D = [0,1,0,0,0,0,0,0]; ENDWITH;
   ELSE IF (!DREQ) THEN            "If DMA request was removed, return to state 1
      S1 WITH STDATA.D = [0,1,0,0,0,0,0,0]; ENDWITH;
   ELSE IF (!HLDA) THEN            "If bus control was revoked, return to state 2
      S2 WITH STDATA.D = [0,1,0,0,0,0,0,1]; ENDWITH;
   ELSE IF (SM_IO & !DM_IO) THEN  "Start DMA: Memory - I/O Device
      S4 WITH STDATA.D = [0,1,1,0,1,0,1,1]; ENDWITH;
   ELSE IF (!SM_IO & DM_IO) THEN  "Start DMA: I/O Device - Memory
      S6 WITH STDATA.D = [0,1,1,0,0,0,1,1]; ENDWITH;
   ELSE IF (SM_IO & DM_IO) THEN   "Start DMA: Memory - Memory
      S8 WITH STDATA.D = [0,1,1,0,1,0,1,1]; ENDWITH;
   ELSE IF (!SM_IO & !DM_IO) THEN "Start DMA: I/O Device - I/O Device
      S10 WITH STDATA.D = [0,1,1,0,0,0,1,1]; ENDWITH;

STATE S4:                          "DMA cycle, memory read
   IF (!DREQ # RST) THEN           "If DMA request removed or reset, return to state 0
      S0 WITH STDATA.D = [0,1,0,0,0,0,0,0]; ENDWITH;
   ELSE                            "else, continue DMA transfer
      S5 WITH STDATA.D = [1,0,1,1,0,1,1,1]; ENDWITH;

STATE S5:                          "DMA cycle, I/O device write
   IF (!DREQ # RST # DONE) THEN    "If DMA request removed, reset or done,
                                   "return to state 0
      S0 WITH STDATA.D = [0,1,0,0,0,0,0,0]; ENDWITH;
   ELSE IF (!HLDA) THEN            "If bus control revoked, return to state 2
      S2 WITH STDATA.D = [0,1,0,0,0,0,0,1]; ENDWITH;
   ELSE                            "else, continue DMA transfer
      S4 WITH STDATA.D = [0,1,1,0,1,0,1,1]; ENDWITH;

STATE S6:                          "DMA cycle, I/O device read
   IF (!DREQ # RST) THEN           "If DMA request removed or reset, return to state 0
      S0 WITH STDATA.D = [0,1,0,0,0,0,0,0]; ENDWITH;
   ELSE                            "else, continue DMA transfer
      S7 WITH STDATA.D = [1,0,1,1,1,1,1,1]; ENDWITH;
```

```
STATE S7:                    "DMA cycle, memory write
   IF (!DREQ # RST # DONE) THEN  "If DMA request removed, reset or done,
                                 "return to state 0
      S0 WITH STDATA.D = [0,1,0,0,0,0,0,0]; ENDWITH;
   ELSE IF (!HLDA) THEN          "If bus control revoked, return to state 2
      S2 WITH STDATA.D = [0,1,0,0,0,0,0,1]; ENDWITH;
   ELSE                          "else, continue DMA transfer
      S6 WITH STDATA.D = [0,1,1,0,0,0,1,1]; ENDWITH;

STATE S8:                    "DMA cycle, memory read
   IF (!DREQ # RST) THEN     "If DMA request removed or reset, return to state 0
      S0 WITH STDATA.D = [0,1,0,0,0,0,0,0]; ENDWITH;
   ELSE                      "else, continue DMA transfer
      S9 WITH STDATA.D = [1,0,1,1,1,1,1,1]; ENDWITH;

STATE S9:                    "DMA cycle, memory write
   IF (!DREQ # RST # DONE) THEN "If DMA request removed, reset or done,
                                "return to state 0
      S0 WITH STDATA.D = [0,1,0,0,0,0,0,0]; ENDWITH;
   ELSE IF (!HLDA) THEN      "If bus control revoked, return to state 2
      S2 WITH STDATA.D = [0,1,0,0,0,0,0,1]; ENDWITH;
   ELSE                      "else, continue DMA transfer
      S8 WITH STDATA.D = [0,1,1,0,1,0,1,1]; ENDWITH;

STATE S10:                   "DMA cycle, I/O device read
   IF (!DREQ # RST) THEN     "If DMA request removed or reset, return to state 0
      S0 WITH STDATA.D = [0,1,0,0,0,0,0,0]; ENDWITH;
   ELSE                      "else, continue DMA transfer
      S11 WITH STDATA.D = [1,0,1,1,0,1,1,1]; ENDWITH;

STATE S11:                    "DMA cycle, I/O device write
   IF (!DREQ # RST # DONE) THEN  "If DMA request removed, reset or done,
                                 "return to state 0
      S0 WITH STDATA.D = [0,1,0,0,0,0,0,0]; ENDWITH;
   ELSE IF (!HLDA) THEN          "If bus control revoked, return to state 2
      S2 WITH STDATA.D = [0,1,0,0,0,0,0,1]; ENDWITH;
   ELSE                          "else, continue DMA transfer
      S10 WITH STDATA.D = [0,1,1,0,0,0,1,1]; ENDWITH;

"This set of test vectors initializes the source address, destination address,
"word count and command data.

TEST_VECTORS (
[CLK,RST,CS_,M_IO,R_W,ALSB,DLSB] - [SRCLSB,DSTLSB,CNTLSB,COMMAND])
[ 1,  0, 1,  0,   1,  0,   0   ] - [  0,     0,     0,    0      ];
[ 1,  1, 1,  0,   1,  0,   0   ] - [  0,     0,     0,    0      ];
[ K,  0, 0,  0,   1,  1,  00A  ] - [00A,     0,     0,    0      ];
[ K,  0, 0,  0,   1,  2,  0B0  ] - [00A,   0B0,     0,    0      ];
[ K,  0, 0,  0,   1,  3,  003  ] - [00A,   0B0,   003,    0      ];
[ K,  0, 0,  0,   1,  0,  007  ] - [00A,   0B0,   003,    7      ];

"This set of test vectors performs a DMA transfer using the addresses and word
"count which was loaded.

TEST_VECTORS (
[CLK,RST,CS_,ALSB,DLSB,DREQ,HLDA] - [STMACH,STDATA,SRCLSB,DSTLSB,CNTLSB,DONE])
[ 1, 0,  1,  0,   0,   0,   0   ] - [1,     X,     0A,    0B0,   03,    0   ];
[ C, 0,  1,  0,   0,   0,   0   ] - [1,     X,     0A,    0B0,   03,    0   ];
[ C, 0,  1,  0,   0,   1,   0   ] - [2,     X,     0A,    0B0,   03,    0   ];
[ C, 0,  1,  0,   0,   1,   1   ] - [3,     X,     0A,    0B0,   03,    0   ];
[ C, 0,  1,  0,   55,  1,   1   ] - [8,     06B,   0A,    0B0,   03,    0   ];
[ C, 0,  1,  0,   0,   1,   1   ] - [9,     0BF,   0A,    0B0,   03,    0   ];
[ C, 0,  1,  0,   66,  1,   1   ] - [8,     06B,   0B,    0B1,   02,    0   ];
```

```
[ C, 0,  1,  0,   0,   1,   1   ] - [9,     0BF,   0B,    0B1,   02,    0   ];
[ C, 0,  1,  0,   77,  1,   1   ] - [8,     06B,   0C,    0B2,   01,    0   ];
[ C, 0,  1,  0,   0,   1,   1   ] - [9,     0BF,   0C,    0B2,   01,    0   ];
[ C, 0,  1,  0,   0,   1,   1   ] - [8,     06B,   0D,    0B3,   00,    1   ];
[ C, 0,  1,  0,   0,   1,   1   ] - [9,     0BF,   0D,    0B3,   00,    1   ];
[ C, 0,  1,  0,   0,   1,   1   ] - [0,     X,     0E,    0B4,   0FF,   0   ];

END ;
```

Using the Programmable Polarity Control

The output programmable polarity control in PLDs brings efficiency in logic reduction and control of output polarity to the customers. Unfortunately, it also brings confusion to customers who are not familiar with the software syntax to properly configure the output polarity.

This application note shows the proper usage of the popular ABEL™ and CUPL™ syntax to configure the output polarity of Atmel EPLDs.

Configuring Polarity with Atmel-ABEL™ 4.x and ABEL™ 4.x

The optimization level best suited for Atmel EPLDs is the default option – reduce by pin and auto polarity. This reduction level will take advantage of the polarity control when performing logic optimization one output at a time. This will override the ISTYPE 'NEG' and ISTYPE 'POS' used in ABEL™ 3.x source files (check the user manual on backward compatibility for detail). Therefore, the 'NEG' and 'POS' extensions are not recommended.

The following examples have A, B, and C defined as inputs and OUT or !OUT as the output:

Case 1: (Combinatorial - no ISTYPE definition)

```
Declaration
OUT pin 14;
"assume 14 is an I/O pin
equations
OUT = A # B # C;
```

In this case, the compiler will consider both Figure 1 (on-set) and Figure 2 (off-set) and automatically select the implementation requiring fewer product terms for the same function. The outcome is represented by Figure 2. Since Figures 1 and 2 are each DeMorgan equivalent of the other, either one is logically correct.

Case 2: (Combinatorial - ISTYPE 'BUFFER')

```
Declaration
OUT pin 14 ISTYPE 'buffer';
"assume 14 is an I/O pin
equations
OUT = A # B # C;
```

In this case, the compiler will only consider the on-set because the ISTYPE 'BUFFER' overrides the automatic selection. The outcome is represented by Figure 1.

Case 3a: (Combinatorial - ISTYPE 'INVERT')

```
Declaration
OUT pin 14 ISTYPE 'invert';
"assume 14 is an I/O pin
equations
OUT = A # B # C;
```

In this case, the compiler will only consider Figure 2 (off-set) because the ISTYPE 'INVERT' overrides the automatic selection. The outcome is represented by Figure 2.

Case 3b: (Combinatorial - no ISTYPE definition)

```
Declaration
!OUT pin 14;
"assume 14 is an I/O pin
equations
OUT = A # B # C;
```

The compiler would pick Figure 3 to implement the logic because it takes fewer product terms. In ABEL™ documentation, signals on the right side of the equation do not have "!" as part of their names. ABEL™ preprocessor will remove the "!" from the pin name on the right side of the equation and replace all references on the left side with an additional "!". Logically, this does not change anything. It does, however, tend to create some confusion reading the .DOC files. In the source file, the user should still use whatever pin name is given in the declaration section. All references to the pin or .FB feedbacks will be adjusted by the software to reflect the changes automatically.

Case 3c: (Combinatorial - ISTYPE 'INVERT')

```
Declaration
!OUT pin 14 ISTYPE 'invert';
"assume 14 is an I/O pin
equations
OUT = A # B # C;
```

The compiler would pick Figure 4 to implement the logic.

For combinatorial equations, it is best to leave out the ISTYPE statement and let the optimizer choose the best DeMorgan equivalent implementation.

Figure 1.

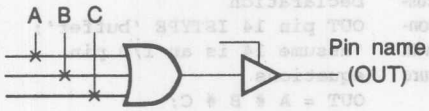


Figure 2.

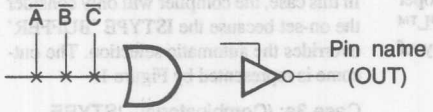


Figure 3.

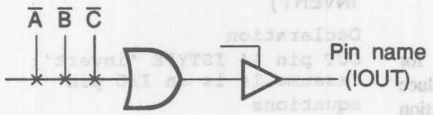
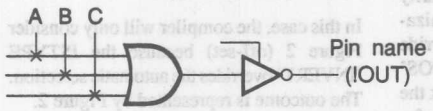


Figure 4.



Case 4: (Registered - no ISTYPE definition) Beware!

```
Declaration
OUT pin 14;
"assume 14 is an I/O pin
equations
OUT.d  = A # B # C;
OUT.c  = CLK;
OUT.ar = AR1;
```

The pre-processor will warn you for not specifying the ISTYPE of the output. In this case, the compiler will use the fewest product term implementation (Figure 6). This might not be what the user is expecting.(1)

Note:

1. Figure 5 and Figure 6 do not produce identical results. In Figure 5, at power up or after a reset, the output pin appears to be a "0." Unlike Figure 5, Figure 6 powers up and resets to a "1" on the output. Preset and preload behave differently between the two as well. In some applications where power-up state of a register is not important and it never resets or presets, Figures 5 and 6 become identical. Only in this case are they logically equivalent. When using a registered output, always specify the ISTYPE desired.

Case 5: (Registered - ISTYPE 'BUFFER')

```
Declaration
OUT pin 14 ISTYPE 'buffer';
"assume 14 is an I/O pin
equations
OUT.d  = A # B # C;
OUT.c  = CLK;
OUT.ar = AR1;
```

The compiler will only consider Figure 5 (on-set) because the ISTYPE 'BUFFER' overrides the automatic selection.

Case 6: (Registered - ISTYPE 'INVERT') Be careful!

```
Declaration
OUT pin 14 ISTYPE 'invert';
"assume 14 is an I/O pin
equations
OUT.d  = A # B # C;
OUT.c  = CLK;
OUT.ar = AR1;
```

The compiler will only consider Figure 6 (off-set) because the ISTYPE 'INVERT' overrides the automatic selection (see Note 1 on Case 4).

Case 7: (Registered - ISTYPE 'BUFFER') Confusing – don't use.

```
Declaration
!OUT pin 14 ISTYPE 'buffer';
"assume 14 is an I/O pin
equations
OUT.d  = A # B # C;
OUT.c  = CLK;
OUT.ar = AR1;
```

The compiler will only consider Figure 7 (on-set) because the ISTYPE 'BUFFER' overrides the automatic selection.

Case 8: (Registered - ISTYPE 'INVERT')

```
Declaration
!OUT pin 14 ISTYPE 'invert';
"assume 14 is an I/O pin
equations
OUT.d  = A # B # C;
OUT.c  = CLK;
OUT.ar = AR1;
```

The compiler will only consider Figure 8 (off-set) because the ISTYPE 'INVERT' overrides the automatic selection. In ABEL™ documentation, the pin name will be stripped of the "!". It will replace all pin name references with an additional "!" on the right-hand side of the equations.

Figure 5.

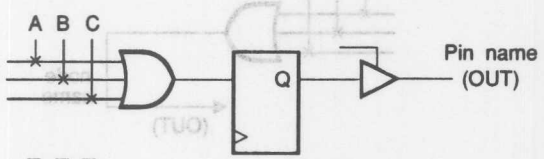


Figure 6.

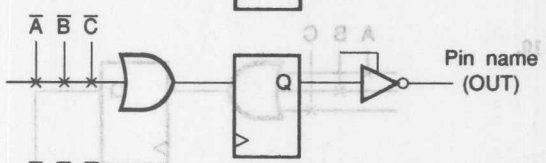


Figure 7.

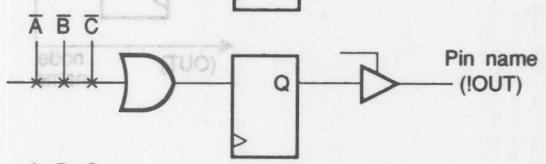
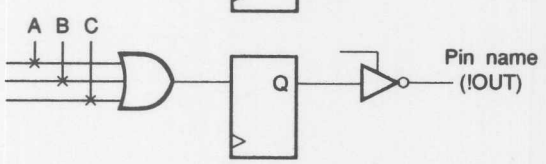


Figure 8.



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Configuring Polarity with Internal Nodes

Internal nodes do not have programmable polarity control. Do not use any ISTYPE extensions. Think of it as "positive logic" only.

Case 1: (Figure 9)

```
Declaration
OUT node 50;
"assume 50 is an internal node
equations
OUT = A # B # C;
```

Case 2: (Figure 10)

```
Declaration
OUT node 50;
"assume 50 is an internal node
equations
OUT.d  = A # B # C;
OUT.c  = CLK;
OUT.ar = AR1;
```

The above example is the only legal method of assigning equations to nodes.

Figure 9.

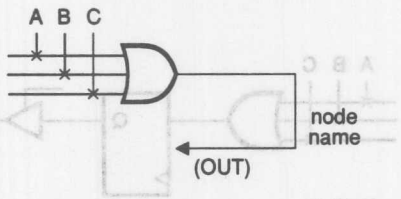
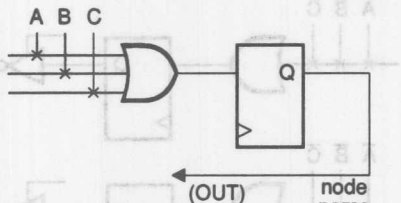


Figure 10.



Configuring Polarity with CUPL™

Note that CUPL™ has no "buffer/invert" ISTYPE statement. Output polarity is controlled by pin declaration versus equation polarity.

Case 1: (Combinatorial)

```
PIN 14 OUTC; /* assume 14 is an I/O pin */
OUTC = A # B # C;
```

The compiler would choose Figure 11. It does not choose the better DeMorgan equivalent automatically. If your equation does not fit, you should check to see if you can rewrite it as:

```
PIN 14 OUTC;
!OUTC = !A & !B & !C;
```

Case 2: (Combinatorial)

```
PIN 14 !OUTC; /* assume 14 is an I/O pin */
OUTC = A # B # C;
```

The compiler would choose Figure 12. The difference between the pin declaration (!OUTC) and the equation name (OUTC) tells the compiler to have an inverter on the output and to implement the equations as specified by the equation.

Case 3: (Registered)

```
PIN 14 OUTC; /* assume 14 is an I/O pin */
OUTC.d = A # B # C;
OUTC.ck = CLK;
```

The compiler would choose Figure 13. The pin name and the equation name are identical; the compiler does not place an inverter on the output.

Case 4: (Registered)

```
PIN 14 !OUTC; /* assume 14 is an I/O pin */
OUTC.d = A # B # C;
OUTC.ck = CLK;
```

The compiler would choose Figure 14. The difference between the pin declaration (!OUTC) and the equation name (OUTC) tells the compiler to have an inverter on the output and to implement the equations as specified by the equation. CUPL™ maintains the !OUTC on the pinout diagram documentation and equation name OUTC in the reduced equation portion of the documentation.

Both ABEL™ and CUPL™ conventions for handling signal polarity have drawn praises and criticisms. Help on the software is readily available from Data I/O Corporation (ABEL™), Logical Devices, Incorporated (CUPL™), and Atmel. Don't hesitate to call for help.

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Figure 11.

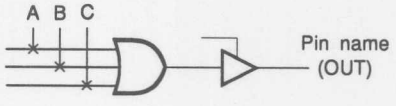


Figure 12.

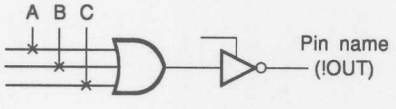


Figure 13.

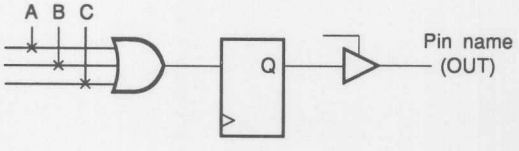
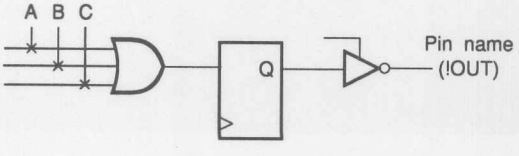


Figure 14.



Configuring Polarity with CUPL™

Note that CUPL™ has no "buffer/inverter" ISTYPE statement. Output polarity is controlled by pin declaration versus equation polarity.

Case 1: (Combinatorial)

```
PIN 14 OUTC; /* assume 14 is an I/O pin */
OUTC = A # B # C;
```

The compiler would choose Figure 11. It does not choose the better DeMorgan equivalent automatically. If your equation does not fit, you should check to see if you can rewrite it as:

```
PIN 14 OUTC;
!OUTC = !A & !B & !C;
```

Case 2: (Combinatorial)

```
PIN 14 !OUTC; /* assume 14 is an I/O pin */
OUTC = A # B # C;
```

The compiler would choose Figure 12. The difference between the pin declaration (!OUTC) and the equation name (OUTC) tells the compiler to have an inverter on the output and to implement the equations as specified by the equation.

Case 3: (Registered)

```
PIN 14 OUTC; /* assume 14 is an I/O pin */
OUTC.d = A # B # C;
OUTC.ck = CLK;
```

The compiler would choose Figure 13. The pin name and the equation name are identical; the compiler does not place an inverter on the output.

Case 4: (Registered)

```
PIN 14 !OUTC; /* assume 14 is an I/O pin */
OUTC.d = A # B # C;
OUTC.ck = CLK;
```

The compiler would choose Figure 14. The difference between the pin declaration (!OUTC) and the equation name (OUTC) tells the compiler to have an inverter on the output and to implement the equations as specified by the equation. CUPL™ maintains the !OUTC on the pinout diagram documentation and equation name OUTC in the reduced equation portion of the documentation.

Both ABEL™ and CUPL™ conventions for handling signal polarity have drawn praises and criticisms. Help on the software is readily available from Data I/O Corporation (ABEL™), Logical Devices, Incorporated (CUPL™), and Atmel. Don't hesitate to call for help.

Figure 11.



Figure 12.



Figure 13.

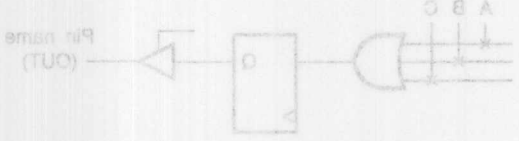
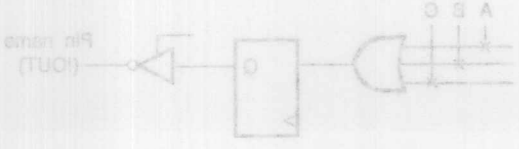


Figure 14.



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Section 8

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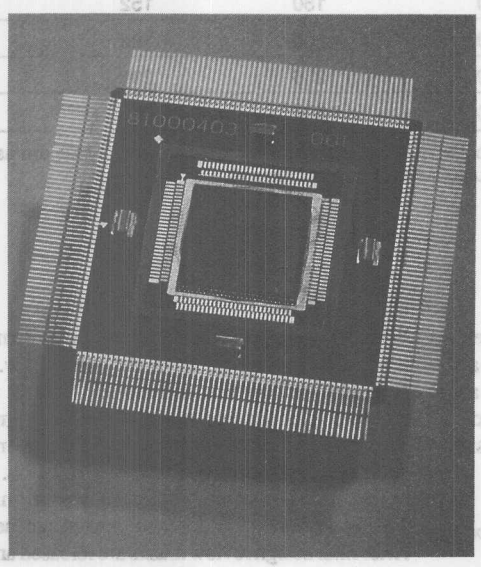
Features

- 1.0 µ Drawn Gate Length High-performance CMOS Gate Arrays
- All ATL Gate Arrays are Specified from 3.0 Volts to 5.5 Volts, for Standard and Low Voltage Applications
- Design Translation of Existing ASIC Designs Provide for Easy Alternate Sourcing with Equivalent or Improved Performance
- EPLD/FPGA Conversions to ATL Gate Array, Several EPLD and FPGA can be Combined into a Single Gate Array.
- ATL C Version, Fine Pad Pitch Gate Arrays are Ideal for High I/O, Low Gate Count Designs (Commercial, Industrial Only)
- ATL Gate Arrays can be Supplied Compliant to MIL-STD-883
- Improved Product Testability Using Serial Scan, Boundary Scan, JTAG and Built-in-self-test

Description

The high-performance ATL Series CMOS gate arrays employ 1.0 µ-drawn, double-level metal, Si-gate, CMOS technology processed in Atmel's U.S.-based, advanced manufacturing facility. The arrays utilize an enhanced channelless architecture which results in greater than 50 percent usable gates.

Atmel's flexible design system uses industry design standards and is compatible with popular CAD/CAE software and hardware packages. The customer can start designing with the ATL series today using existing CAD/CAE tools.



ATL Series Gate Arrays

ATL4
ATL10
ATL20
ATL40
ATL60
ATL75
ATL100
ATL130
ATL160

ATL7C
ATL10C
ATL15C
ATL20C
ATL35C
ATL55C
ATL75C

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ATL Array Organization

Device Number	Maximum Gates	Routable Gates	Max Pin Count	Max I/O(1) Pins	Gate(2) Speed
ATL4	4,100	2,600	68	60	375 ps
ATL10	10,000	6,500	124	116	375 ps
ATL20	22,000	12,000	144	136	375 ps
ATL40	40,000	22,000	180	168	375 ps
ATL60	57,000	30,000	224	208	375 ps
ATL75	72,000	38,000	256	236	375 ps
ATL100	95,000	50,000	292	262	375 ps
ATL130	131,000	67,000	338	308	375 ps
ATL160	157,000	80,000	360	320	375 ps

ATL C Array Organization - Fine Pad Pitch

Device Number	Maximum Gates	Routable Gates	Max Pin Count	Max I/O(1) Pins	Gate(2) Speed
ATL7C	7,000	4,000	100	92	375 ps
ATL10C	10,000	6,000	120	112	375 ps
ATL15C	15,000	8,000	144	136	375 ps
ATL20C	22,000	12,000	160	152	375 ps
ATL35C	35,000	18,000	208	192	375 ps
ATL55C	55,000	29,000	256	236	375 ps
ATL75C	75,000	39,000	304	280	375 ps

Notes: 1. Absolute maximum I/O pins is maximum pin count minus 8. Additional power and ground pins are assumed to be required to support simultaneous switching outputs as pin count increases.
2. Nominal 2 input nand gate with a fan out of 2

ATL Design

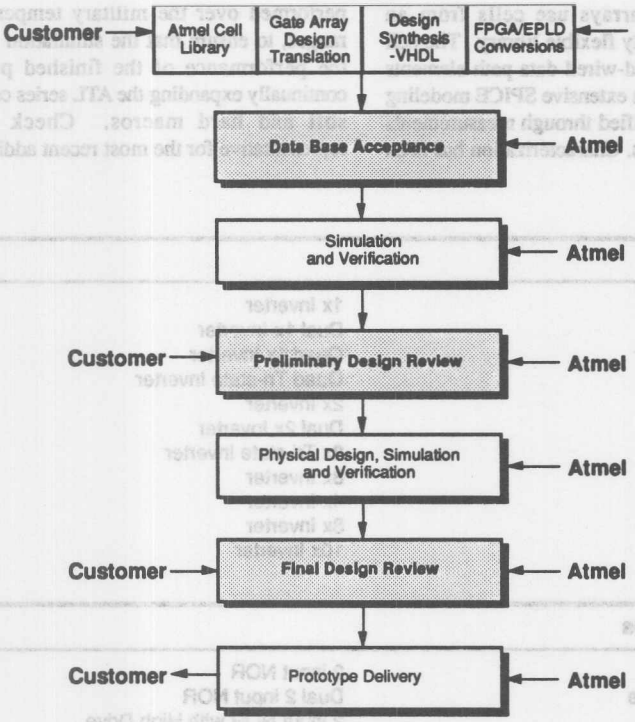
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Valid	Synopsys	Racal-Redac	

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Atmel has successfully translated existing FPGA/EPLD designs from most major vendors (Xilinx, Actel, Altera, AMD & Atmel) into our ATL series gate arrays. The design can be optimized for speed or power consumption, modified to add logic or memory or replicated for a pin-for-pin compatible, drop-in replacement. Atmel frequently combines several devices onto a single gate array.

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Atmel's ATL series gate arrays use cells from an accurately modeled and highly flexible library. The cell library contains over 120 hard-wired data path elements and has been characterized via extensive SPICE modeling at the transistor level and verified through measurements made on fabricated test arrays. Characterization has been performed over the military temperature and voltage ranges, to ensure that the simulation accurately predicts the performance of the finished product. Atmel is continually expanding the ATL series cell library with both soft and hard macros. Check with your sales representative for the most recent additions.

Cell Guide

Buffers and Inverters	
1x Buffer	1x Inverter
2x Buffer	Dual 1x Inverter
2x Buffer with Enable	Quad 1x Inverter
2x Buffer with Enable Low	Quad Tri-state Inverter
3x Buffer	2x Inverter
4x Buffer	Dual 2x Inverter
8x Buffer	2x Tri-state Inverter
12x Buffer	3x Inverter
16x Buffer	4x Inverter
Delay Buffer 2.0 ns	8x Inverter
Delay Buffer 3.5 ns	10x Inverter
Delay Buffer 8.0 ns	

AND, NAND, OR, NOR Gates	
2 input AND	2 input NOR
2 input AND with High Drive	Dual 2 input NOR
3 input AND	2 input NOR with High Drive
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Cell Guide

Multiplexers	
2:1 MUX	4:1 MUX
2:1 MUX with High Drive	4:1 MUX w/o Buffered Inputs
Inverting 2:1 MUX w/o Buffered Inputs	4:1 MUX w/o Buffered Inputs, High Drive
Inverting 2:1 MUX w/o Buffered Inputs, High Drive	5:1 MUX with High Drive
2:1 MUX with Enable Low	8:1 MUX
Quad 2:1 MUX with Enable	8:1 MUX with Enable Low
Quad 2:1 MUX	8:1 MUX High Drive
Inverting 3:1 MUX w/o Buffered Inputs	
Inverting 3:1 MUX w/o Buffered Inputs, High Drive	

AND/OR, OR/AND Gates	
3 input AND OR INVERT	3 input OR AND INVERT
3 input AND OR INVERT with High Drive	3 input OR AND INVERT with High Drive
4 input AND OR INVERT	4 input OR AND INVERT
4 input AND OR INVERT with High Drive	4 input OR AND INVERT with High Drive
6 input AND OR INVERT	8 input OR AND INVERT
6 input AND OR INVERT with High Drive	4 input OR AND INVERT with 2 inputs to AND

Exclusive OR/NOR Gates	
1 bit Adder	2 input Exclusive OR with High Drive
1 bit Adder with Buffered Outputs	2 input Exclusive NOR
7 input Carry Lookahead	2 input Exclusive NOR with High Drive
2 input Exclusive OR	

Decoders	
2:4 Decoder	3:8 Decoder with Low Enable
2:4 Decoder with Low Enable	

Flip-flops/Latches	
D Flip-flop	LATCH
D Flip-flop with Clear/Preset	LATCH with Complementary Outputs
D Flip-flop with Clear	LATCH with Inverted Gate Signal
D Flip-flop with High Drive	QUAD LATBG with Common Gate Signal
D Flip-flop with Reset	LATCH with High Drive
D Flip-flop with Set	QUAD Inverting LATCH
D Flip-flop with Set/Reset	LATCH with Reset
JK Flip-flop	LATCH with Set
JK Flip-flop with Clear/Preset	LATCH with Set and Reset
JK Flip-flop with Clear	

Cell Guide

Scan Cells	
Set-scan Register	Set-scan Register with Set
Set-scan Register with Clear and Preset	Set-scan Register with Set and Reset
Set-scan Register with Reset	

I/O Options
Input, Output, Bidirectional, Tristate Output, Internal Clock Driver and Oscillator
Output Drive Value Programmable from 2 mA to 24 mA in 2 mA increments with Slew Rate Control
CMOS or TTL Operation
Schmitt Trigger (Bidirectional, Input)
Testable NAND Gate on Input (Bidirectional, Input)
Inverting and Non-inverting Input Buffers (Bidirectional, Input)
Pullup Resistor - 10K Ω to 310K Ω
Pulldown Resistor - 3.5K Ω to 108.5K Ω

74XX Series Soft Macros
24 cells available

HDL Macros - Available in Verilog-HDL or VHDL Simulation Models	
Function Group	**Available Cells**
adder	37
alu	29
baud rate generator	3
comparator	18
counter	27
fifo	56
incrementor/decrementor	60
mux	7
parity/error correction	15
scan	31
shifter	9
multipliers	10

CMOS/TTL Input Interface Characteristics

Interface	Logic High	Logic Low	Switchpoint
CMOS	3.5 V Minimum	1.5 V Maximum	$V_{dd}/2$ Typical
TTL	2.0 V Minimum	0.8 V Maximum	1.4 V Typical

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V[1]
Maximum Operating Voltage	6.0 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{dd} + 0.75 V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

5.0 Volt DC Characteristics

Applicable over recommended operating range from T_a = -55°C to +125°C, V_{dd} = 4.5 V to 5.5 V (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
I_{IH}	Input Leakage High	$V_{IN} = V_{dd}$, V_{dd} = 5.5 V		.01	10	µA
I_{IL}	Input Leakage Low (no pull-up)	$V_{IN} = V_{SS}$, V_{dd} = 5.5 V	-10	.01		µA
	40K pull-up	$V_{IN} = V_{SS}$, V_{dd} = 5.5 V	-325	-160	-40	µA
I_{OZ}	Output Leakage (no pull-up)	$V_{IN} = V_{dd}$ or V_{SS}, V_{dd} = 5.5 V	-10	.01	10	µA
I_{OS}	Output Short Circuit Current (3 x Buffer)(2)	V_{dd} = 5.5 V, $V_{OUT} = V_{dd}$	10	50	100	mA
		V_{dd} = 5.5 V, $V_{OUT} = V_{SS}$	-100	-50	-10	mA
V_{IL}	TTL Input Low Voltage				0.8	V
V_{IL}	CMOS Input Low Voltage				0.3 x V_{dd}	V
V_{IH}	TTL Input High Voltage		2.0			V
V_{IH}	CMOS Input High Voltage		0.7 x V_{dd}			V
V_T	TTL Switching Threshold	V_{dd} = 5.0 V, 25°C		1.4		V
	CMOS Switching Threshold	V_{dd} = 5.0 V, 25°C		2.4		V
V_{OL}	Output Low Voltage Output buffer has 12 stages of drive capability with 2 mA I_{OL} per stage.	I_{OL} = as rated, V_{dd} = 4.5 V		0.2	0.4	V
V_{OH}	Output High Voltage Output buffer has 12 stages of drive capability with -2 mA I_{OH} per stage.	I_{OH} = as rated, V_{dd} = 4.5 V	0.7 x V_{dd}	4.2		V

Note: 2. This is the specification for the 3 x Output Buffer. Output short circuit current for other outputs will scale accordingly. Not more than one output shorted at a time, for a maximum of one second, is allowed.

8

5.0 Volt DC Characteristics

Applicable over recommended operating range from T_a = -55°C to +125°C, V_{dd} = 3.0 V to 3.6 V (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
I_{IH}	Input Leakage High	$V_{IN} = V_{dd}$, V_{dd} = 3.6 V		.01	10	µA
I_{IL}	Input Leakage Low (no pull-up)	$V_{IN} = V_{SS}$, V_{dd} = 3.6 V	-10	.01		µA
	40K pull-up	$V_{IN} = V_{SS}$, V_{dd} = 3.6 V	-200	-60	-10	µA
I_{OZ}	Output Leakage (no pull-up)	$V_{IN} = V_{dd}$ or V_{SS}, V_{dd} = 3.6 V	-10	.01	10	µA
I_{OS}	Output Short Circuit Current (3 x Buffer)(2)	V_{dd} = 3.6 V, $V_{OUT} = V_{dd}$	5	25	60	mA
		V_{dd} = 3.6 V, $V_{OUT} = V_{SS}$	-60	-25	-5	mA
V_{IL}	CMOS Input Low Voltage				0.3 x V_{dd}	V
V_{IH}	CMOS Input High Voltage		0.7 x V_{dd}			V
V_T	CMOS Switching Threshold	V_{dd} = 3.3 V, 25°C		1.5		V
V_{OL}	Output Low Voltage Output buffer has 12 stages of drive capability with 1 mA I_{OL} per stage.	I_{OL} = as rated V_{dd} = 3.0 V			0.4	V
V_{OH}	Output High Voltage Output buffer has 12 stages of drive capability with -1 mA I_{OH} per stage.	I_{OH} = as rated V_{dd} = 3.0 V	0.7 x V_{dd}			V

Note: 2. This is the specification for the 3 x Output Buffer. Output short circuit current for other outputs will scale accordingly. Not more than one output shorted at a time, for a maximum of one second, is allowed.

I/O Buffer DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
C_{IN}	Capacitance Input Buffer (Die)	5.0 V, 3.3 V		2.4		pF
C_{OUT}	Capacitance Output Buffer (Die)	5.0 V, 3.3 V		5.6		pF
$C_{I/O}$	Capacitance Bi-Directional	5.0 V, 3.3 V		6.6		pF
Schmitt Trigger						
V+	TTL Positive Threshold	25°C, 5.0 V		1.8	2.0	V
	CMOS Positive Threshold	25°C, 5.0 V		3.2	3.5	V
V-	TTL Negative Threshold	25°C, 5.0 V	0.6	0.8		V
	CMOS Negative Threshold	25°C, 5.0 V	1.0	1.2		V
ΔV	TTL Hysteresis	25°C, 5.0 V	0.4	1.0		
	CMOS Hysteresis	25°C, 5.0 V	1.0	2.0		
V+	CMOS Positive Threshold	25°C, 3.3 V		2.2	2.3	V
V-	CMOS Negative Threshold	25°C, 3.3 V	.65	0.9		V
ΔV	CMOS Hystersis	25°C, 3.3 V	.65	1.3		

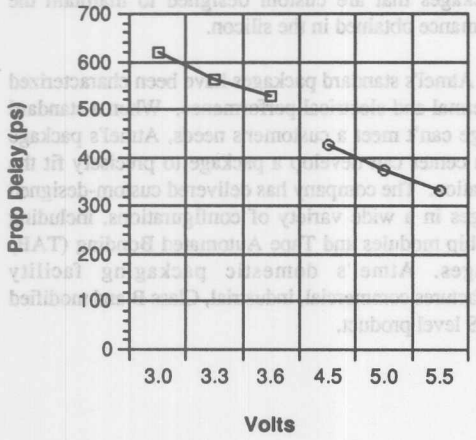
I/O Buffers

- Programmable output drive
  (2 to 24 mA I_{OL}, -2 to -24 mA I_{OH} for 5.0 V
  1 to 12 mA I_{OL}, -1 to -12 mA I_{OH} for 3.3 V)
- 3000 volts ESD protection
- Built-in configurable test logic

The ATL series input/output ring contains the I/O buffer circuitry capable of sourcing and sinking currents up to 24 mA, and responds to CMOS or TTL logic levels. I/O locations on this ring can accommodate bidirectional cells.

AC Characteristics

Delay vs V_{dd}

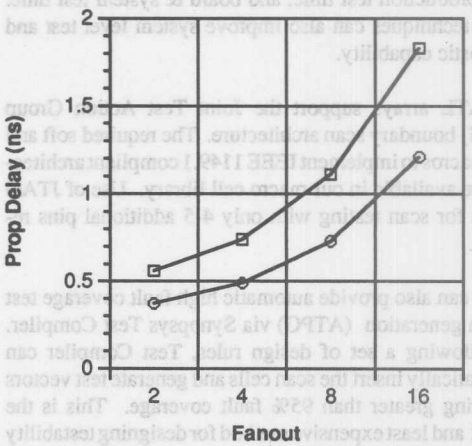


3.3 Volts V_{dd}

5.0 Volts V_{dd}

NAND2 - 2 input NAND
Temp = 25°C
FO = 2

Delay vs Fanout

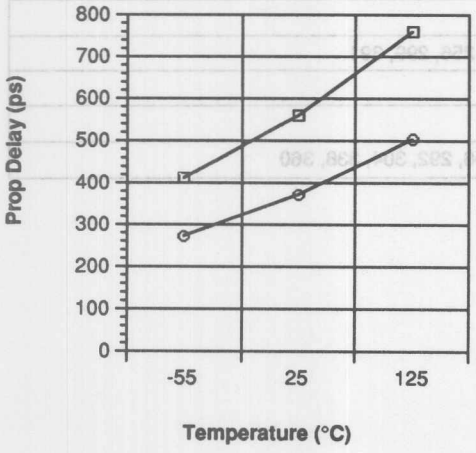


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5.0 Volts V_{dd}

NAND2 - 2 input NAND
Temp = 25°C

Delay vs Temperature

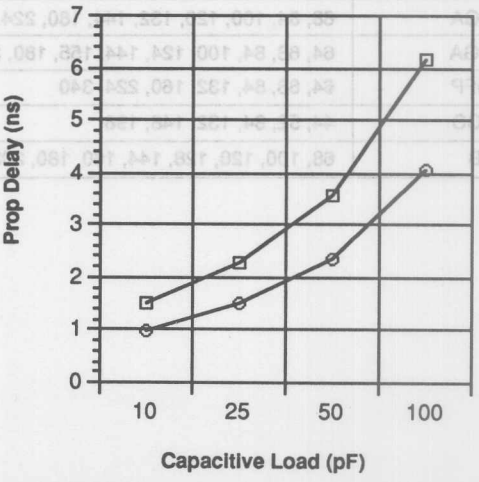


3.3 Volts V_{dd}

5.0 Volts V_{dd}

NAND2 - 2 input NAND
FO = 2

Output Buffer vs Load



3.3 Volts V_{dd}

5.0 Volts V_{dd}

PDO4 - Output Buffer 8 mA
Temp = 25°C

Design for Testability

Atmel supports a full range of Design-for-Test improvement techniques which reduce design and prototype debug time, production test time, and board & system test time. These techniques can also improve system level test and diagnostic capability.

The ATL arrays support the Joint Test Action Group (JTAG) boundary scan architecture. The required soft and hard macros to implement IEEE 1149.1 compliant architecture are available in our macro cell library. Use of JTAG allows for scan testing with only 4-5 additional pins required.

Atmel can also provide automatic high fault coverage test pattern generation (ATPG) via Synopsys Test Compiler. By following a set of design rules, Test Compiler can automatically insert the scan cells and generate test vectors providing greater than 95% fault coverage. This is the easiest and least expensive method for designing testability into a gate array design.

Advanced Packaging

Atmel supports a wide variety of standard packages for the ATL series, but also offers its ATL series gate arrays in packages that are custom designed to maintain the performance obtained in the silicon.

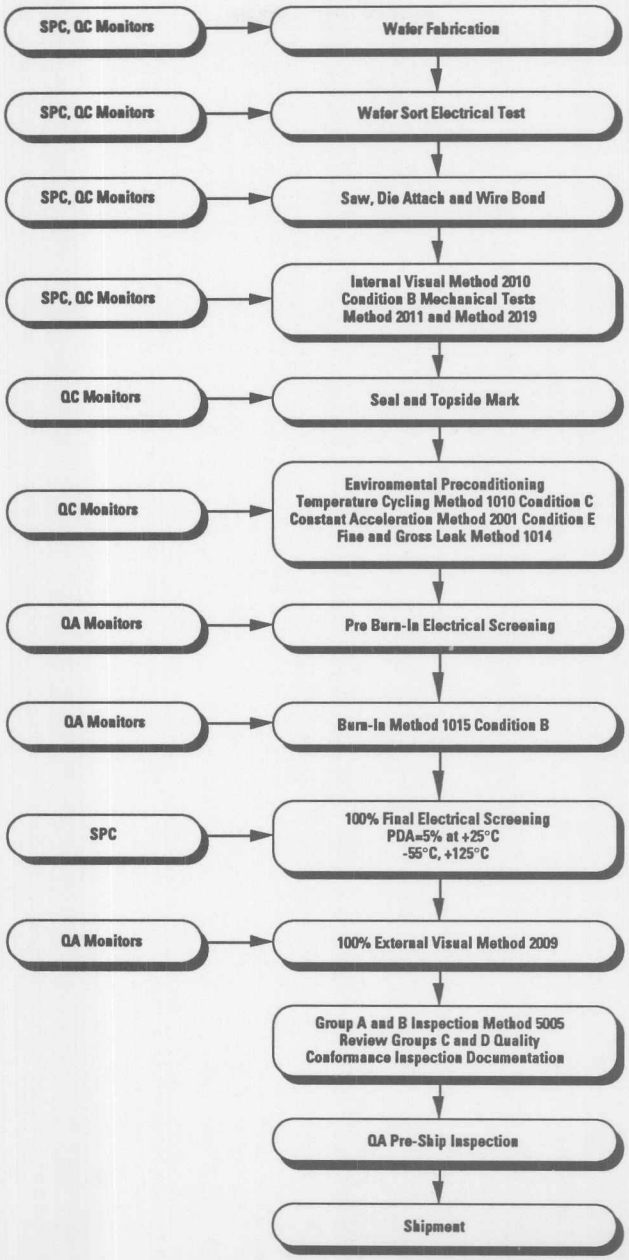
All of Atmel's standard packages have been characterized for thermal and electrical performance. When a standard package can't meet a customer's needs, Atmel's package design center can develop a package to precisely fit the application. The company has delivered custom-designed packages in a wide variety of configurations, including multichip modules and Tape Automated Bonding (TAB) packages. Atmel's domestic packaging facility manufactures commercial, industrial, Class B and modified Class S level product.

Packaging Options

Package Type	Pin Count
TQFP	44, 48, 64, 80, 100, 144, 160, 208, 240, 248, 304
PQFP	44, 64, 68, 80, 100, 120, 128, 132, 136, 144, 160, 184, 208, 232, 256, 304
PLCC	28, 44, 68, 84
PPGA	68, 84, 100, 120, 132, 144, 180, 224
CPGA	64, 68, 84, 100, 124, 144, 155, 180, 223, 224, 256, 299, 391
CQFP	64, 68, 84, 132, 160, 224, 340
CLCC	44, 52, 84, 132, 148, 196
TAB	68, 100, 120, 128, 144, 160, 180, 208, 224, 256, 292, 304, 338, 360

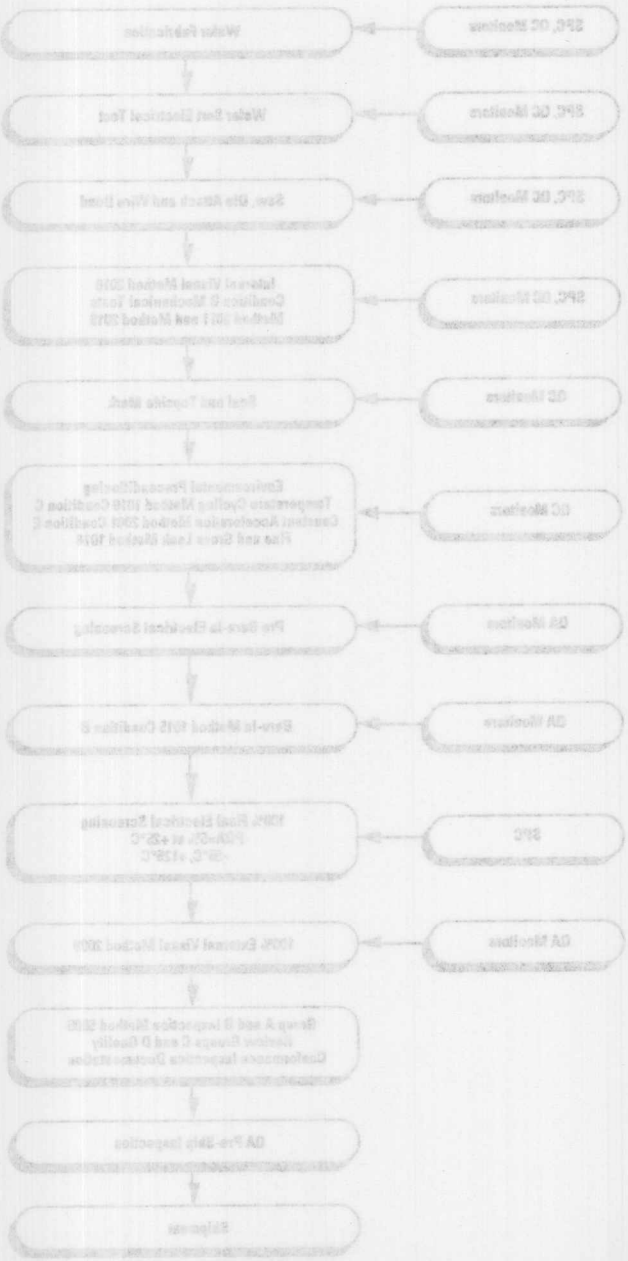
Military Product Flow Chart

MIL-STD-883 Class B



8

Actel, Altera, AMD, Cadence, DAZIX, Fujitsu, LSI Logic, Mentor, NEC, Oki, Racal-Redac, Synopsys, Valid, Verilog-XL, Viewlogic, and Xilinx may be registered trademarks of others.



Features

- 0.8 µ drawn gate length combined with triple level metal provides outstanding speed/power performance
- Design translation of existing ASIC, PLD and FPGA designs provide for easy alternate sourcing with equivalent performance
- All ATL80 arrays can operate at 5.0 volts and 3.3 volts for low-power applications
- Product testability is improved using techniques such as serial and boundary scan, ATPG, built-in self test and JTAG
- ATL80 arrays can be screened to MIL-STD-883

Description

The high-performance ATL80 Series CMOS gate arrays offer superior system performance, flexibility, testability and board utilization. The ATL80 gate arrays employ an advanced technology 0.8 µ-drawn, triple-level metal, Si-gate, CMOS technology processed in a U.S.-based, manufacturing facility.

Atmel's efficient routing scheme combined with tight spacing for three metal layers allows Atmel to provide more gates and faster speeds. With double row bond pads as a standard feature, high I/O gate arrays can easily be accommodated. The ATL80 gate array can have 3.3 volt and 5.0 volt I/O on the same chip.

Atmel's flexible design system uses industry design standards and is compatible with popular CAD/CAE software and hardware packages. The 0.8 µ macro cell libraries are upward compatible with the existing 1.0 µ libraries and design utilities. The customer can start designing with the ATL80 series today using existing CAD/CAE tools.

ATL80 Array Organization

Device Number	Maximum Gates	Routable Gates	Max Pin Count	Gate(1) Speed
ATL80/14	13,700	9,000	100	200 ps
ATL80/25	22,500	12,000	120	200 ps
ATL80/35	35,000	20,000	144	200 ps
ATL80/60	61,000	35,000	180	200 ps
ATL80/90	87,000	45,000	208	200 ps
ATL80/140	140,000	70,000	256	200 ps
ATL80/200	194,000	90,000	304	200 ps
ATL80/250	242,000	100,000	340	200 ps
ATL80/300	296,000	120,000	360	200 ps
ATL80/425	422,000	160,000	424	200 ps
ATL80/550	580,000	200,000	490	200 ps

Note: 1. Nominal 2 Input Nand Gate With a Fan Out of 2

ATL80 Series Gate Arrays 0.8 Micron

ATL80/14
ATL80/25
ATL80/35
ATL80/60
ATL80/90
ATL80/140
ATL80/200
ATL80/250
ATL80/300
ATL80/425
ATL80/550
Preliminary

8

PRELIMINARY

ATL80 Design

Design Systems Supported

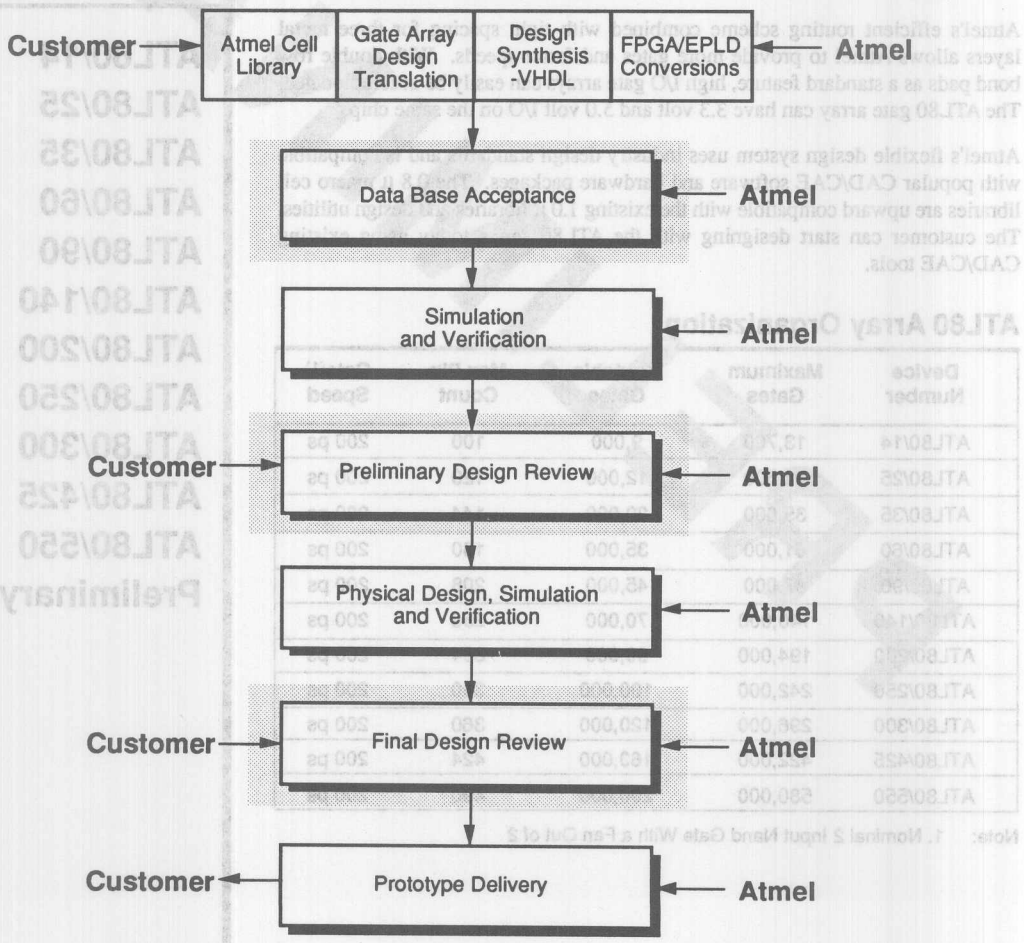
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The design flow for the ATL80 gate arrays is the same as the 1.0µ ATL gate arrays. While Atmel provides four options for implementing a gate array design, they all have the same flow. Data base acceptance is the first milestone. This is when Atmel receives and accepts the complete design data base. Preliminary design review is where the performance of the design is set based on the Cadence simulation. Final design review is the last review of the design before making masks. The back annotation data is incorporated into the simulations. After final design review masks are released and prototypes, in ceramic packages, are delivered.

ATL80 Gate Array Design Flow



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5 input AND	4 input NOR with High Drive
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Dual 2-input NAND	8 input NOR
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3 input NAND with High Drive	2 input OR with High Drive
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Inverting 2:1 MUX w/o Buffered Inputs, High Drive	5:1 MUX with High Drive
2:1 MUX with Enable Low	8:1 MUX
Quad 2:1 MUX with Enable	8:1 MUX with Enable Low
Quad 2:1 MUX	8:1 MUX High Drive
Inverting 3:1 MUX w/o Buffered Inputs	
Inverting 3:1 MUX w/o Buffered Inputs, High Drive	

AND/OR, OR/AND Gates	
3 input AND OR INVERT	3 input OR AND INVERT
3 input AND OR INVERT with High Drive	3 input OR AND INVERT with High Drive
4 input AND OR INVERT	4 input OR AND INVERT
4 input AND OR INVERT with High Drive	4 input OR AND INVERT with High Drive
6 input AND OR INVERT	8 input OR AND INVERT
6 input AND OR INVERT with High Drive	4 input OR AND INVERT with 2 inputs to AND

Exclusive OR/NOR Gates	
1 bit Adder	2 input Exclusive OR with High Drive
1 bit Adder with Buffered Outputs	2 input Exclusive NOR
7 input Carry Lookahead	2 input Exclusive NOR with High Drive
2 input Exclusive OR	

Decoders	
2:4 Decoder	3:8 Decoder with Low Enable
2:4 Decoder with Low Enable	

Flip-flops/Latches	
D Flip-flop	LATCH
D Flip-flop with Clear/Preset	LATCH with Complementary Outputs
D Flip-flop with Clear	LATCH with Inverted Gate Signal
D Flip-flop with High Drive	QUAD LATBG with Common Gate Signal
D Flip-flop with Reset	LATCH with High Drive
D Flip-flop with Set	QUAD Inverting LATCH
D Flip-flop with Set/Reset	LATCH with Reset
JK Flip-flop	LATCH with Set
JK Flip-flop with Clear/Preset	LATCH with Set and Reset
JK Flip-flop with Clear	

Scan Cells	
Set-scan Register	Set-scan Register with Set
Set-scan Register with Clear and Preset	Set-scan Register with Set and Reset
Set-scan Register with Reset	

I/O Options
Input, Output, Bidirectional, Tristate Output, Internal Clock Driver and Oscillator
Output Drive Value Programmable from 2 mA to 24 mA in 2 mA increments with Slew Rate Control
CMOS or TTL Operation
Schmitt Trigger (Bidirectional, Input)
Testable NAND Gate on Input (Bidirectional, Input)
Inverting and Non-inverting Input Buffers (Bidirectional, Input)
Pullup Resistor - 10K Ω to 310K Ω
Pulldown Resistor - 3.5K Ω to 108.5K Ω

74XX Series Soft Macros
24 cells available

HDL Macros - Available in Verilog-HDL or VHDL Simulation Models

Function Group	Available Cells
adder	37
alu	29
baud rate generator	3
comparator	18
counter	27
fifo	56
incrementor/decrementor	60
mux	7
parity/error correction	15
scan	31
shifter	9
multipliers	10

CMOS/TTL Input Interface Characteristics

Interface	Logic High	Logic Low	Switchpoint
CMOS	3.5 V Minimum	1.5 V Maximum	V_{DD}/2 Typical
TTL	2.0 V Minimum	0.8 V Maximum	1.4 V Typical

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Maximum Operating Voltage	6.0 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{DD} + 0.75 V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

5.0 Volt DC Characteristics

Applicable over recommended operating range from T_a = -55°C to +125°C, V_{DD} = 4.5 V to 5.5 V (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
I_{IH}	Input Leakage High	$V_{IN} = V_{DD}$, V_{DD} = 5.5 V		0.01	10	µA
I_{IL}	Input Leakage Low (no pull-up)	$V_{IN} = V_{SS}$, V_{DD} = 5.5 V	-10	0.01		µA
	40K pull-up	$V_{IN} = V_{SS}$, V_{DD} = 5.5 V	-325	-160	-40	µA
I_{OZ}	Output Leakage (no pull-up)	$V_{IN} = V_{DD}$ or V_{SS}, V_{DD} = 5.5 V	-10	0.01	10	µA
I_{OS}	Output Short Circuit Current (3 x Buffer)(2)	V_{DD} = 5.5 V, $V_{OUT} = V_{DD}$	10	50	100	mA
		V_{DD} = 5.5 V, $V_{OUT} = V_{SS}$	-100	-50	-10	mA
V_{IL}	TTL Input Low Voltage				0.8	V
V_{IL}	CMOS Input Low Voltage				0.3 x V_{DD}	V
V_{IH}	TTL Input High Voltage		2.0			V
V_{IH}	CMOS Input High Voltage		0.7 x V_{DD}			V
V_T	TTL Switching Threshold	V_{DD} = 5.0 V, 25°C		1.4		V
	CMOS Switching Threshold	V_{DD} = 5.0 V, 25°C		2.4		V
V_{OL}	Output Low Voltage Output buffer has 12 stages of drive capability with 2 mA I_{OL} per stage.	I_{OL} = as rated V_{DD} = 4.5 V		0.2	0.4	V
V_{OH}	Output High Voltage Output buffer has 12 stages of drive capability with -2 mA I_{OH} per stage.	I_{OH} = as rated V_{DD} = 4.5 V	0.7 x V_{DD}	4.2		V

Note: 2. This is the specification for the 3 x Output Buffer. Output short circuit current for other outputs will scale accordingly. Not more than one output shorted at a time, for a maximum of one second, is allowed.

8

3.3 Volt DC Characteristics

Applicable over recommended operating range from T_a = -55°C to +125°C, V_{DD} = 3.0 V to 3.6 V (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
I_{IH}	Input Leakage High	$V_{IN} = V_{DD}$, V_{DD} = 3.6 V		0.01	10	µA
I_{IL}	Input Leakage Low (no pull-up)	$V_{IN} = V_{SS}$, V_{DD} = 3.6 V	-10	0.01		µA
	40K pull-up	$V_{IN} = V_{SS}$, V_{DD} = 3.6 V	-200	-60	-10	µA
I_{OZ}	Output Leakage (no pull-up)	$V_{IN} = V_{DD}$ or V_{SS}, V_{DD} = 3.6 V	-10	0.01	10	µA
I_{OS}	Output Short Circuit Current (3 x Buffer)(2)	V_{DD} = 3.6 V, $V_{OUT} = V_{DD}$	5	25	60	mA
		V_{DD} = 3.6 V, $V_{OUT} = V_{SS}$	-60	-25	-5	mA
V_{IL}	CMOS Input Low Voltage				0.3 x V_{DD}	V
V_{IH}	CMOS Input High Voltage		0.7 x V_{DD}			V
V_T	CMOS Switching Threshold	V_{DD} = 3.3 V, 25°C		1.5		V
V_{OL}	Output Low Voltage Output buffer has 12 stages of drive capability with 1 mA I_{OL} per stage.	I_{OL} = as rated V_{DD} = 3.0 V			0.4	V
V_{OH}	Output High Voltage Output buffer has 12 stages of drive capability with -1 mA I_{OH} per stage.	I_{OH} = as rated V_{DD} = 3.0 V	0.7 x V_{DD}			V

Note: 2. This is the specification for the 3 x Output Buffer. Output short circuit current for other outputs will scale accordingly. Not more than one output shorted at a time, for a maximum of one second, is allowed.

I/O Buffer DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
C_{IN}	Capacitance, Input Buffer (Die)	5.0 V, 3.3 V		2.4		pF
C_{OUT}	Capacitance, Output Buffer (Die)	5.0 V, 3.3 V		5.6		pF
$C_{I/O}$	Capacitance, Bi-Directional	5.0 V, 3.3 V		6.6		pF
Schmitt Trigger						
V+	TTL Positive Threshold	25°C, 5.0 V		1.8	2.0	V
	CMOS Positive Threshold	25°C, 5.0 V		3.2	3.5	V
V-	TTL Negative Threshold	25°C, 5.0 V	0.6	0.8		V
	CMOS Negative Threshold	25°C, 5.0 V	1.0	1.2		V
ΔV	TTL Hysteresis	25°C, 5.0 V	0.4	1.0		
	CMOS Hysteresis	25°C, 5.0 V	1.0	2.0		
V+	CMOS Positive Threshold	25°C, 3.3 V		2.2	2.3	V
V-	CMOS Negative Threshold	25°C, 3.3 V	0.65	0.9		V
ΔV	CMOS Hystersis	25°C, 3.3 V	0.65	1.3		

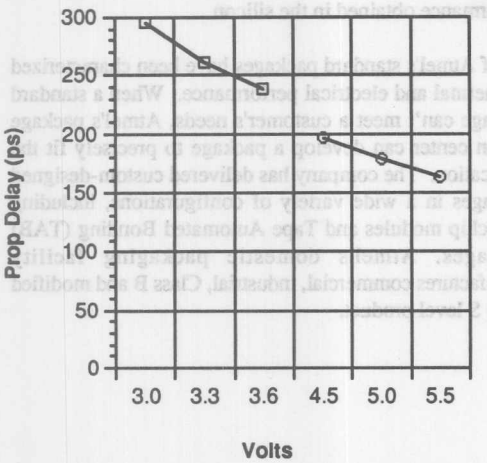
I/O Buffers

- Programmable output drive
  (2 to 24 mA I_{OL}, -2 to -24 mA I_{OH} for 5.0 V
  1 to 12 mA I_{OL}, -1 to -12 mA I_{OH} for 3.3 V)
- 3,000 volts ESD protection
- Built-in configurable test logic

The ATL80 series input/output ring contains the I/O buffer circuitry capable of sourcing and sinking currents up to 24 mA, and responds to CMOS or TTL logic levels. All outputs can be switched to a high impedance state. I/O locations on this ring can accommodate bidirectional cells.

AC Characteristics

Delay vs V_{CC}

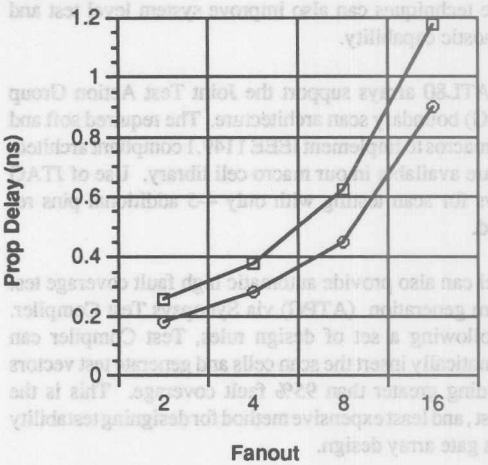


3.3 Volts V_{dd}

5.0 Volts V_{dd}

2 input NAND
Temp = 25°C
FO = 2

Delay vs Fanout

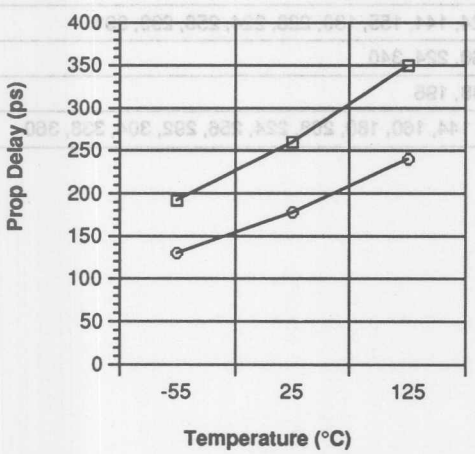


3.3 Volts V_{dd}

5.0 Volts V_{dd}

2 input NAND
Temp = 25°C

Delay vs Temperature



3.3 Volts V_{dd}

5.0 Volts V_{dd}

2 input NAND
FO = 2

Design for Testability

Atmel supports a full range of Design-for-Test improvement techniques which reduce design and prototype debug time, production test time, and board and system test time. These techniques can also improve system level test and diagnostic capability.

The ATL80 arrays support the Joint Test Action Group (JTAG) boundary scan architecture. The required soft and hard macros to implement IEEE 1149.1 compliant architecture are available in our macro cell library. Use of JTAG allows for scan testing with only 4-5 additional pins required.

Atmel can also provide automatic high fault coverage test pattern generation (ATPG) via Synopsys Test Compiler. By following a set of design rules, Test Compiler can automatically insert the scan cells and generate test vectors providing greater than 95% fault coverage. This is the easiest, and least expensive method for designing testability into a gate array design.

Advanced Packaging

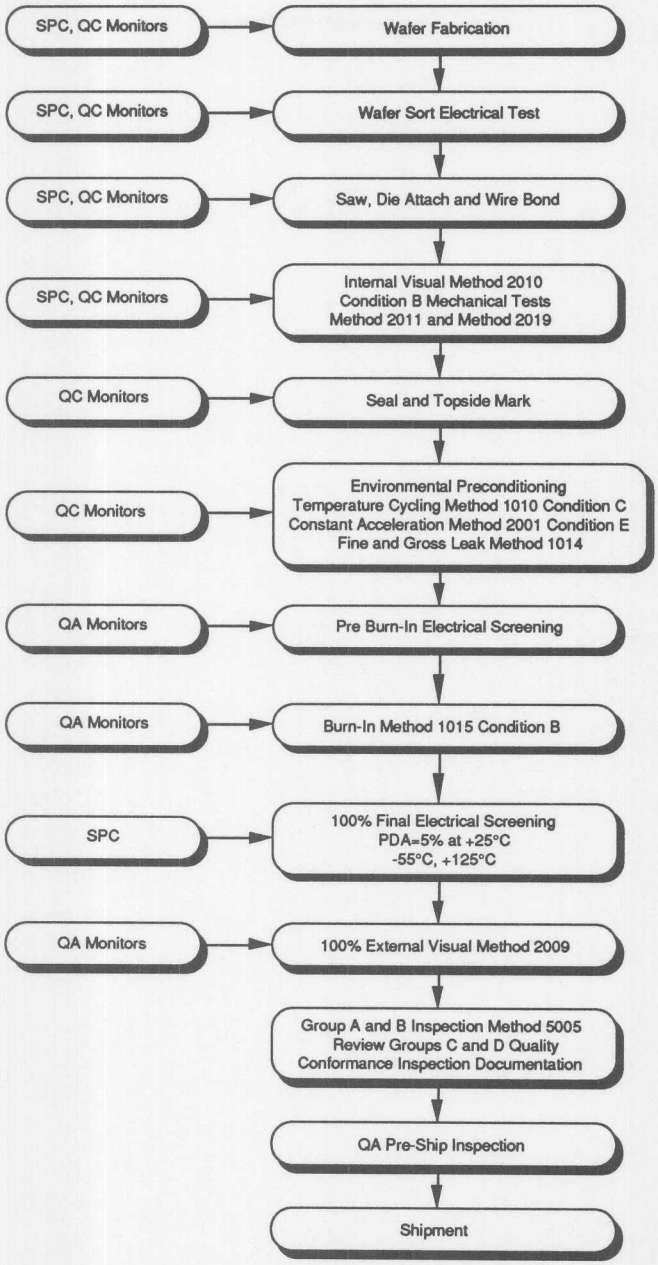
Atmel supports a wide variety of standard packages for the ATL80 series, but also offers its ATL80 series gate arrays in packages that are custom designed to maintain the performance obtained in the silicon.

All of Atmel's standard packages have been characterized for thermal and electrical performance. When a standard package can't meet a customer's needs, Atmel's package design center can develop a package to precisely fit the application. The company has delivered custom-designed packages in a wide variety of configurations, including multichip modules and Tape Automated Bonding (TAB) packages. Atmel's domestic packaging facility manufactures commercial, industrial, Class B and modified Class S level product.

Packaging Options

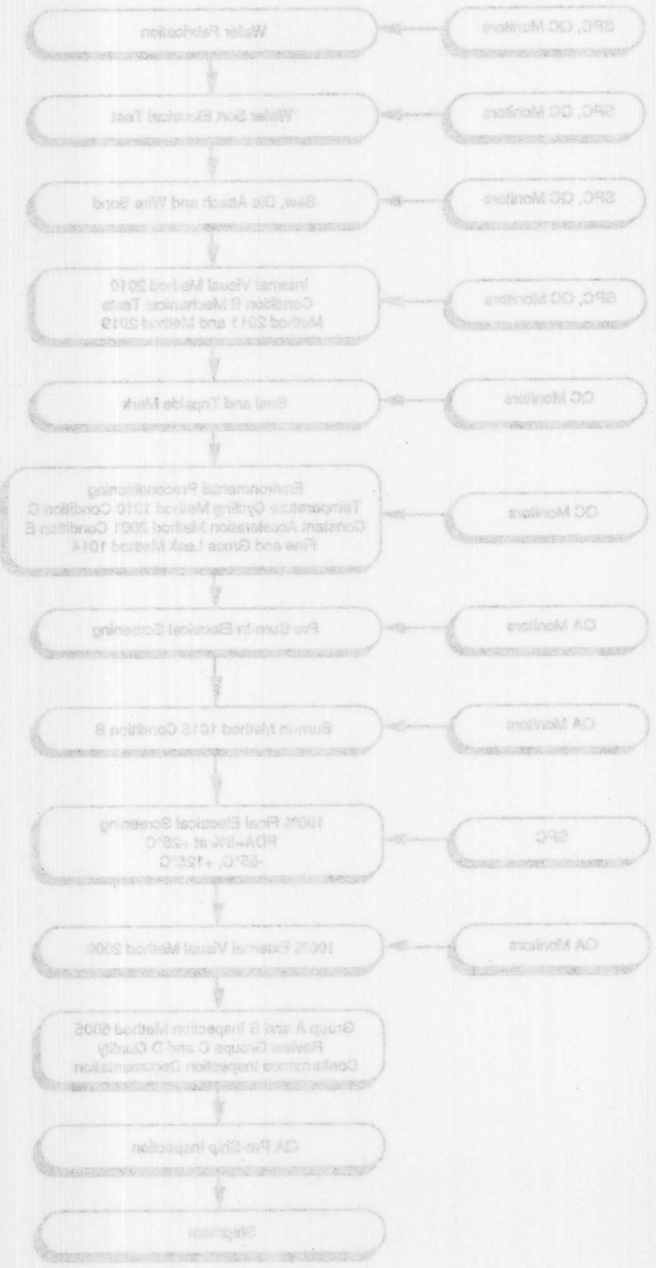
Package Type	Pin Count
TQFP	44, 48, 64, 80, 100, 144, 160, 208, 240, 248, 304
PQFP	44, 64, 68, 80, 100, 120, 128, 132, 136, 144, 160, 184, 208, 232, 256, 304
PLCC	28, 44, 68, 84
PPGA	68, 84, 100, 120, 132, 144, 180, 224
CPGA	64, 68, 84, 100, 124, 144, 155, 180, 223, 224, 256, 299, 391
CQFP	64, 68, 84, 132, 160, 224, 340
CLCC	44, 52, 84, 132, 148, 196
TAB	68, 100, 120, 128, 144, 160, 180, 208, 224, 256, 292, 304, 338, 360

Military Product Flow Chart
MIL-STD-883 Class B



8

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Converting FPGAs and EPLDs to Atmel's ATL Series Gate Arrays

Introduction

Atmel is the only company which designs and manufactures both complex CMOS electrically programmable logic devices (EPLDs) and high-performance CMOS gate arrays. In a natural progression, Atmel now offers a seamless, direct conversion for designs implemented on most EPLDs and field programmable gate arrays (FPGAs) to the ATL series gate arrays. FPGA/EPLD conversions provide the following benefits:

- You can save money. Atmel's process converts a single FPGA or EPLD into a lower-priced gate array that is a pin-for-pin compatible, drop-in replacement. In other words, Atmel will match the timing of the FPGA or EPLD, at a lower cost.
- You can reduce board space. Since Atmel converts to a true gate array, multiple FPGA/EPLDs can be easily integrated into a single chip, reducing board space and component cost.
- Atmel can also take an existing FPGA/EPLD design and improve system performance.
- Save time and prove your design. Your ASIC design can be prototyped in programmable logic and moved to a gate array, without redesign.

In all cases, Atmel uses the FPGA/EPLD design database so that little engineering effort is required from the customer. This document details the information needed to perform a conversion. It also discusses when a conversion makes sense.

Table 1. ATL Series Gate Arrays

Device Number	Maximum Gates	Routable Gates	Max Pin Count	Max I/O Pins	Gate[1] Speed
ATL4	4,100	2,600	68	60	434 ps
ATL10	10,000	6,500	124	116	434 ps
ATL20/20C	22,000	12,000	144/160	136/148	434 ps
ATL40	40,000	22,000	180	168	434 ps
ATL60	57,000	30,000	224	208	434 ps
ATL75	72,000	38,000	256	236	434 ps
ATL100	95,000	50,000	292	262	434 ps
ATL130	131,000	67,000	338	308	434 ps
ATL160	157,000	80,000	360	320	434 ps

Note: 1. Nominal 2 Input Nand Gate With a Fan Out of 2

FPGA/EPLD to Gate Array Conversion

Application Note

8

Programmable Logic vs. Gate Array

Programmable logic has enjoyed tremendous popularity over the past several years because the user saves both time and money. Users may work with inexpensive design tools, run on inexpensive platforms. Designs can be implemented in hours and modified easily. As a result, a designer can implement an ASIC design and evaluate performance in the system in the same week. This instant feedback allows designers to rectify system errors without additional cost. Programmable logic provides an ideal solution for low- to moderate- volume designs or for fast prototyping.

Gate arrays continue to offer superior performance, higher densities and lower cost-per-gate in volume production when compared to an FPGA/EPLD. While the cost of design tools has dropped in recent years and quality third party tools have emerged, they are still more expensive than FPGA/EPLD tools. Also, while gate array prototypes can be available in a few weeks, that is still much longer than the several hour turn around of an FPGA/EPLD.

When to Convert

There are four instances when converting from an FPGA/EPLD to a gate array offers the user a direct benefit.

1. High Volume - If your annual volume is over 10,000 units (commercial) for a single design, or 2,000 units for combined designs (commercial), converting to a gate array can save money.

2. Performance - Gate arrays have lower stand-by current requirements and offer greater speed than an FPGA/EPLD. Frequently the speed of an FPGA/EPLD becomes the limiting factor in a system design.

3. Integration - Converting to a true gate array allows several FPGA/EPLDs to be integrated into a single chip, requiring less board space and providing a cost savings.

4. Prototyping - Using the FPGA/EPLD for prototyping and then converting into a gate array for production gives the user the best of both worlds; fast design cycle times and low-cost volume production.

The Conversion Process Summary

Atmel's conversion process is designed to minimize the amount of engineering support required from the system designers. Figure 1 outlines the conversion process flow. The inputs required vary depending on the original manufacturer of the FPGA/EPLD.

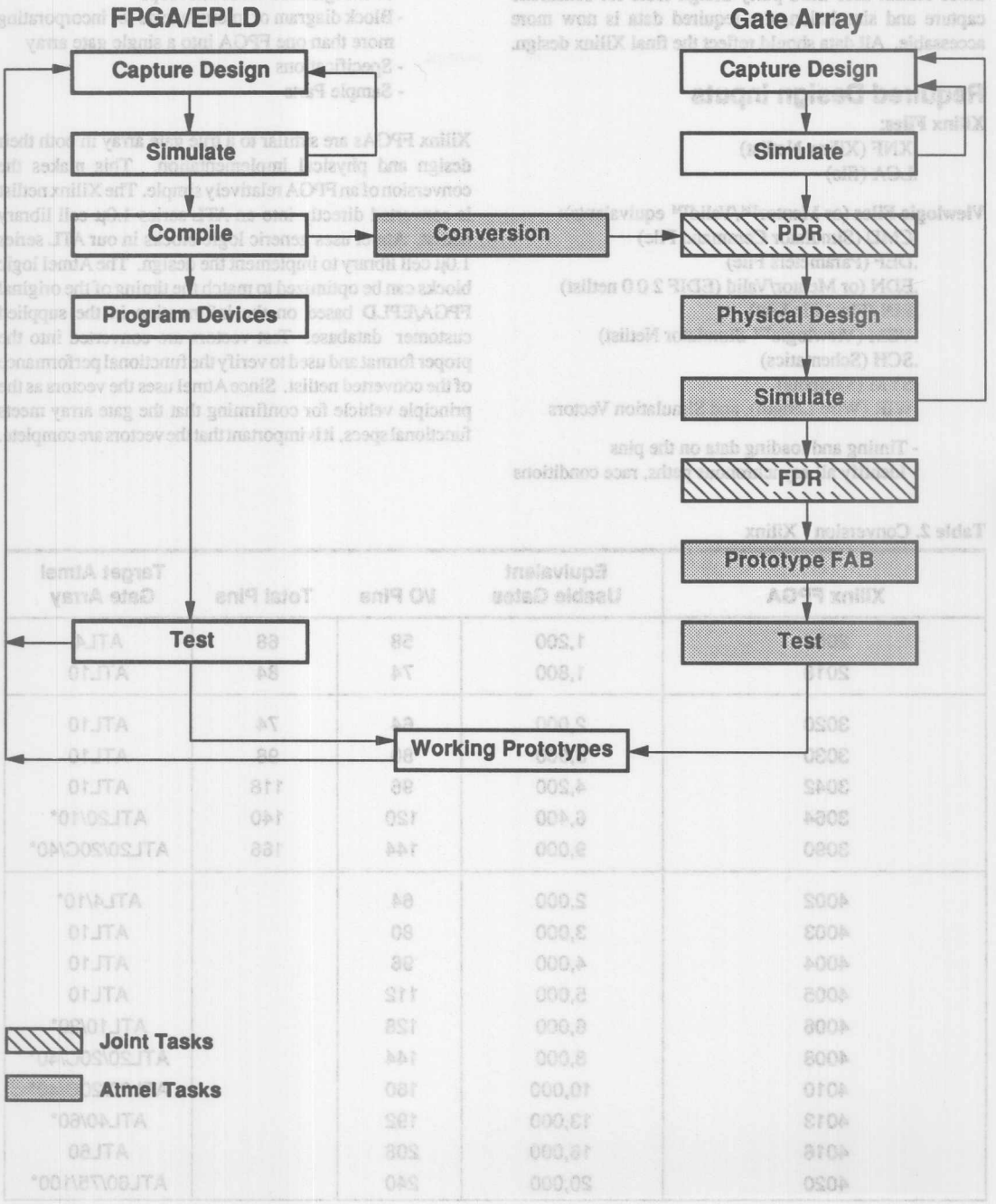
Once Atmel has received the design database, the original design (s) is converted into an equivalent netlist using the ATL series library. The equivalent netlist ensures that both the functionality and timing of the new design match the original. Using this technique, almost any FPGA/EPLD design can be converted to a gate array.

The original test vectors are also converted and are used to verify the gate array design. This is important because the functional test vectors are the verification vehicle for the design. Good functional vectors must be provided or developed. After the design has been converted and verified for functional performance, the optimization process begins. The design can be optimized to match the timing performance of the original FPGA/EPLD design, or to meet new performance goals. Additional logic functions or memory can be added to the gate array as well.

Before physical design of the chip begins, a joint Preliminary Design Review is held with Atmel and the customer to approve the results of the converted design. From this point on the design process is identical to that of a traditionally designed gate array. The design is physically placed and routed on the gate array and verified for electrical and design rules. Atmel uses Cadence's Verilog-XL™ as a golden simulator. Atmel provides performance equal to that predicted by Verilog-XL.

Back annotation data is extracted from the actual layout and incorporated into the post-route functional and timing simulation. Minor layout modifications may be required to meet the timing specification. A Final Design Review is held to approve the post-route simulation data. After customer approval, the design is released for mask generation and prototyping. Prototypes can be delivered in as little as three weeks and production units in as short as six weeks after customer approval of prototypes. Atmel guarantees the gate array will be a pin-for-pin compatible replacement for the FPGA/EPLD.

Figure 1. FPGA/EPLD to Gate Array Conversion



Conversion - Xilinx™ FPGA

Since Xilinx uses third party design tools for schematic capture and simulation, the required data is now more accessable. All data should reflect the final Xilinx design.

Required Design Inputs

Xilinx Files:

.XNF (Xilinx Netlist)
.LCA (file)

Viewlogic Files (or Mentor™/Valid™ equivalents):

.CMD (Simulator Command File)
.DEF (Parameters File)
.EDN (or Mentor/Valid (EDIF 2 0 0 netlist)
.PIN (Final Pin List)
.VSM (Viewlogic™ Simulator Netlist)
.SCH (Schematics)
.SYM (Symbols)
.WIR (Wire Length), and Simulation Vectors

- Timing and loading data on the pins
- Identify all asynchronous paths, race conditions or unregistered feedback loops
- Block diagram of interconnects for incorporating more than one FPGA into a single gate array
- Specifications
- Sample Parts

Xilinx FPGAs are similar to a true gate array in both their design and physical implementation. This makes the conversion of an FPGA relatively simple. The Xilinx netlist is converted directly into an ATL series 1.0µ cell library netlist. Atmel uses generic logic blocks in our ATL series 1.0µ cell library to implement the design. The Atmel logic blocks can be optimized to match the timing of the original FPGA/EPLD based on the information in the supplied customer database. Test vectors are converted into the proper format and used to verify the functional performance of the converted netlist. Since Atmel uses the vectors as the principle vehicle for confirming that the gate array meets functional specs, it is important that the vectors are complete.

Table 2. Conversion - Xilinx

Xilinx FPGA	Equivalent Usable Gates	I/O Pins	Total Pins	Target Atmel Gate Array
2064	1,200	58	68	ATL4
2018	1,800	74	84	ATL10
3020	2,000	64	74	ATL10
3030	3,000	80	98	ATL10
3042	4,200	96	118	ATL10
3064	6,400	120	140	ATL20/10*
3090	9,000	144	166	ATL20/20C/40*
4002	2,000	64		ATL4/10*
4003	3,000	80		ATL10
4004	4,000	96		ATL10
4005	5,000	112		ATL10
4006	6,000	128		ATL10/20*
4008	8,000	144		ATL20/20C/40*
4010	10,000	160		ATL20/20C/40*
4013	13,000	192		ATL40/60*
4016	16,000	208		ATL60
4020	20,000	240		ATL60/75/100*

Note: *Target array dependent on number of pins used.

Conversion - Actel™ FPGA

Since Actel uses only third party design tools for schematic capture and simulation, the required data should already be in the correct format for delivery to Atmel. All data should reflect the final Actel design.

Required Design Inputs

Actel Files:

.ADL (Flatten Netlist)
.CRT (Criticality file)
.DEL (Actel Delay Table)
.FUS (Fuse File)
.IPF (Initial Placement File)

Viewlogic Files (or Mentor/Valid equivalents):

.CMD (Simulator Command File)
.DEF (Parameters File)
.EDN (or Mentor/Valid (EDIF 200 netlist)
.PIN (Final Pin List)
.VSM (Viewlogic Simulator Netlist)
.SCH (Schematics)
.SYM (Symbols)
.WIR (Wire Length), and Simulation Vectors

- Timing and loading data on the pins
- Identify all asynchronous paths, race conditions or unregistered feedback loops
- Block diagram of interconnects for incorporating more than one FPGA into a single gate array
- Specifications
- Sample parts

Actel FPGAs are very similar to a true gate array in both their design and physical implementation. This makes the conversion of an FPGA to a gate array relatively simple. The Actel netlist is converted directly into an ATL series 1.0µ cell library netlist. The Actel devices actually use only a few basic logic blocks to implement all of their functions. Atmel uses generic logic blocks in our ATL series 1.0µ cell library to implement the design. The Atmel logic blocks can be optimized to match the timing of the original FPGA/EPLD, based on information in the customer design database. The test vectors are converted into the proper format and used to verify the functional performance of the converted netlist. Since Atmel uses the vectors as the principal vehicle for confirming that the gate array meets functional specs, it is important that the vectors are complete.

8

Table 3. Target Atmel Gate Array

Actel FPGA	Equivalent Usable Gates	I/O Pins	Total Pins	Target Atmel Gate Array
Act 1 1010	1,200	57	68	ATL4
1020	2,000	69	84	ATL4 or 10*
Act 2 1225	2,500	82	100	ATL4 or 10*
1240	4,000	104	132	ATL10 or 20*
1280	8,000	140	176	ATL20

Note: *Target array dependent on number of pins used.

Conversion - Altera™ EPLD

Using Altera inputs, an EDIF 2 0 0 netlist with actual delay data can be easily extracted. This netlist comes from the MAX+PLUS design system and incorporates the delay data from the fitter/assembler.

Required Design Inputs

MAX+PLUS Files:

Archive File (Menu: File/Project/Archive)
Should contain these files as a minimum:
.GDF (Graphic File)
.TDF (Text File)
.HIF, .FIT (Fitter)
.POF (Programmer Object File)
.SNF (Simulation Netlist File)
.VEC (Simulation Vectors)

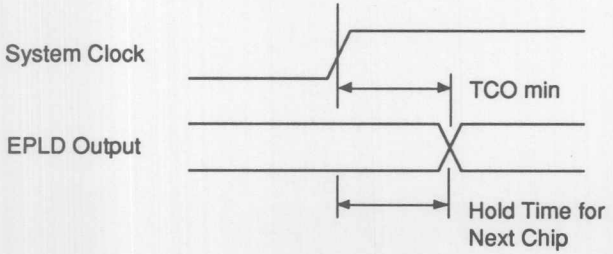
- Timing and loading data on the pins
- Identify all asynchronous paths, race conditions or unregistered feedback loops
- Block diagram of interconnects for incorporating more than one FPGA into a single gate array
- Specifications
- Sample parts

Altera EPLDs have a uniform, deterministic architecture. Every signal traverses the same length path, avoiding race conditions. If the converted design is to be used as a drop-in replacement, the design must meet the specifications of the original design including minimum and maximum signal arrival times as well as set-up and hold times. For example (Figure 2), EPLDs often drive a chip with a

Table 4. Target Atmel Gate Array

Altera EPLD		Equivalent Usable Gates	I/O Pins	Total Pins	Target Atmel Gate Array
Max Series	5016	300	16	20	ATL4
	5032	600	24	28	ATL4
	5064	1200	36	44	ATL4
	5128	2400	60	68	ATL4
	5130	2400	84	100	ATL10
	5192	3500	72	100	ATL10
Classic Series	320/30	150	18	20	ATL4
	610/30/10A	300	20	28	ATL4
	910	450	36	44	ATL4
	1810	900	54	68	ATL4

Figure 2. System Timing Concerns (Positive Hold Times)



positive hold time. A reduction in the minimum clock-to-output timing causes a violation of the hold time. The gate array would run faster than the EPLD, but the system would fail.

The design is mapped into Atmel cells and Synopsys is used to add delay, if needed, to match the original timing. Many potential timing problems disappear using this technique. The original functional test vectors are converted and used to verify that the gate array design is a functional equivalent of the original design.

If the EPLD design is a fully synchronous design, timing optimization can be achieved by meeting the minimum propagation delay for each signal path in the circuit. The maximum signal arrival time for each path in the gate array is specified to be equal to that of the equivalent path in the EPLD. Additional gates may be added to the product and sum terms so the propagation delays of the gate array match those of the original EPLD design.

Synthesis Option

All FPGA/EPLD compilers offer behavioral level simulation. Using logic synthesis, the behavioral level design is mapped into a functionally equivalent circuit and implemented in the ATL series library. The process of synthesis is relatively easy and offers the maximum gate utilization and performance. This technique is used when several FPGA/EPLDs are being converted into a single gate array or if a performance improvement is desired.

Atmel uses Synopsys™ as the synthesis tool of choice. Using Synopsys, the behavioral description of the FPGA/EPLD(s) is synthesized down to a gate level description in the ATL series library. The resulting netlist is a functionally equivalent circuit, equal to the original FPGA/EPLD(s). Synopsys is also used to optimize the design for speed, power usage or gate count.

Use of synthesis allows the FPGA/EPLD(s) to be reduced to the smallest possible gate array implementation. Since the design is not implemented in the same deterministic manner, the timing will generally be different than the original design.

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Translation Of Existing ASIC Designs

ASIC Design Translation

Application Note

8

Introduction

It has only been in the last few years that designers and users of application specific integrated circuits (ASIC) have been able to obtain additional sources for these types of integrated circuits. The introduction of design synthesis software by CAD / CAE companies has made the task of converting from one ASIC vendor's library into another's, a feasible task even for the most dense designs.

The user of an application specific integrated circuit who desires the flexibility and security offered by having multiple sources for what are often key system components, or the user who requires an improvement in performance offered by advanced process technologies, now have an easy path to satisfy their needs. That path is Atmel's Design Translation ASIC design flow, shown in Figure 1. The Design Translation flow highlights the major steps that are taken in converting a netlist into Atmel's gate array cells, verifying the translation, performing the layout and realizing the desired circuit performance, and fabricating and testing the resulting silicon product.

This application note describes the types of data required from the ASIC user and the process steps followed by Atmel to successfully translate an existing ASIC design, and presents the results of two translation efforts. The first was an effort where the Atmel device performance was required to match that of the original ASIC. The second was a translation where the improved performance of Atmel's device was required. The process has been proven through successful translation of designs from such vendors as LSI Logic, NEC, Fujitsu, and Oki, into our 1.0 µ ATL series gate array family.

The Process

Simply stated, the Design Translation process maps cells from the original design into cells contained in Atmel's cell library. These cells may be equivalent primitives or may be soft macros which include several primitives. The choice of Atmel cell will depend upon the required performance objective, and, in some instances, hard macros may be created to replace soft macros to achieve performance goals for the design.

Once the mapping is complete, the process follows Atmel's normal ASIC design flow, including cell placement and routing, resimulation using Atmel's "golden" simulator, comparison of predicted versus desired performance and, after approval of the design by the user, PG tape out and prototype fabrication.

Data Base Required

ASIC design can be accomplished on a variety of platforms, and with a variety of software tools - some open, some proprietary. Designs are completed using generic and/or vendor-specific library cells as well. This level of flexibility available to the ASIC designer does not hinder the translation effort. Most design tools are capable of providing a netlist in EDIF (EDIF 2.0.0) format. Other netlist formats which are acceptable to Atmel are listed below:

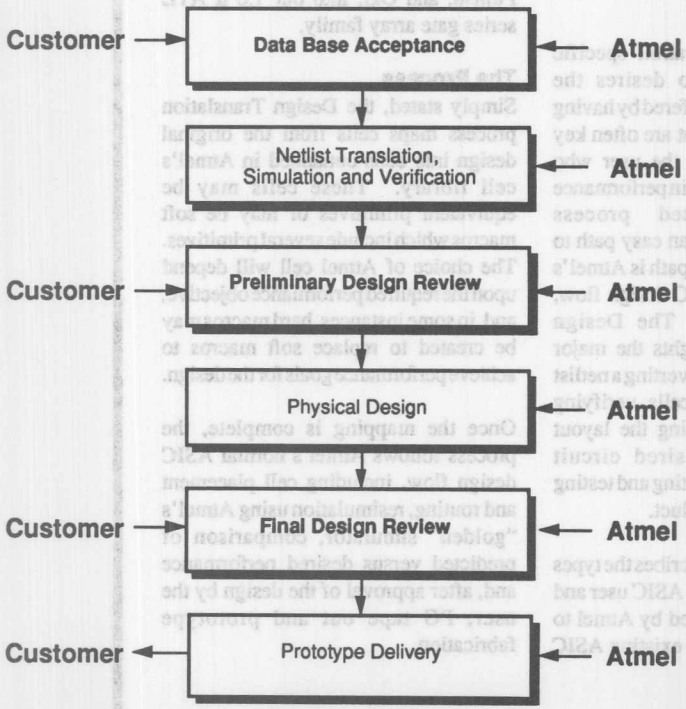
Cadence™ - Verilog-XL™, EDIF 2.0.0
DAZIX™ - Tegas™, EDIF 2.0.0
LSI Logic - NDL™
Mentor™ - MIF™
Racal-Redac™ - EDIF 2.0.0
Valid™ - EDIF 2.0.0
Viewlogic™ - EDIF 2.0.0

In addition to the netlist for the original design, several other pieces of information are needed to successfully translate the design. Also required are:

A description of the original design library
Functional test vectors, print-on-change format
Device specifications
Identification of critical and/or asynchronous paths
"As-routed" delay data from the original design

To make an assessment of whether the desired performance match or improvement has been achieved, an understanding of the starting point must be reached. The description of the original cell library, with its functional and timing information for each cell, is also essential to the definition of the starting point.

Figure 1. Design Translation Flow



If sample parts of the original design can be provided, performance data on the actual silicon can be used to help establish a baseline.

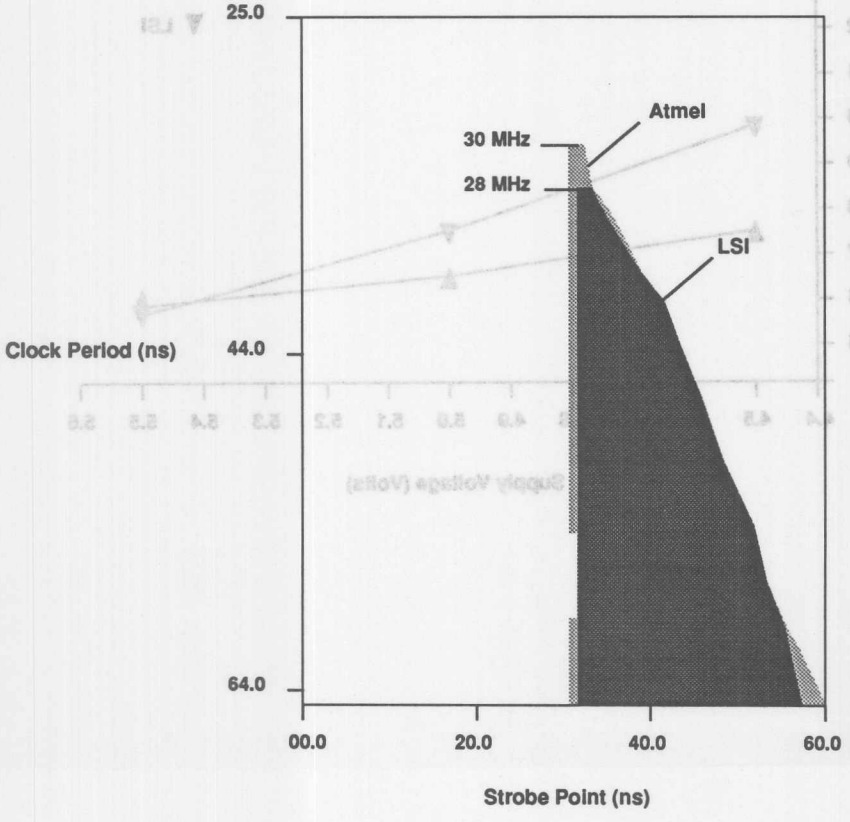
The functional vector set (in ASCII or TSSI, print-on-change format) serves two purposes. The functional vector set, when converted into tester-specific format and used in conjunction with the sample devices, provides a mechanism for establishing detailed performance attributes of the original design. These attributes, such as maximum frequency, path timing performance, and buffer characteristics to name a few, provide the base for cell and buffer selection to match or improve the design. Individual performance attributes can also be used as input to a waveform comparison tool. This tool, using the actual data and the functional test vectors, now converted to simulator format, permits the Atmel designer to determine when and where timing mismatches occur and adjust the netlist accordingly.

The device specification provides key information concerning the required device pin-out, system loading for each pin, the desired performance, and the range of operating conditions.

Performance Matching

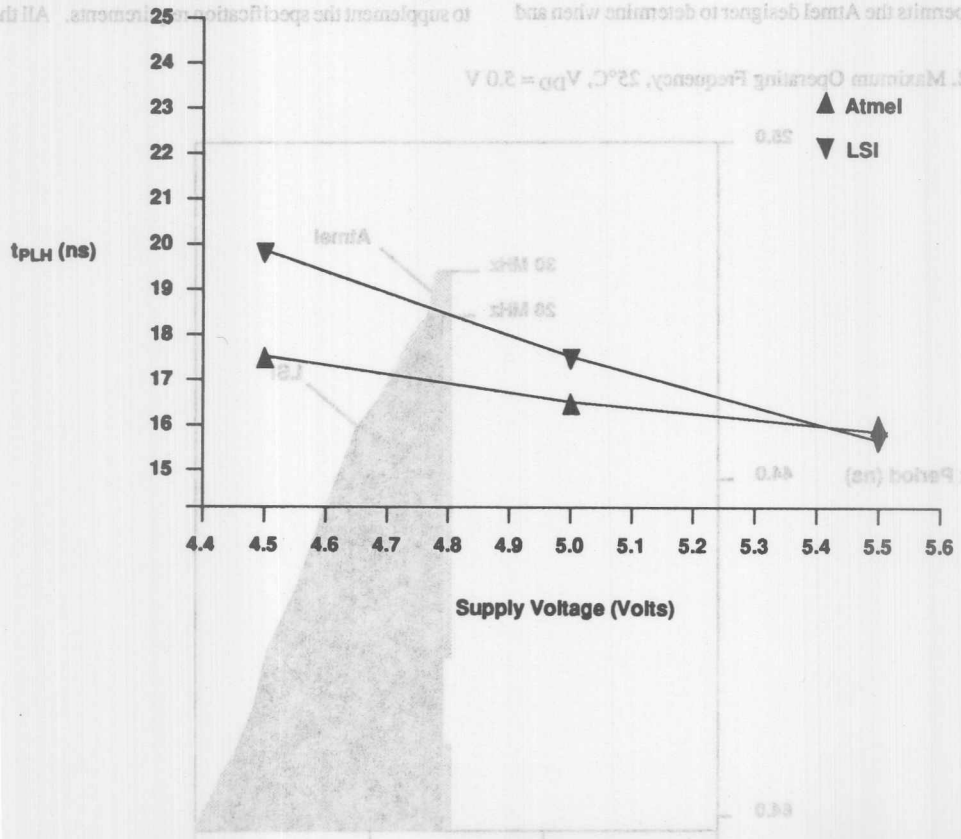
Our first example of ASIC translation presents the results of work performed for a military application, where interchangeability with the original designs was required. The original design was an LSI Logic 10K series gate array of approximately 5,000 gates. The design was asynchronous and had multiple clocks. Samples representing the original designs were available at the outset and were characterized to supplement the specification requirements. All the data

Figure 2. Maximum Operating Frequency, 25°C, V_{DD} = 5.0 V



presented is a direct comparison of LSI Logic and Atmel silicon. Figure 2, depicting maximum operating frequency for constant temperature and voltage, shows how closely the performance can be matched. Figures 3 and 4 depict the average performance for nine critical paths, for low-to-high transitions, both as a function of supply voltage and of temperature. And finally, Figures 5 and 6 depict rise and fall time of bidirectional buffers. The performance match is extremely close.

Figure 3. Atmel vs LSI Package Test Results for 9 Critical Paths, t_{PLH}, +25°C



The customer performed extensive tester-based characterization and qualification of the Atmel device to insure that it was pin-for-pin compatible, drop-in replacement of the original LSI Logic part. The parts were then assembled onto boards and tested again. The Atmel and LSI parts were interchanged and mixed and matched on boards. The complete system evaluation was performed and in all tests the Atmel parts proved to be equal or superior to the LSI gate array.

Figure 4. Atmel vs LSI Package Test Results for 9 Critical Paths, t_{PLH}, V_{DD} = 5.0 V

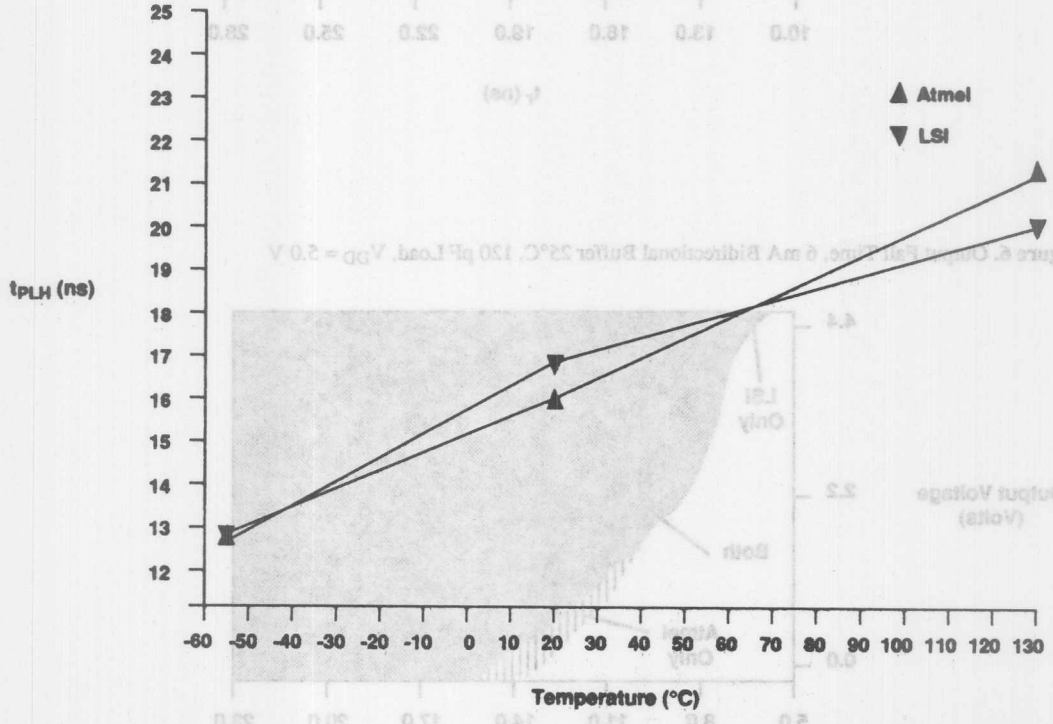


Figure 5. Output Rise Time, 8 mA Bidirectional Buffer, 25°C, 120 pF Load, V_{DD} = 5.0 V

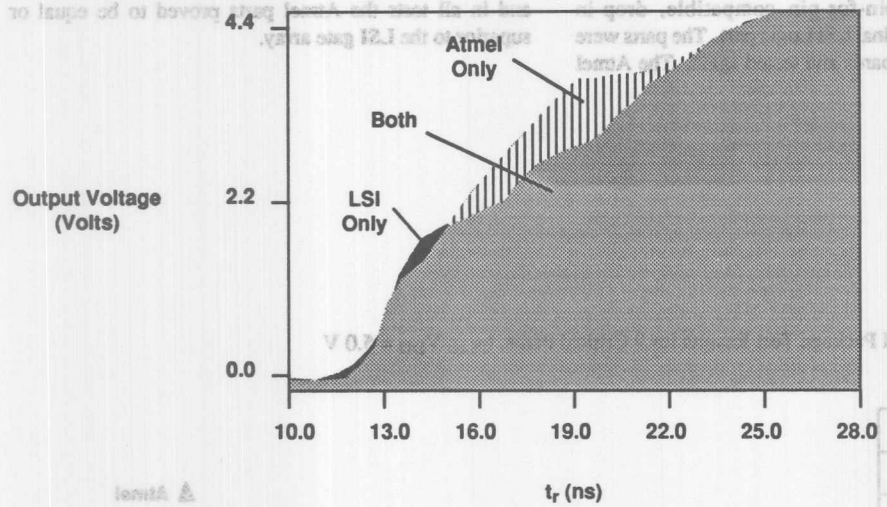
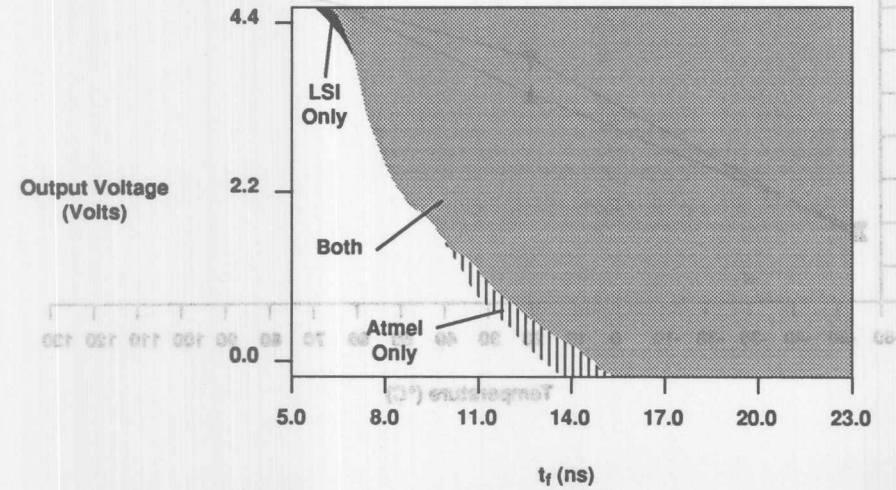


Figure 6. Output Fall Time, 6 mA Bidirectional Buffer 25°C, 120 pF Load, V_{DD} = 5.0 V



Performance Improvement

The second example of ASIC translation presents the results of work performed for a commercial application. This design required approximately 8,000 gates, was completely synchronous, and was operating at 25 MHz. The customer desired an improvement in performance to 33 MHz. To achieve this speed, Atmel compared the performance of its cells to those of the original design, as samples were not available. This evaluation indicated that a 30 to 35 percent speed improvement could be realized over the existing design. Atmel also employed higher drive cells where appropriate to further enhance performance. Extensive board level testing, performed by the customer, confirmed that the Atmel implementation exceeded the 33 MHz design goal over the rated voltage and temperature ranges.

Atmel's CMOS Gate Array Design Manual provides more detailed information about the gate arrays, design methodologies, and individual cell timing, and should be used as a reference for evaluating ASIC performance.

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Introduction

The ATL series gate arrays use a library of highly accurate cells implemented on an advanced 1.0µ (drawn) CMOS process. The cell library contains over 110 hard-wired cells which have been characterized through SPICE modeling at the transistor level. The cells have also been verified through measurements made on test arrays over commercial and military temperature and voltage ranges. The 1.0µ CMOS process is under strict statistical process control to ensure that the simulations will accurately predict the performance of the fabricated gate arrays.

The cell library contains both standard and high drive cells. Also included are scan cells, and all the cells required to implement IEEE 1149.1 (JTAG) boundary scan architecture as well as other testability schemes. New cells are being added to the library on a regular basis. Check with your Atmel sales representative for the latest list.

ATL Series Gate Array 1.0µ CMOS Cell Library Index

Cell Index (Worst Delays at Tj = 25°C; Vdd = 5.0V; Input Rise and Fall Times = 1ns; Process = Nominal)

Macrocells in alpha-numeric order

Cell Name	Cell Description	Cell Sites	Input Signal	Output Rising Base (ns)	Output Rising Load Factor (ns/FO)	Output Falling Base (ns)	Output Falling Load Factor (ns/FO)
ADD3	1 Bit Adder	6	P	1.681	0.121	1.782	0.110
			Q	0.652	0.103	0.725	0.073
			CI	0.728	0.091	0.785	0.069
ADD3X	1 Bit Adder with buffered outputs	4	P	1.245	0.060	1.387	0.050
			Q	1.243	0.062	1.164	0.048
			CI	0.772	0.059	0.714	0.050
AND2	2 Input AND	1	A, B	0.485	0.056	0.501	0.043
AND2H	2 Input AND (high drive)	1	A, B	0.554	0.028	0.564	0.024
AND3	3 Input AND	2	A - C	0.689	0.058	0.572	0.046
AND3H	3 Input AND (high drive)	2	A - C	0.732	0.032	0.618	0.025
AND4	4 Input AND	2	A - D	0.806	0.063	0.642	0.043
AND4H	4 Input AND (high drive)	2	A - D	0.861	0.038	0.647	0.026
AND5	5 Input AND	2	A - E	0.440	0.138	0.447	0.046
AOI22	3 Input AND OR INVERT	1	A - C	0.435	0.105	0.348	0.063
AOI22H	3 Input AND OR INVERT (high drive)	2	A - C	0.405	0.048	0.275	0.035
AOI222	4 Input AND OR INVERT	2	A - D	0.608	0.105	0.517	0.065
AOI222H	4 Input AND OR INVERT (high drive)	2	A - D	0.406	0.038	0.428	0.032
AOI2223	6 Input AND OR INVERT	2	A - F	0.647	0.105	0.643	0.064
AOI2223H	6 Input AND OR INVERT (high drive)	4	A - F	0.892	0.061	0.780	0.044
BUF1	1x Buffer	1	I	0.372	0.054	0.450	0.040
BUF2	2x Buffer	1	I	0.461	0.026	0.512	0.021
BUF2T	2x Buffer w/ Enable	2	I	0.536	0.082	0.676	0.048
			E	0.416	0.080	0.257	0.058
BUF2Z	2x Buffer w/ Enable Low	2	I	0.534	0.081	0.677	0.049
			E	0.167	0.061	0.282	0.032
BUF3	3x Buffer	2	I	0.495	0.020	0.547	0.019

Cell Name	Cell Description	Cell Sites	Input Signal	Output Rising Base (ns)	Output Rising Load Factor (ns/FO)	Output Falling Base (ns)	Output Falling Load Factor (ns/FO)
BUF4	4x Buffer	2	I	0.549	0.016	0.624	0.014
BUF8	8x Buffer	3	I	0.557	0.007	0.636	0.006
BUF12	12x Buffer	4	I	0.565	0.005	0.643	0.004
BUF16	16x Buffer	5	I	0.545	0.004	0.618	0.003
CLA7X	7 Input Carry Lookahead	2	A - G	0.816	0.230	0.531	0.105
DEC4	2:4 Decoder	4	S0, S1	0.414	0.055	0.430	0.063
DEC4N	2:4 Decoder w/ Enable Low	4	S0, S1	0.868	0.061	0.769	0.066
			E	0.449	0.061	0.630	0.065
DEC8N	3:8 Decoder w/ Enable Low	12	S0, S1, S2	1.303	0.059	1.481	0.084
			E	0.767	0.058	1.194	0.086
DFF	D Flip-flop	5	CLK	1.009	0.058	0.934	0.048
DFFBCPX	D Flip-flop w/ Clear and Preset	6	CLK	1.218	0.179	1.405	0.194
			C	1.156	0.175	0.553	0.041
			P	1.151	0.175	0.687	0.043
DFFBSRX	D Flip-flop w/ Set and Reset	6	CLK	1.350	0.179	1.309	0.153
			S	0.480	0.056	1.008	0.152
			R	0.623	0.057	1.092	0.154
DFFC	D Flip-flop w/ Clear	5	CLK	1.069	0.063	0.916	0.049
			C	—.—	—.—	0.896	0.048
DFFH	D Flip-flop (high drive)	5	CLK	1.059	0.029	0.946	0.027
DFFR	D Flip-flop w/ Reset	5	CLK	1.079	0.061	0.924	0.049
			R	—.—	—.—	1.215	0.050
DFFS	D Flip-flop w/ Set	5	CLK	1.006	0.058	0.968	0.057
			S	0.754	0.058	—.—	—.—
DFFSR	D Flip-flop w/ Set and Reset	5	CLK	1.113	0.104	1.009	0.055
			S	0.855	0.104	—.—	—.—
			R	—.—	—.—	0.346	0.043
DLY2000	Delay Buffer 2.0 ns	3	I	2.315	0.058	2.166	0.067
DLY3500	Delay Buffer 3.5 ns	5	I	3.388	0.052	3.542	0.059
DLY8000	Delay Buffer 8.0 ns	11	I	8.011	0.052	7.637	0.060
DSS	Set Scan Register	6	CLK	0.826	0.069	0.920	0.045

Cell Name	Cell Description	Cell Sites	Input Signal	Output Rising Base (ns)	Output Rising Load Factor (ns/FO)	Output Falling Base (ns)	Output Falling Load Factor (ns/FO)
DSSBCPY	Set Scan Register w/ Clear and Preset	11	CLK	1.053	0.069	1.253	0.066
			C	0.773	0.070	1.222	0.049
			P	0.709	0.068	1.304	0.055
DSSBR	Set Scan Register w/ Reset	9	CLK	1.442	0.075	1.430	0.060
			R	0.444	0.070	0.713	0.044
DSSBS	Set Scan w/ Set	10	CLK	1.563	0.041	1.696	0.032
			S	1.680	0.028	1.281	0.029
DSSR	Set Scan Register w/Reset	7	CLK	0.855	0.072	0.899	0.047
			R	—.—	—.—	0.786	0.046
DSSS	Set Scan Register w/Set	7	CLK	0.833	0.067	0.960	0.046
			S	0.929	0.066	—.—	—.—
DSSSR	Set Scan Register w/Set and Reset	8	CLK	0.874	0.072	1.036	0.051
			R	—.—	—.—	0.755	0.051
			S	0.393	0.070	—.—	—.—
INV1	1x Inverter	1	I	0.250	0.055	0.193	0.045
INV1D	Dual 1x Inverter	1	I0, I1	0.250	0.055	0.193	0.045
INV1Q	Quad 1x Inverter	2	I0 - I3	0.250	0.055	0.193	0.045
INV1TQ	Quad Tri-state Inverter	5	I0 - I3	0.199	0.107	0.225	0.064
			E0, E1	0.450	0.107	0.558	0.064
INV2	2x Inverter	1	I	0.238	0.030	0.168	0.026
INV2D	Dual 2x Inverter	2	I0, I1	0.238	0.030	0.168	0.026
INV2T	2x Tristate Inverter	2	I	0.345	0.048	0.305	0.036
			E	0.287	0.047	0.217	0.041
INV3	3x Inverter	1	I	0.227	0.022	0.154	0.020
INV4	4x Inverter	1	I	0.214	0.017	0.153	0.016
INV8	8x Inverter	2	I	0.178	0.010	0.113	0.010
INV10	10x Inverter	4	I	0.895	0.005	0.858	0.004
JKF	JK Flip-flop	6	CLK	1.067	0.057	0.981	0.047
JKFBCPX	JK Flip-flop w/ Clear and Preset	8	CLK	1.849	0.061	1.616	0.051
			C	1.280	0.068	0.546	0.050
			P	1.263	0.068	0.774	0.051
JKFC	JK Flip-flop w/ Clear	6	CLK	1.125	0.063	0.947	0.048
			CLR	_._	_._	0.970	0.047

Cell Name	Cell Description	Cell Sites	Input Signal	Output Rising Base (ns)	Output Rising Load Factor (ns/FO)	Output Falling Base (ns)	Output Falling Load Factor (ns/FO)
LAT	LATCH	3	D	0.711	0.057	0.817	0.047
			H	0.904	0.057	0.730	0.046
LATB	LATCH w/Complementary Output	3	D	1.053	0.059	0.920	0.049
			H	1.494	0.059	1.225	0.050
LATBG	LATB w/ Inverted Gate Signal	3	D	1.155	0.059	1.024	0.050
			G	1.256	0.062	1.418	0.051
LATBGQ	QUAD LATBG w/ Common Gate Signal	9	D0 - D3	1.088	0.059	0.888	0.048
			G	1.278	0.059	1.517	0.052
LATBH	LATCH (high drive)	4	D	1.182	0.032	1.027	0.030
			H	1.498	0.032	1.266	0.033
LATIQ	Quad Inverting LATCH	7	D0 - D3	0.414	0.054	0.347	0.046
			H	1.009	0.055	1.233	0.043
LATR	LATCH w/ Reset	3	D	0.843	0.102	0.875	0.047
			H	1.012	0.102	0.794	0.047
			R	–.–	–.–	0.352	0.043
LATS	LATCH w/ Set	3	D	0.751	0.058	1.169	0.053
			H	0.911	0.058	0.961	0.055
			S	0.839	0.058	–.–	–.–
LATSR	LATCH w/ Set and Reset	3	D	0.876	0.102	1.166	0.054
			H	1.019	0.102	0.971	0.056
			S	0.864	0.105	—.—	—.—
			R	—.—	—.—	0.352	0.042
MUX2	2:1 MUX	2	I0, I1	0.664	0.058	0.786	0.049
			S	0.611	0.058	0.613	0.048
MUX2H	2:1 MUX (high drive)	2	I0, I1	0.651	0.029	0.770	0.027
			S	0.843	0.029	0.874	0.026
MUX2I	Inverting 2:1 MUX w/o Buffered Inputs	2	I0, I1	0.391	0.072	0.313	0.050
			S	0.612	0.075	0.548	0.043
MUX2IH	Inverting 2:1 MUX w/o Buffered Inputs (high drive)	2	I0, I1	0.371	0.039	0.269	0.033
			S	0.638	0.035	0.528	0.026
MUX2N	2:1 MUX w/ Enable Low	2	I0, I1	0.742	0.103	0.806	0.050
			S	0.688	0.103	0.636	0.048
			E	0.355	0.099	0.298	0.044
MUX2NQ	Quad 2:1 MUX w/ Enable Low	8	S	1.194	0.106	1.139	0.049
			E	0.813	0.105	0.767	0.047
			I	0.786	0.104	0.907	0.048

Cell Name	Cell Description	Cell Sites	Input Signal	Output Rising Base (ns)	Output Rising Load Factor (ns/FO)	Output Falling Base (ns)	Output Falling Load Factor (ns/FO)
MUX2Q	Quad 2:1 MUX	6	I	0.667	0.058	0.806	0.050
			S	1.059	0.056	1.065	0.050
MUX3I	Inverting 3:1 MUX w/o Buffered Inputs	3	I0 - I2	0.558	0.104	0.435	0.063
			S0, S1	0.649	0.104	0.619	0.063
MUX3IH	Inverting 3:1 MUX w/o Buffered Inputs (high drive)	4	I0 - I2	0.559	0.047	0.433	0.033
			S0, S1	0.624	0.049	0.602	0.031
MUX4	4:1 MUX	4	I0 - I3	1.091	0.065	1.324	0.059
			S0, S1	1.135	0.068	1.385	0.061
MUX4X	4:1 MUX w/o Buffered Inputs	5	I0 - I3	0.645	0.050	0.758	0.043
			S0, S1	0.953	0.058	1.050	0.047
MUX4XH	4:1 MUX w/o Buffered Inputs (high drive)	5	I0 - I3	0.680	0.028	0.789	0.026
			S0, S1	0.953	0.028	1.074	0.029
MUX5H	5:1 MUX (high drive)	7	I0 - I4	1.491	0.030	1.557	0.029
			S0 - S2	1.770	0.033	2.132	0.027
MUX8	8:1 MUX	10	I0 - I7	1.588	0.072	1.862	0.070
			S0 - S2	2.302	0.074	2.527	0.075
MUX8N	8:1 MUX w/ Enable Low	10	I0 - I7	1.753	0.110	1.833	0.075
			E	0.349	0.102	0.290	0.044
			S0 - S2	2.378	0.109	2.578	0.073
MUX8XH	8:1 MUX (high drive)	10	I0 - I7	1.014	0.036	1.152	0.033
			S0 - S2	1.598	0.035	1.772	0.035
NAN2	2 Input NAND	1	A, B	0.290	0.056	0.257	0.064
NAN2D	Dual 2 Input NAND	2	A0, A1, B0, B1	0.290	0.056	0.257	0.064
NAN2H	2 Input NAND (high drive)	1	A, B	0.281	0.033	0.229	0.035
NAN3	3 Input NAND	1	A - C	0.394	0.051	0.403	0.080
NAN3H	3 Input NAND (high drive)	2	A - C	0.377	0.031	0.328	0.041
NAN4	4 Input NAND	1	A - D	0.429	0.054	0.578	0.101
NAN4H	4 Input NAND (high drive)	2	A - D	0.354	0.029	0.453	0.050
NAN5	5 Input NAND	3	A - E	0.772	0.055	1.035	0.048
NAN5H	5 Input NAND (high drive)	3	A - E	0.818	0.029	1.089	0.029

Cell Name	Cell Description	Cell Sites	Input Signal	Output Rising Base (ns)	Output Rising Load Factor (ns/FO)	Output Falling Base (ns)	Output Falling Load Factor (ns/FO)
NAN6	6 Input NAND	3	A - F	0.841	0.056	1.085	0.047
NAN6H	6 Input NAND (high drive)	3	A - F	0.879	0.030	1.132	0.029
NAN8	8 Input NAND	3	A - H	0.813	0.054	1.061	0.047
NAN8H	8 Input NAND (high drive)	3	A - H	0.911	0.029	1.223	0.029
NOR2	2 Input NOR	1	A, B	0.345	0.100	0.290	0.044
NOR2D	Dual 2 Input NOR	2	A0, A1, B0, B1	0.345	0.100	0.290	0.044
NOR2H	2 Input NOR (high drive)	1	A, B	0.297	0.046	0.211	0.027
NOR3	3 Input NOR	1	A - C	0.477	0.151	0.312	0.044
NOR3H	3 Input NOR (high drive)	2	A - C	0.447	0.070	0.270	0.028
NOR4	4 Input NOR	1	A - D	0.736	0.196	0.342	0.045
NOR4H	4 Input NOR (high drive)	2	A - D	0.612	0.094	0.304	0.026
NOR5	5 Input NOR	3	A - E	1.007	0.057	0.714	0.043
NOR8	8 Input NOR	3	A - H	1.263	0.057	0.729	0.044
NOR16H	16 Input NOR (high drive)	6	I0 - I15	1.724	0.037	0.866	0.026
OAI22	3 Input OR AND INVERT	1	A - C	0.466	0.104	0.378	0.063
OAI22H	3 Input OR AND INVERT (high drive)	2	A - C	0.348	0.049	0.337	0.033
OAI222	4 Input OR AND INVERT	2	A - D	0.566	0.098	0.584	0.069
OAI222H	4 Input OR AND INVERT (high drive)	2	A - D	0.448	0.049	0.256	0.035
OAI22224	8 Input OR AND INVERT	3	A - H	1.067	0.057	1.070	0.047
OAI23	4 Input OR AND INVERT w/ 2 Inputs to AND	1	A - D	0.473	0.099	0.555	0.083
ORR2	2 Input OR	1	A, B	0.493	0.054	0.618	0.046
ORR2H	2 Input OR (high drive)	1	A, B	0.534	0.027	0.699	0.026
ORR3	3 Input OR	2	A - C	0.498	0.056	0.836	0.052
ORR3H	3 Input OR (high drive)	2	A - C	0.553	0.030	0.959	0.031

Cell Name	Cell Description	Cell Sites	Input Signal	Output Rising Base (ns)	Output Rising Load Factor (ns/FO)	Output Falling Base (ns)	Output Falling Load Factor (ns/FO)
ORR4	4 Input OR	2	A - D	0.566	0.059	1.217	0.059
ORR4H	4 Input OR (high drive)	2	A - D	0.590	0.031	1.344	0.036
ORR5	5 Input OR	2	A - E	0.588	0.054	0.701	0.088
XNR2	2 Input Exclusive NOR	2	A, B	0.456	0.100	0.508	0.062
XNR2H	2 Input Exclusive NOR (high drive)	2	A, B	0.866	0.031	0.898	0.028
XOR2	2 Input Exclusive OR	2	A, B	0.693	0.099	0.640	0.065
XOR2H	2 Input Exclusive OR (high drive)	2	A, B	0.698	0.032	0.713	0.030

I/O cells

Sample of buffers composed of modular I/O building blocks

Cell Name	Cell Description	Input Signal	Output Rising Base (ns)	Output Rising *Load Factor	Output Falling Base (ns)	Output Falling *Load Factor
PDIabccde	Input Buffers					
PDICbcce		P	0.434	0.00770	0.403	0.00680
PDICbccSe			1.741	0.01000	2.041	0.00900
PDITbcce			0.323	0.00872	0.646	0.00984
PDITbccSe			1.102	0.00900	2.562	0.00900
PDIabccdeI	Inverting Input Buffers					
PDICbcceI		P	0.100	0.02069	0.093	0.02476
PDabb	Output Buffers					
PDO21		AO	1.429	0.06543	1.179	0.07107
PDO4			0.587	0.03240	0.712	0.03600
PDO51			1.037	0.02678	1.085	0.02734
PDO61			0.670	0.02620	0.854	0.02390
PDO71			0.755	0.02553	0.867	0.02099
PDT3			1.720	0.04349	1.260	0.04865
PDT4			1.775	0.03270	1.372	0.03630
PDK3	Clock Buffer	I	0.498	0.00274	0.435	0.00312
PDT3		E0	1.665	0.04358	0.862	0.04870
PDT4			1.789	0.03270	0.941	0.03660
PDT3		E1	1.628	0.04348	1.131	0.04870
PDT4			1.742	0.03260	1.222	0.03660
PDBaabcddef	Bi-directional Buffers					
PDBaaCcddf		P	0.434	0.00770	0.403	0.00680
PDBaaTcddf			0.323	0.00872	0.646	0.00984
PDB2Ccddef		AO	1.601	0.06520	1.218	0.07120
PDB2Tcddef			1.601	0.06520	1.218	0.07120
PDB31Ccddef			1.455	0.06522	1.513	0.04749
PDB3Tcddef			1.720	0.04349	1.260	0.04865
PDB4Ccddef			1.775	0.03270	1.372	0.03630
PDB4Tcddef			1.775	0.03270	1.372	0.03650
PDB52Ccddef			1.777	0.03270	1.428	0.00292
PDB52Tcddef			1.777	0.03270	1.428	0.00292
PDB62Ccddef			1.732	0.02209	1.544	0.02419
PDB62Tcddef			1.732	0.02209	1.544	0.02419
PDB2bcddef		E0	1.554	0.06540	0.772	0.07270
PDB31bcddef			1.431	0.06547	1.218	0.04869
PDB3bcddef			1.665	0.04358	0.862	0.04870
PDB4bcddef			1.789	0.03270	0.941	0.03660
PDB52bcddef			1.790	0.03270	1.036	0.02930
PDB62bcddef			1.796	0.02612	1.132	0.02473

*Load Factor is ns/FO for input and clock buffers and ns/pF for output buffers.

Cell Name	Cell Description	Input Signal	Output Rising Base (ns)	Output Rising *Load Factor	Output Falling Base (ns)	Output Falling *Load Factor
PDB2bcddef		E1	1.523	0.06530	1.040	0.07300
PDB31bcddef			1.389	0.06535	1.372	0.04870
PDB3bcddef			1.628	0.04348	1.131	0.04870
PDB4bcddef			1.742	0.03260	1.222	0.03660
PDB52bcddef			1.743	0.03260	1.300	0.02940
PDB62bcddef			2.216	0.02601	1.362	0.02469
PDBaabcddeN		E2	0.119	0.08686	0.200	0.10140
PDBaabcddeN		AIO	0.148	0.08722	0.133	0.10310
PSBaabcddef	Bi-directional Buffers					
PSBaaCcddef		P	1.741	0.01000	2.041	0.00900
PSBaaTcddef			1.102	0.00900	2.562	0.00900
PSB9CcddS		AO	1.840	0.01503	1.560	0.01564
PSB91CcddS			2.291	0.04360	3.162	0.02118
PSB9TcddS			1.840	0.01503	1.560	0.01564
PSB91TcddS			2.291	0.04360	3.162	0.02118
PSB9bcddef		E0	1.976	0.01503	1.120	0.01664
PSB91bcddef			2.313	0.04369	1.729	0.01910
PADCIabb	Input Buffers					
PADCITbb		P	0.639	0.01130	0.650	0.00906
PADCabc	Output Buffers					
PADCO22		AO	0.969	0.06030	1.116	0.07890
PADCT44			1.015	0.03030	1.119	0.04000
PADCT66			1.040	0.02050	1.095	0.02660
PADCT44		E	1.004	0.02960	1.178	0.04000
PADCT66			1.060	0.01970	1.176	0.02710
PADCBabcdd	Bi-directional Buffers					
PADCBabTdd		P	0.639	0.01130	0.650	0.00906
PADCB22Tdd		AO	0.969	0.06030	1.116	0.07890
PADCB33Tdd			1.018	0.04010	1.145	0.05270
PADCB22Tdd		E	0.976	0.05810	1.135	0.07940
PADCB33Tdd			0.988	0.03950	1.119	0.05330
PADCXabc	Oscillator Buffers					
PADCX22C		PI	0.295	0.06780	0.277	0.07500
PADIabb	Input Buffers					
PADICbb		P	0.959	0.01020	1.077	0.01020
PADITbb			0.639	0.01130	0.650	0.00906

*Load Factor is ns/FO for input buffers and ns/pF for output buffers.

Cell Name	Cell Description	Input Signal	Output Rising Base (ns)	Output Rising *Load Factor	Output Falling Base (ns)	Output Falling *Load Factor
PADOab	Output Buffers					
PADO22 (4 mA)		AO	0.969	0.06030	1.116	0.07890
PADO33 (6 mA)			1.018	0.04010	1.145	0.05270
PADO44 (8 mA)			1.015	0.03030	1.119	0.04000
PADO66 (12 mA)			1.040	0.02050	1.095	0.02660
PADO88 (16 mA)			1.048	0.01586	1.122	0.02009
PADTab	Tri-state Output Buffers					
PADT22 (4 mA)		AO	0.969	0.06030	1.116	0.07890
PADT33 (6 mA)			1.018	0.04010	1.145	0.05270
PADT44 (8 mA)			1.015	0.03030	1.119	0.04000
PADT66 (12 mA)			1.040	0.02050	1.095	0.02660
PADTCC (24 mA)			1.141	0.00995	1.211	0.01313
PADT22 (4 mA)		E	0.976	0.05810	1.135	0.07940
PADT33 (6 mA)			0.988	0.03950	1.119	0.05330
PADT44 (8 mA)			1.004	0.02960	1.178	0.04000
PADT66 (12 mA)			1.060	0.01970	1.176	0.02710
PADTCC (24 mA)			1.085	0.01027	1.082	0.01550
PADBabcdd	Bi-directional Buffers					
PADBabCdd		P	0.959	0.01020	1.077	0.01020
PADabTdd			0.639	0.01130	0.650	0.00906
PADB22cdd (4 mA)		AO	0.969	0.06030	1.116	0.07890
PADB22Tdd (4 mA)			0.969	0.06030	1.116	0.07890
PADB33Tdd (6 mA)			1.018	0.04010	1.145	0.05270
PADB44Tdd (8 mA)			1.015	0.03030	1.119	0.04000
PADB66Tdd (12 mA)			1.040	0.02050	1.095	0.01313
PADB22cdd		E	0.976	0.05810	1.135	0.07940
PADB22Tdd			0.976	0.05810	1.135	0.07940
PADB33Tdd			0.988	0.03950	1.119	0.05330
PADB44Tdd			1.004	0.02960	1.178	0.04000
PADB66Tdd			1.060	0.01970	1.176	0.02710
PADXabc	Oscillator Buffers					
PADX22C		PI	0.959	0.01020	1.077	0.01020

*Load Factor is ns/FO for input buffers and ns/pF for output buffers.

74XX Series Soft Macros

Cell Name	Cell Description MSI Part Number	Similar to MSI Part Number
AT64	4232 And Or Invert	74ALS64
AT74	DFF	74ALS74
AT109	JKBar FF	74ALS109
AT138	3 to 8 Decoder	74ALS138
AT139	Dual 2 to 4 Decoder	74ALS139
AT148	8 to 3 Priority Encoder	74ALS148
AT151	8 to 1 MUX	74ALS151
AT153	4 to 1 MUX	74ALS153
AT157	Quad 2 to 1 MUX	74ALS157
AT158	Quad Inverting 2 to 1 MUX	74ALS158
AT161	4 BIT Binary Counter	74ALS161
AT164	8 BIT Serial in Parallel Out Shift Register	74ALS164
AT166	8 BIT Parallel Load Shift Register	74ALS166
AT169	4 BIT U/D Counter	74ALS169
AT174	Hex DFF	74ALS174
AT194	4 BIT BiDi Shift Register	74ALS194
AT273	Octal DFF	74ALS273
AT280	9 BIT Parity Generator	74ALS280
AT283	4 BIT Fast Adder	74ALS283
AT688	8 BIT Comparator	74ALS688
AT823	9 BIT DFF	74ALS823
AT825	8 BIT DFF	74ALS825
AT85	4 BIT Magnitude Comparator	74ALS85
AT86	Quad 2 Input Ex OR	74ALS86

HDL Macros

Available in Verilog - HDL or VHDL Simulation Models

Function Group (Directory): adder

Cell Name MSI Part Number	Cell Description
c_add	2's complement carry look-ahead adder
c_add12	2's complement carry look-ahead 12 bit adder
c_add16	2's complement carry look-ahead 16 bit adder
c_add20	2's complement carry look-ahead 20 bit adder
c_add24	2's complement carry look-ahead 24 bit adder
c_add28	2's complement carry look-ahead 28 bit adder
c_add32	2's complement carry look-ahead 32 bit adder
c_add4	2's complement carry look-ahead 4 bit adder
c_add8	2's complement carry look-ahead 8 bit adder
cla	Carry look-ahead
cla12	Carry look-ahead for 12 bit adder
cla16	Carry look-ahead for 16 bit adder
cla20	Carry look-ahead for 20 bit adder
cla24	Carry look-ahead for 24 bit adder
cla28	Carry look-ahead for 28 bit adder
cla32	Carry look-ahead for 32 bit adder
cla4	2's complement carry look-ahead 4 bit adder
cla8	2's complement look-ahead for 8 bit adder
g_add16	2's complement group look-ahead 16 bit adder
g_add24	2's complement group look-ahead 24 bit adder
g_add32	2's complement group look-ahead 32 bit adder
g_add8	2's complement group look-ahead 8 bit adder
g_add9	2's complement group look-ahead 9 bit adder
gen_prop	Carry generate and propagate
gen_prop12	Carry generate and propagate for 12 bit adder
gen_prop16	Carry generate and propagate for 16 bit adder
gen_prop20	Carry generate and propagate for 20 bit adder
gen_prop24	Carry generate and propagate for 24 bit adder
gen_prop28	Carry generate and propagate for 28 bit adder
gen_prop32	Carry generate and propagate for 32 bit adder
gen_prop4	Carry generate and propagate for 4 bit adder
gen-prop8	Carry generate and propagate for 8 bit adder
gla16	Group look-ahead for 16 bit adder
gla16x	Group look-ahead of 16 bits for second stage
gla8	Group look-ahead for 8 bit adder
gla8x	Group look-ahead of 8 bits for second stage
gla9	Group look-ahead for 9 bit adder

HDL Macros

Available in Verilog - HDL or VHDL Simulation Models

Function Group (Directory): alu

Cell Name MSI Part Number	Cell Description
alu16a	16 bit arith logic unit
alu16ap	16 bit arith logic unit with parity prediction
alu16op_a	16 bit arith logic unit pre-operation
alu16op_ap	16 bit pre-operation with parity prediction
alu16op_t	16 bit t type alu pre-operation
alu16op_tp	16 bit t type pre_op with parity prediction
alu16tp	16 bit t type alu, with parity prediction
alu32a	32 bit arith logic unit
alu32ap	32 bit arith logic unit with parity prediction
alu32op_a	32 bit arith logic unit pre-operation
alu32op_ap	32 bit pre-operation with parity prediction
alu32op_t	32 bit type t alu pre-operation
alu8a	8 bit arith logic unit
alu8a_dcod	arith logic unit operand decoder
alu8ap	8 bit arith logic unit with parity prediction
alu8op_a	8 bit arith logic unit pre-operation
alu8 op_ap	8 bit arith logic unit parity prediction
alu8t_dcod	t type arith logic unit operand decoder
alu_g16	16 bit adder for alu
alu_g16p	16 bit parity prediction for adder
alu_g32	32 bit group look-ahead adder for alu
alu_g32p	32 bit parity prediction for adder
alu_g8	8 bit adder for alu
alu_g8p	8 bit parity prediction for adder
alu_gl16	16 bit group look-ahead for alu, 1st stage
alu_gl32	32 bit group look-ahead for alu, 1st stage
alu_gl8	8 bit group look-ahead for alu, 1st stage
alu_g1x16	16 bit group look-ahead for alu, 2nd stage
get16msb	One hot 16 bit priority encoder

HDL Macros

Available in Verilog - HDL or VHDL Simulation Models

Function Group (Directory): baud rate generator

Cell Name MSI Part Number	Cell Description
brg16l	Baud Rate Generator, 16 bit prog. (tc latch)
brg 16r	Baud Rate Generator, 16 bit prog. (tc register)
dpll	Digital Phase Lock Loop

Function Group (Directory): comparator

Cell Name MSI Part Number	Cell Description
ecmp	Expandable equality comparator
ecmp12	12 bit equality comparator
ecmp16	16 bit equality comparator
ecmp20	20 bit equality comparator
ecmp24	24 bit equality comparator
ecmp28	28 bit equality comparator
ecmp32	32 bit equality comparator
ecmp4	4 bit equality comparator
ecmp8	8 bit equality comparator
mcmp12	12 bit magnitude comparator
mcmp16	16 bit magnitude comparator
mcmp20	20 bit magnitude comparator
mcmp24	24 bit magnitude comparator
mcmp28	28 bit magnitude comparator
mcmp32	32 bit magnitude comparator
mcmp4	4 bit magnitude comparator
mcmp4i	Internal 4 bit magnitude comparator
mcmp8	8 bit magnitude comparator

HDL Macros

Available in Verilog - HDL or VHDL Simulation Models

Function Group (Directory): counter

Cell Name MSI Part Number	Cell Description
csbda	Synchronous Down Center Asynchronous Preset
csbds	Synchronous Down Center Synchronous Preset
csbdxa	Expandable Synchronous Binary Down Cenetr Asynchronous Preset
csbdxs	Expandable Synchronous Binary Down Center Synchronous Preset
csblda	Synchronous Binary Loadable Down Center Asynchronous Preset
csblds	Synchronous Binary Loadable Down Center Synchronous Preset
csbldxa	Expandable Synchronous Binary Loadable Down Center Asynchronous Preset
csbldxs	Expandable Synchronous Loadable Binary Down Center Sinchronous Preset
csblpa	Sinchronous Binary Loadable Up/Down Center Asynchronous Clear/Preset
csblps	Synchronous Binary Loadable Up/Down Center Synchronous Clear/Preset
csblpxa	Expandable Synchronous Binary Loadable Up Center Asynchronous Clear
csblpxs	Expandable Synchronous Binary Loadable Up Center Synchronous Clear
csblua	Synchronous Binary Loadable Up Center Asynchronous Clear
csblus	Synchronous Binary Loadable Up Center Synchronous Clear
csbluxa	Expandable Synchronous Binary Loadable Up Center Asynchronous Clear
csbluxs	Expandable Synchronous Loadable Binary Up Center Synchronous Clear
csbpa	Synchronous Binary Up/Down Center Asynchronous Clear/Preset
csbps	Synchronous Binary Up/Down Center Synchronous Clear/Preset
csbpxa	Expandable Synchronous Binary Up Center Asynchronous Clear
csbpxs	Expandable Synchronous Binary Up Center Synchronous Clear
csbua	Synchronous Binary Up Center Asynchronous Clear
csbus	Synchronous Binary Up Center Synchronous Clear
csbuxa	Expandable Synchronous Binary Up Center Asynchronous Clear
csbuxs	Expandable Synchronous Binary Up Center Synchronous Clear
csvblu	Synchronous Variable Binary Loadable Up Center
csvblup	Synchronous Variable Binary Loadable Up Center W/Parity
csvblupd	Synchronous Variable Binary Loadable Up Center W/Parity and Difference

HDL Macros

Available in Verilog - HDL or VHDL Simulation Models

Function Group (Directory): fifo

Cell Name MSI Part Number	Cell Description
af_ctl3	Control for 3 deep asynchronous fifo's
af_ctl8	Control for 8 deep asynchronous fifo's
dx8_16s	Data expander for synchronous fifo front end
f16w3da	Asynchronous 16 bit wide, 3 byte deep fifo
f16w4d2cs	Synchronous 4 byte deep fifo, independent read/write control
f16w4ds	Synchronous 16 bit wide, 4 byte deep fifo
f16w8d2cs	Synchronouse 8 byte deep fifo, independen read/write control
f16w8da	Asynchronous 16 bit wide, 8 byte deep fifo
f16w8ds	Synchronous 16 bit wide, 8 byte deep fifo
f18w3da	Asynchronous 18 bit wide, 3 byte deep fifo
f18w4d2cs	Synchronous 4 byte deep fifo, independent read/write control
f18w4ds	Synchronous 18 bit wide, 4 byte deep fifo
f18w8d2cs	Synchronous 8 byte deep fifo, independent read/write control
f18w8da	Asynchronous 18 bit wide, 8 byte deep fifo
f18w8ds	Synchronous 18 bit wide, 8 byte deep fifo
f32w3da	Asynchronous 32 bit wide, 3 byte deep fifo
f32w4d2cs	Synchronous 4 byte deep fifo, independent read/write control
f32w4ds	Synchronous 32 bit wide, 4 byte deep fifo
f32w8d2cs	Synchronous 8 byte deep fifo, independent read/write control
f32w8da	Asynchronous 32 bit wide, 8 byte deep fifo
f32w8ds	Synchronous 32 bit wide, 8 byte deep fifo
f36w3da	Asynchronous 36 bit wide, 3 byte deep fifo
f36w4d2cs	Synchronous 4 byte deep fifo, independent read/write control
f36w4ds	Synchronous 36 bit wide, 4 byte deep fifo
f36w8d2cs	Synchronous 8 byte deep fifo, independent read/write control
f36w8da	Asynchronous 36 bit wide, 8 byte deep fifo
f36w8ds	Synchronous 36 bit wide, 8 byte deep fifo
f8i16w4d2cs	Synchronous 4 byte deep fifo, independent read/write control
f8w3da	Asynchronous 8 bit wide, 3 byte deep fifo
f8w4d2cs	Synchronous 4 byte deep fifo, independent read/write control
f8w4ds	Synchronous 8 bit wide, 4 byte deep fifo
f8w8d2cs	Synchronous 8 byte deep fifo, independent read/write control
f8w8da	Asynchronous 8 bit wide, 8 byte deep fifo
f8w8ds	Synchronous 8 bit wide, 8 byte deep fifo
f9w3da	Asynchronous 9 bit wide, 3 byte deep fifo
f9w4d2cs	Synchronous 4 byte deep fifo, independent read/write control
f9w4ds	Synchronous 9 bit wide, 4 byte deep fifo
f9w8d2cs	Synchronous 8 byte deep fifo, independent read/write control

HDL Macros

Available in Verilog - HDL or VHDL Simulation Models

Function Group (Directory): fifo (continued)

Cell Name MSI Part Number	Cell Description
f9w8da	Asynchronous 9 bit wide, 8 byte deep fifo
f9w8ds	Synchronous 9 bit wide, 8 byte deep fifo
ltwd16	Two byte latch for asynchronous fifo's
ltwd18	Eighteen bit latch for asynchronous fifo's
ltwd32	Four byte latch for asynchronous fifo's
ltwd36	Thirty six bit latch for asynchronous fifo's
ltwd8	One byte latch for asynchronous fifo's
ltwd9	Nine bit latch for asynchronous fifo's
regwd16	Two byte register for synchronous fifo's
regwd18	Eighteen bit register for synchronous fifo's
regwd32	Four byte register for synchronous fifo's
regwd36	Thirty six bit register for synchronous fifo's
regwd8	One byte register for synchronous fifo's
regwd9	Nine bit register for synchronous fifo's
rw_ptr4	read/write control for 4 deep synchronous fifo
rw_ptr8	read/write control for 8 deep synchronous fifo
sf_ctl4	Control for 4 deep synchronous fifo w/independent read/write control
sf_ctl8	Control for 8 deep synchronous fifo w/indepependent read/write control

Function Group (Directory): inc_dec

Cell Name MSI Part Number	Cell Description
dec12	Twelve bit decrementer
dec12p	Twelve bit decrementer with parity prediction
dec13	Thirteen bit decrementer
dec13p	Thirteen bit decrementer with parity prediction
dec16	Sixteen bit decrementer
dec16p	Sixteen bit decrementer with parity prediction
dec24	Twenty four bit decrementer
dec24p	Twenty four bit decrementer with parity prediction
dec32	Thirty two bit decrementer
dec32p	Thirty two bit decrementer with parity prediction
dec4f	Four bit decrementer, for first stage
dec4fp	Four bit decrementer parity predictor, for 1st stage
dec4x	Four bit decrementer, extendable
dec4xp	Four bit decrementer parity predictor, for 2nd + stages

HDL Macros

Available in Verilog - HDL or VHDL Simulation Models

Function Group (Directory): inc_dec (continued)

Cell Name MSI Part Number	Cell Description
dec5f	Five bit decrementer, for first stage
dec5fp	Five bit decrementer parity predictor, for 1st stage
dec5x	Five bit decrementer, extendable
dec5xp	Five bit decrementer parity predictor, for 2nd + stages
dec8	Eight bit decrementer
dec8p	Eight bit decrementer with parity prediction
idec12	Twelve bit incrementer/decrementer
idec12p	Twelve bit incrementer/decrementer with parity prediction
idec13	Thirteen bit incrementer/decrementer
idec13p	Thirteen bit incrementer/decrementer with parity prediction
idec16	Sixteen bit incrementer/decrementer
idec16p	Sixteen bit incrementer/decrementer with parity prediction
idec24	Twenty four bit incrementer/decrementer
idec24p	Twenty four bit incrementer/decrementer with parity prediction
idec32	Thirty two bit incrementer/decrementer
idec32p	Thirty two bit incrementer/decrementer with parity prediction
idec4f	Four bit incrementer/decrementer for 1st stage
idec4fp	Four bit incrementer/decrementer parity predictor, 1st stage
idec4x	Four bit incrementer/decrementer, extendable
idec4xp	Four bit incrementer/decrementer parity predictor, 2nd + stages
idec5f	Five bit incrementer/decrementer, for 1st stage
idec5fp	Five bit incrementer/decrementer parity predictor, 1st stage
idec5x	Five bit incrementer/decrementer, extendable
idec5xp	Five bit incrementer/decrementer parity predictor, 2nd + stages
idec8	Eight bit incrementer/decrementer
idec8p	Eight bit incrementer/decrementer with parity prediction
inc12	Twelve bit incrementer
inc12p	Twelve bit incrementer with parity prediction
inc13	Thirteen bit incrementer
inc13p	Thirteen bit incrementer with parity prediction
inc16	Sixteen bit incrementer
inc16p	Sixteen bit incrementer with parity prediction
inc24	Twenty four bit incrementer
inc24p	Twenty four bit incrementer with parity prediction
inc32	Thirty two bit incrementer
inc32p	Thirty two bit incrementer with parity prediction
inc4f	Four bit incrementer, for first stage
inc4fp	Four bit incrementer parity predictor, for first stage

HDL Macros

Available in Verilog - HDL or VHDL Simulation Models

Function Group (Directory): inc_dec (continued)

Cell Name MSI Part Number	Cell Description
inc4x	Four bit incrementer, extendable
inc4xp	Four bit incrementer parity predictor, for 2nd + stages
inc5f	Five bit incrementer, for first stage
inc5fp	Five bit incrementer parity predictor, for first stage
inc5x	Five bit incrementer, extendable
inc5xp	Five bit incrementer parity predictor, for 2nd + stages
inc8	Eight bit incrementer
inc8p	Eight bit incrementer with parity prediction

Function Group (Directory): mux

Cell Name MSI Part Number	Cell Description
mx2X	4 bit wide, non-inverting 2 to 1 mux
mx3X	4 bit wide, non-inverting 3 to 1 mux
mx4X	4 bit wide, non-inverting 4 to 1 mux
mx5X	4 bit wide, non-inverting 5 to 1 mux
mx6X	4 bit wide, non-inverting 6 to 1 mux
mx7X	4 bit wide, non-inverting 7 to 1 mux
mx8X	4 bit wide, non-inverting 8 to 1 mux

HDL Macros

Available in Verilog - HDL or VHDL Simulation Models

Function Group (Directory): par_ecc

Cell Name MSI Part Number	Cell Description
ecc32cd	32 Bit ECC Corrector Decoder
ecc32cd	32 Bit ECC Corrector Decoder
ecc32cl	ECC Corrector for 32 Bit Data (latched inputs)
ecc32gl	ECC Generator for 32 Bit Data (latched inputs)
ep12gv	Even Parity Vector Generator for 12 bit Input
ep13gv	Even Parity Vector Generator for 13 bit Input
ep16gv	Even Parity Vector Generator for 16 bit Input
epar12chk	Even Parity Checker W/Test Input for 12 Bits
epar12gen	Even Parity Generator for 12 bit Input
epar13chk	Even Parity Checker W/Test Input for 13 Bits
epar13gen	Even Parity Generator for 13 bit Input
epar16gen	Even Parity Generator for 16 bit Input
eparXchk	Even Parity Checker W/Test In for Small Widths
eparXgen	Even Parity Generator for Small Data Widths
Opar16gen	Odd Parity Generator for 16 bit Input

Function Group (Directory): scan (JTAG-IEEE Std 1149.1-1990)

Cell Name MSI Part Number	Cell Description
bypass_reg	Bypass Register Cell
dr3soc	Data Register 3-State Output Cell
dr3socct	Data Register 3-State Output Cell w/full EXTEST & INTEST Support
dr3socoep	Data Register 3-State Output Cell with Output Enable from System Pin and Supporting INTEST Instruction
drbic	Data Register Input or Output Cell
dri_oc	Data Register Input or Output Cell
dric	Data Register Input Cell
dricf1	Data Register Input Cell Forcing a '1' during EXTEST
dricpo	Data Register Input Cell with Parallel Output Register
dricsco	Data Register Input Cell Allowing Signal Capture Only Used when Implementing Only the Mandatory Instructions
driocc	Data Register Bi-Directional Output Enable Cell
drmanbic	Data Register Cell at Bi-Directional Pin when only Mandatory Instructions are Implemented
drocnointest	Data Register Output Cell without INTEST Support
idreg	ID Register

Function Group (Directory): scan (JTAG-IEEE Std 1149.1-1990) (continued)

Cell Name MSI Part Number	Cell Description
idusreg	IDCODE and USERCODE Registers
instreg	Instruction Register for both Mandatory and Optional instructions. A RESET will load the IDCODE instruction
min_instreg	Instruction Register for Mandatory Instruction Only
tap_controller	Tap Controller Cell
tap_decode	Instruction Register Decoder for all Public Instruction
tap_mindecode	Instruction Register fDecoder or Mandatory Instructions Only
bscb	boundary Scan Cell for Bi-Directional pad
bscbX	boundary Scan Cells for Bi Directional pads
bscc	boundary Scan Control Cell
bsccV	boundary Scan Control Cell with vectored output
bsci	boundary Scan Cell for Input pin
bsciX	boundary Scan Cells for Input pins
bsco	boundary Scan Cell for Output pin
bscoX	boundary Scan Cells for Output pins
sdlregX	Scan register with data input and load control
sdregX	Scan register with data input
sregX	Scan register without data input

Function Group (Directory): shifter

Cell Name MSI Part Number	Cell Description
bshift16	16 bit barrel shifter - logical and arithmetic
bshift16a	16 bit arithmetic barrel shifter
bshift16l	16 bit logical barrel shifter
bshift32	32 bit barrel shifter - logical and arithmetic
bshift32a	32 bit arithmetic barrel shifter
bshift32l	32 bit logical barrel shifter
bshift8	8 bit barrel shifter - logical and arithmetic
bshift8a	8 bit arithmetic barrel shifter
bshift8l	8 bit logical barrel shifter

HDL Macros

Available in Verilog - HDL or VHDL Simulation Models

Function Group (Directory): multipliers

Cell Name MSI Part Number	Cell Description
m10x10p1	10 x 10 booth bit_pair recoded multiplier with one pipeline
m12x10p1	12 x 10 booth bit_pair recoded multiplier with one pipeline
m12x8p2	12 x 8 booth bit_pair recoded multiplier with two pipelines
m8x8p1	8 x 8 booth bit_pair recoded multiplier with one pipeline
m16x16p1	16 x 16 booth bit_pair recoded multiplier with one pipeline
m16x8p1	16 x 8 booth bit_pair recoded multiplier with one pipeline
m12x12p1	12 x 12 booth bit_pair recoded multiplier with one pipeline
m12x14	12 x 14 booth bit_pair recoded multiplier
m16x12p2	16 x 12 booth bit_pair recoded multiplier with two pipelines
m8x8p3	8 x 8 booth bit_pair recoded multiplier with three pipelines

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Section 9

CMOS Logic

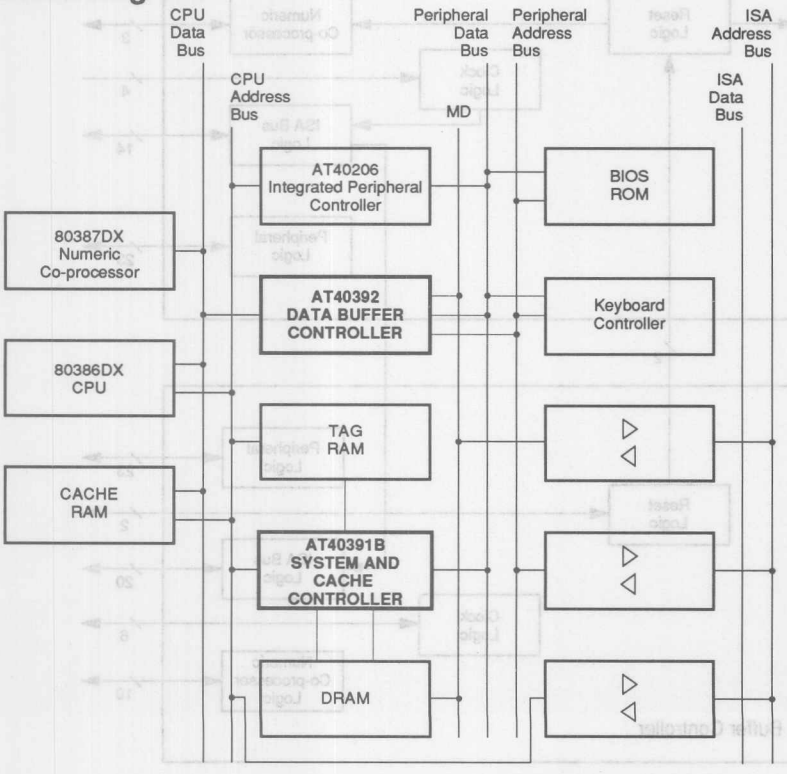
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Features

- Two-Chip PC/AT Compatible Chip Set for 80386DX Systems Operating up to 40 MHz
  - AT40391B System and Cache Controller
  - AT40392 Data Buffer Controller
- Two 160-Pin Quad Flatpacks
- On-Chip Support for Direct-Mapped Write-Back Cache
- 0 Wait State Cache Read Hit and Programmable 0/1 Wait State Cache Write Hit
- Two Programmable Non-Cacheable Regions
- On-Chip Tag Comparator
- Burst Line Fill During Cache Read Misses
- Page Mode Main Memory Operation with Programmable Wait States Supporting Platform Memory Sizes up to 64 Mbytes
- Support for 256K, 1-Mbit and 4-Mbit DRAMs
- Low Power CAS# Before RAS#, Transparent DRAM Refresh
- Low Power, Slow Refresh for Laptop PC Operation
- Parity Generation and Detection
- Support for Shadow RAM
- Cacheable Video BIOS Option
- 8042 Emulation for Fast CPU Reset and Gated A20 Generation
- ISA Bus Control with Programmable Clock
- 0 or 1 Wait State for 16-Bit ISA Bus Cycles
- Support for 80387DX and 3167 Numeric Co-processors

80386DX PC/AT Chip Set

Block Diagram



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Description

The Atmel AT40391B/AT40392 chip set is a 100% IBM PC/AT compatible chip set for 80386DX based systems operating up to 40 MHz. The high integration and an on-chip write-back, direct-mapped cache controller design allows maximum system performance. Together with a peripheral controller, such as the AT40206 integrated peripheral controller, a very high performance, yet low cost, 80386DX motherboard can be built with a minimum number of components.

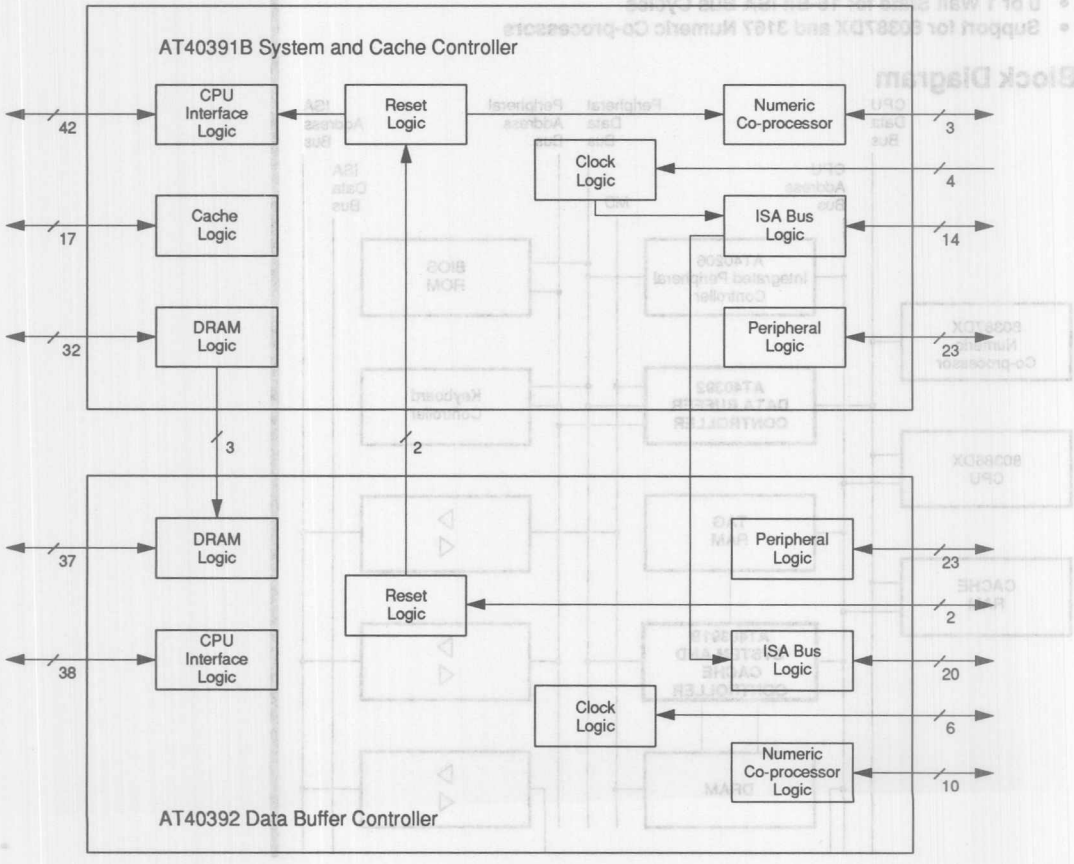
The AT40391B system controller performs the system control, memory and cache control functions. The system control logic consists of the following logic blocks: CPU control, AT bus cycle control, numeric co-processor control, synchronous clock circuitry and peripheral bus control. The memory and cache controller functions consist of a write-back, direct-mapped cache controller and a paged mode DRAM controller. The AT40391B supports cache sizes up to 256 Kbytes (16-byte line size), and platform memory sizes up to 64 Mbytes.

The AT40392 data buffer controller performs the data buffer and co-processor interface functions. The data buffer logic performs bus conversion logic for various 8-, 16- and 32-bit data movements as required among the system buses. The other functions of the AT40392 are co-processor interface, keyboard controller decoding, reset and generation of various peripheral clocks.

Low cost systems are made possible through the support of single ROM/EPROM BIOS configurations. The BIOS ROM/EPROM can be either 8-bit or 16-bit. DRAM is located on the system platform bus, thus reducing DRAM speed requirements by at least 15 ns.

The AT40391B/AT40392 PC/AT chip set is compatible with the AT40206 integrated peripheral controller and works with BIOS from AMI, Phoenix, Award and Quadtel.

Functional Block Diagram



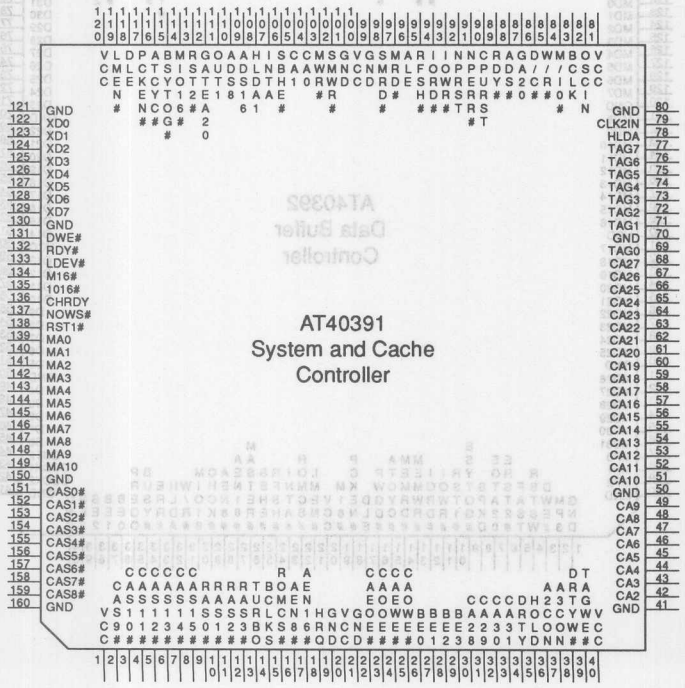
AT40391B System and Cache Controller

- Programmable clock generators for the platform and ISA buses
- CPU and numeric co-processor reset control
- Direct-mapped write-back cache controller
- 0 wait state cache read hit and programmable 0/1 wait state cache write hit
- Two programmable non-cacheable regions
- Cacheable video BIOS option
- On-chip tag RAM comparator
- Burst line fill during cache read misses
- Programmable page mode DRAM controller for 256K, 1-Mbit, and 4-Mbit DRAMs for platform memory sizes up to 64 Mbytes
- Decoupled system platform and ISA bus DRAM refresh
- Low power CAS# before RAS#, transparent DRAM refresh
- Slow refresh option
- Shadow RAM support
- Programmable 0/1 wait state for ISA bus cycles

The Atmel AT40391B is a highly integrated system and cache controller for 25 MHz, 33 MHz and 40 MHz 80386DX PC/AT systems. When combined with the AT40392 data buffer controller and the AT40206 integrated peripheral controller, a powerful but low cost PC/AT can be built with minimal components.

The AT40391B performs all the system control, memory control, cache control, and bus arbitration functions for an 80386DX PC/AT system including the reset and power shutdown functions and synchronous CPU and ISA bus clocks generation. The flexible memory controller supports system memory sizes up to 64 Mbytes with a wide range of DRAMs. The direct-mapped write-back cache controller implements a high performance cache system while requiring minimal external components. The functions of the AT40391B are programmed through twelve configuration registers.

Pin Configuration



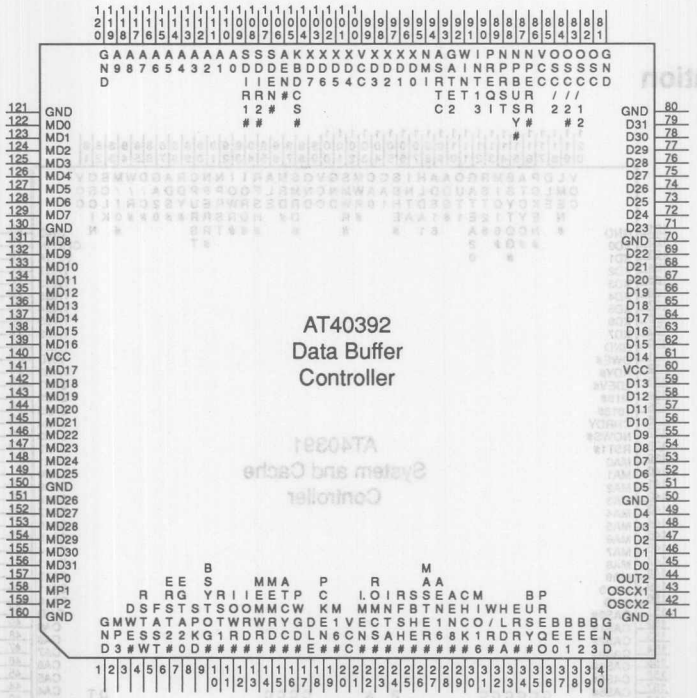
AT40392 Data Buffer Controller

- **Data bus conversions**
- **DRAM parity generation and detection**
- **ISA bus direction control**
- **Reset logic**
- **Peripheral clock generation**
- **Keyboard and real-time clock chip select**
- **Speaker control**
- **PortB, 70H and NMI logic**
- **Numeric co-processor interface**
- **Keyboard reset and Gate A20 emulation logic**

The Atmel AT40392 is a highly integrated data buffer controller for 25 MHz, 33 MHz and 40 MHz 80386DX based PC/AT systems. Together with the AT40391B system and cache controller and the AT40206 integrated peripheral controller, a low cost yet powerful PC/AT can be built with minimal components.

The AT40392 data buffer controller performs all of the data buffering control required in a 386DX PC/AT system. Under the control of the CPU and the AT40391B system and memory controller, the AT40392 routes data to and from the CPU bus, MD bus, XD bus and the ISA bus, while also providing any necessary data size conversions. The AT40392 also performs high byte to low byte and low byte to high byte swapping on the ISA bus. For platform DRAM accesses, the AT40392 performs parity error checking and generation.

Pin Configuration



Ordering Information

CPU Clock (MHz)	Power Supply	Ordering Code	Package	Operation Range
25	5 V ± 5%	AT40391B-25 AT40392-25	160Q 160Q	Commercial (0°C to 70°C)
33	5 V ± 5%	AT40391B-33 AT40392-33	160Q 160Q	Commercial (0°C to 70°C)
40	5 V ± 5%	AT40391B-40 AT40392-40	160Q 160Q	Commercial (0°C to 70°C)

Package Type	
160Q	160 Lead, Plastic Gull Wing Quad Flat Package (PQFP)

Ordering Information

CPU Clock (MHz)	Power Supply	Ordering Code	Package	Operation Range
25	5 V ± 5%	AT40319B-25 AT40392-25	160Q 160Q	Commercial (0°C to 70°C)
33	5 V ± 5%	AT40319B-33 AT40392-33	160Q 160Q	Commercial (0°C to 70°C)
40	5 V ± 5%	AT40319B-40 AT40392-40	160Q 160Q	Commercial (0°C to 70°C)

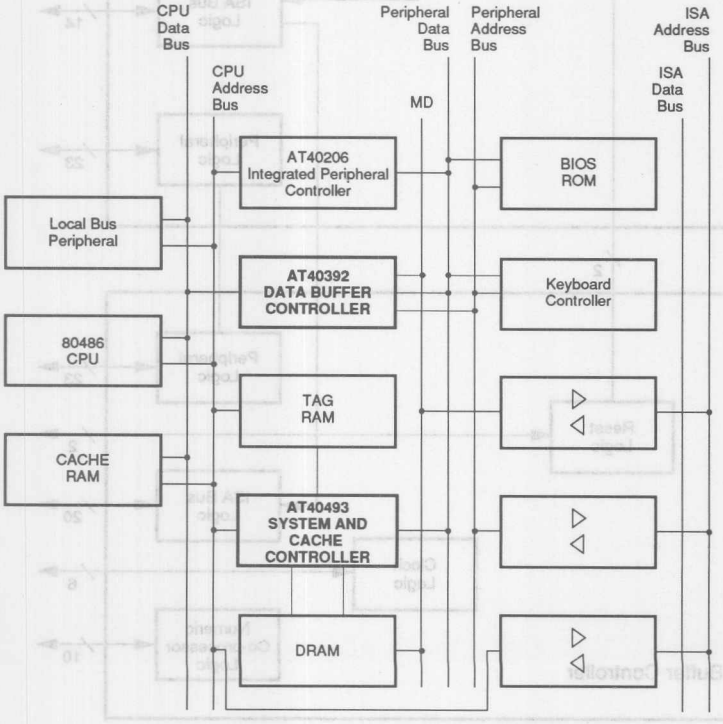
Package Type	
160Q	160 Lead, Plastic Gull Wing Quad Flat Package (PQFP)

Features

- Two-Chip PC/AT Compatible Chip Set for 80486 Based Systems Operating up to 50 MHz
  - AT40493 System and Cache Controller
  - AT40392 Data Buffer Controller
- Two 160-Pin Quad Flatpacks
- On-Chip Support for Direct-Mapped Write-Back Cache
- 0 Wait State Cache Read Hit and Programmable 0/1 Wait State Cache Write Hit
- Two Programmable Non-Cacheable Regions
- On-Chip Tag Comparator
- Burst Line Fill During Cache Read Misses
- Page Mode Main Memory Operation with Programmable Wait States Supporting Platform Memory Sizes up to 64 Mbytes
- Support for 256K, 1-Mbit and 4-Mbit DRAMs
- Low Power CAS# Before RAS#, Transparent DRAM Refresh
- Low Power, Slow Refresh for Laptop PC Operation
- Parity Generation and Detection
- Support for Shadow RAM
- Cacheable Video BIOS Option
- 8042 Emulation for Fast CPU Reset and Gated A20 Generation
- ISA Bus Control with Programmable Clock
- 0 or 1 Wait State for 16-Bit ISA Bus Cycles
- Support for Local Bus Peripherals
- Supports 2-1-1-1 and 3-2-2-2 Cache and DRAM Burst Cycles

80486 PC/AT Chip Set

Block Diagram



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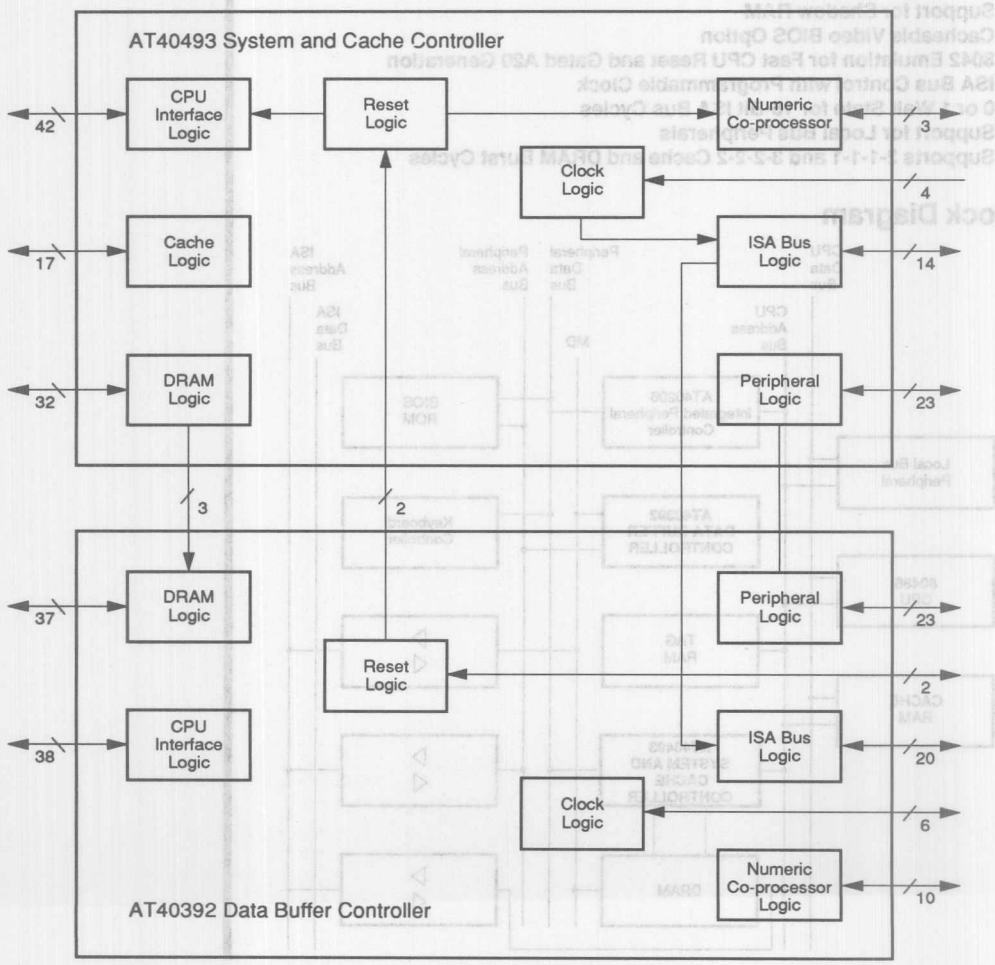
Description

The Atmel AT40493/AT40392 chip set is an IBM PC/AT compatible chip set for 80486 based systems operating up to 50 MHz. The high integration and an on-chip write-back, direct-mapped cache controller design allows maximum system performance. Together with a peripheral controller, such as the AT40206 integrated peripheral controller, a very high performance, yet low cost, 80486 motherboard can be built with a minimum number of components.

The AT40493 system controller performs the system control, memory and cache control functions. The system control logic consists of the following logic blocks: CPU control, AT bus cycle control, numeric co-processor control, synchronous clock circuitry and peripheral bus control. The memory and cache controller functions consist of a write-back, direct-mapped cache controller and a paged mode DRAM controller. The AT40493 supports cache sizes up to 512 Kbytes (16-byte line size), platform memory sizes up to 64 Mbytes and burst mode for all system configurations.

The AT40392 data buffer controller performs the data buffer and co-processor interface functions. The data buffer logic performs bus conversion logic for various 8-, 16- and 32-bit data movements as required among the system buses. The other functions of the AT40392 are co-processor interface, keyboard controller decoding, reset and generation of various peripheral clocks.

Low cost systems are made possible through the support of single ROM/EPROM BIOS configurations. The BIOS ROM/EPROM can be either 8-bit or 16-bit. DRAM is located on the system platform bus, thus reducing DRAM speed requirements by at least 15 ns.



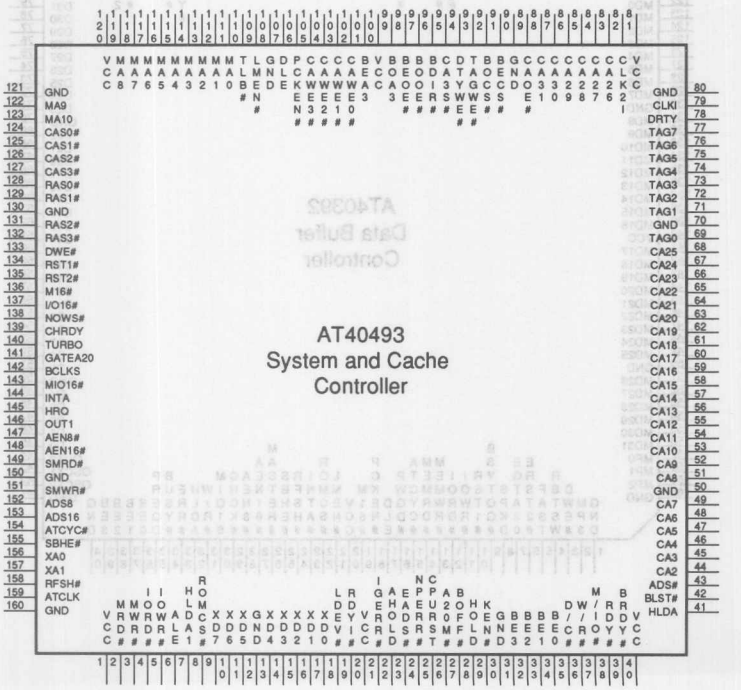
Atmel AT40493 System and Cache Controller

- Programmable ISA bus clock generator
- CPU and numeric co-processor reset control
- Direct-mapped write-back cache controller
- 0 wait state cache read hit and programmable 0/1 wait state cache write hit
- Two programmable non-cacheable regions
- Cacheable video BIOS option
- On-chip tag RAM comparator
- Burst line fill during cache read misses
- Programmable page mode DRAM controller for 256K, 1-Mbit, and 4-Mbit DRAMs for platform memory sizes up to 64 Mbytes
- Decoupled system platform and ISA bus DRAM refresh
- Low power CAS# before RAS#, transparent DRAM refresh
- Slow refresh option
- Shadow RAM support
- Programmable 0/1 wait state for ISA bus cycles
- Supports 2-1-1-1 and 3-2-2-2 cache and DRAM burst cycles

The Atmel AT40493 is a highly integrated system and cache controller for 16 MHz, 20 MHz, 25 MHz, 33 MHz and 50 MHz 80486 PC/AT systems. When combined with the AT40392 data buffer controller and the AT40206 integrated peripheral controller, a powerful but low cost PC/AT can be built with minimal components.

The AT40493 performs all the system control, memory control, cache control, and bus arbitration functions for an 80486 PC/AT system including the reset and power shutdown functions and synchronous CPU and ISA bus clocks generation. The flexible memory controller supports system memory sizes up to 64 Mbytes with a wide range of DRAMs. The direct-mapped write-back cache controller implements a high performance cache system while requiring minimal external components. The functions of the AT40493 are programmed through twelve configuration registers.

Pin Configuration



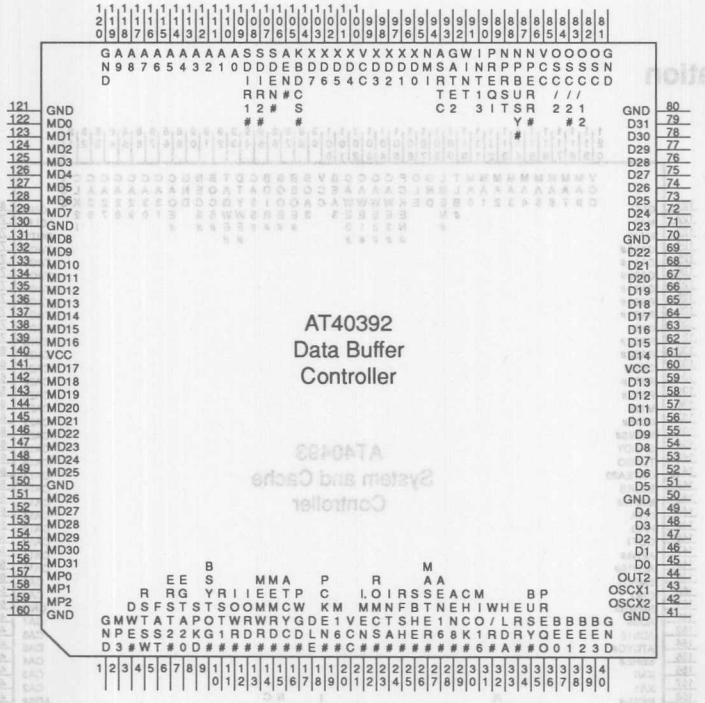
AT40392 Data Buffer Controller

- **Data bus conversions**
- **DRAM parity generation and detection**
- **ISA bus direction control**
- **Reset logic**
- **Peripheral clock generation**
- **Keyboard and real-time clock chip select**
- **Speaker control**
- **PortB, 70H and NMI logic**
- **Numeric co-processor interface**
- **Keyboard reset and Gate A20 emulation logic**

The Atmel AT40392 is a highly integrated data buffer controller for 16 MHz, 20 MHz, 25 MHz, 33 MHz and 50 MHz 80486 based PC/AT systems. Together with the AT40493 system and cache controller and the AT40206 integrated peripheral controller, a low cost yet powerful PC/AT can be built with minimal components.

The AT40392 data buffer controller performs all of the data buffering control required in a 486 PC/AT system. Under the control of the CPU and the AT40493 system and memory controller, the AT40392 routes data to and from the CPU bus, MD bus, XD bus and the ISA bus, while also providing any necessary data size conversions. The AT40392 also performs high byte to low byte and low byte to high byte swapping on the ISA bus. For platform DRAM accesses, the AT40392 performs parity error checking and generation.

Pin Configuration



Ordering Information

CPU Clock (MHz)	Power Supply	Ordering Code	Package	Operation Range
25	5 V ± 5%	AT40493-25 AT40392-25	160Q 160Q	Commercial (0°C to 70°C)
33	5 V ± 5%	AT40493-33 AT40392-33	160Q 160Q	Commercial (0°C to 70°C)
50	5 V ± 5%	AT40493-50 AT40392-50	160Q 160Q	Commercial (0°C to 70°C)

Package Type	
160Q	160 Lead, Plastic Gull Wing Quad Flat Package (PQFP)

Ordering Information

CPU Clock (MHz)	Power Supply	Ordering Code	Package	Operation Range
25	5 V ± 5%	AT40493-25 AT40393-25	160Q 160Q	Commercial (0°C to 70°C)
33	5 V ± 5%	AT40493-33 AT40393-33	160Q 160Q	Commercial (0°C to 70°C)
50	5 V ± 5%	AT40493-50 AT40393-50	160Q 160Q	Commercial (0°C to 70°C)

Package Type	
160Q	160 Lead, Plastic Gull Wing Quad Flat Package (PQFP)

AT40495
Addendum to AT40493

80486
PC/AT
Chip Set

The AT40495 system and cache controller functions exactly like the AT40493 (see AT40493 data sheet) with the following exceptions:

- The AT40495 supports one or two banks of cache SRAM and does not require the use of buffers in the data path. Thus the even and odd bank output enables (BEOE# and BOOE#, respectively) are not asserted during CPU or DMA write cycles.
- The TLB# (pin 110) signal on the AT40493 is redefined as BEA2# (cache even bank address bit 2).
- The AT40495 supports 2-1-1-1 cache burst mode for 16 MHz, 20 MHz and 25 MHz operation and 3-2-2-2- cache burst mode for 33 MHz and 50 MHz operation.

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Ordering Information

CPU Clock (MHz)	Power Supply	Ordering Code	Package	Operation Range
25	5V ± 5%	AT40495-25 AT40392-25	160Q 160Q	Commercial (0°C to 70°C)
33	5V ± 5%	AT40495-33 AT40392-33	160Q 160Q	Commercial (0°C to 70°C)
50	5V ± 5%	AT40495-50 AT40392-50	160Q 160Q	Commercial (0°C to 70°C)

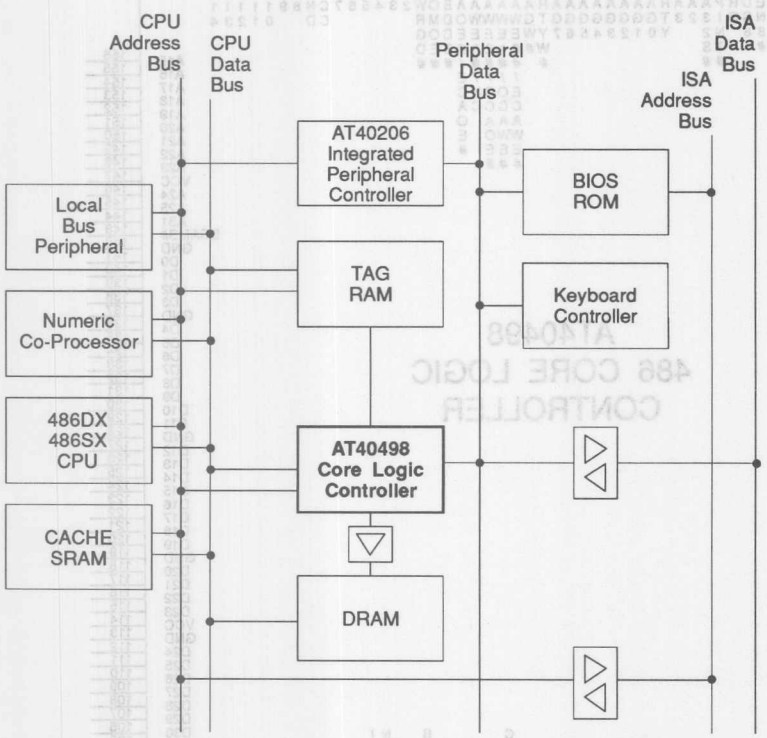
Package Type	
160Q	160 Lead, Plastic Gull Wing Quad Flat Package (PQFP)

Features

- One-Chip PC/AT Compatible Core Logic Controller for 80486 Systems Operating Up to 66 MHz.
- One 208-Pin Quad Flatpack, Sub-Micron CMOS Technology
- Direct Mapped Write-Back Cache Controller with Burst Fill
- Programmable 2-1-1-1, 3-1-1-1, 2-2-2-2 and 3-2-2-2 Cache Burst Cycles
- Local Bus Peripheral Support
- Port B Register and NMI Logic
- Programmable ISA Bus Clock Generator
- Back-to-Back 16-Bit ISA Bus Cycles
- 256K, 1-Mbit and 4-Mbit DRAM Support
- Up to 64 Mbytes of Platform Memory
- Shadow RAM Support
- OS/2 Alternate Hot Reset Support

80486 Core Logic Controller

Block Diagram



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Description

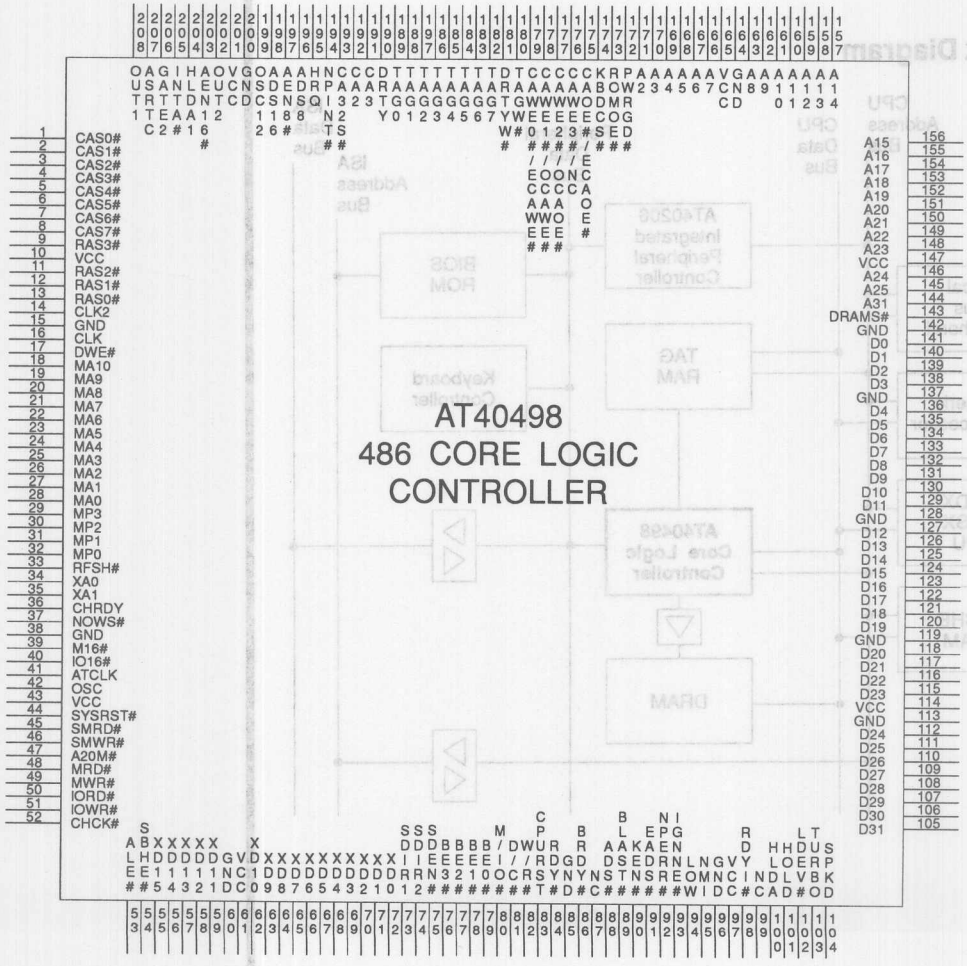
The Atmel AT40498 is a highly integrated single-chip core logic controller for 80486 PC/AT systems operating up to 66 MHz. The chip integrates system control, memory control, secondary cache control, bus arbitration functions, and data buffering and translation. In addition, the AT40498 supports local bus peripherals.

The memory controller addresses up to 64 Mbytes of main memory. The memory can consist of 256K, 1-Mbit, and 4-Mbit DRAMS. Refresh can be conventional or hidden, fast or slow.

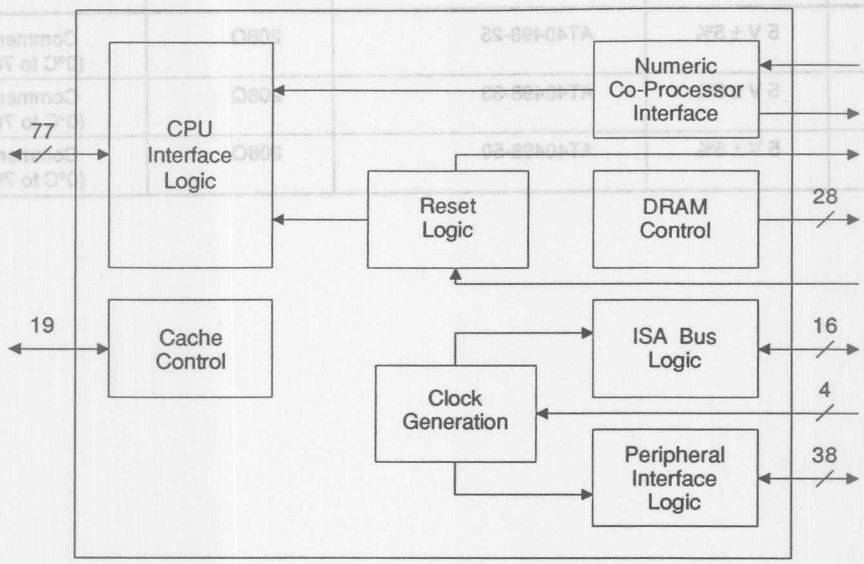
The secondary write-back cache controller supports one-bank or two-bank operation with interleaving to maximize performance. Cache sizes can range from 32 Kbytes to 512 Kbytes. Cache read and write burst cycles are programmable.

Together with a standard peripheral controller such as the AT40206 IPC and a minimum number of other components, the AT40498 implements a powerful, low-cost PC/AT compatible computer.

Pin Configuration

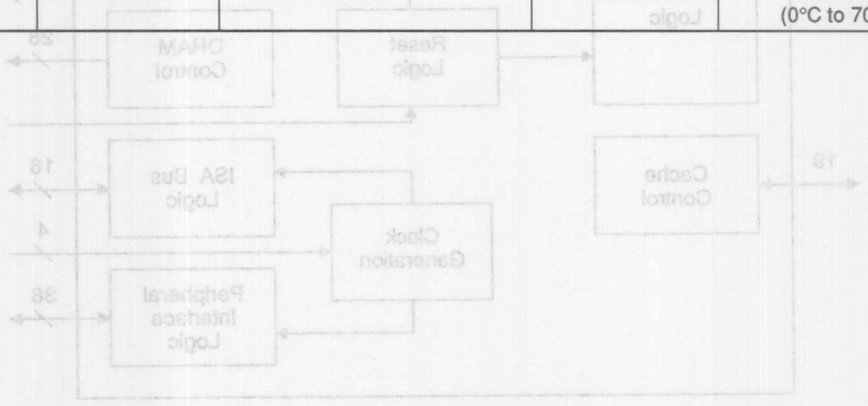


Core Logic Controller Block Diagram



Ordering Information

CPU Clock (MHz)	Power Supply	Ordering Code	Package	Operation Range
25	5 V ± 5%	AT40498-25	208Q	Commercial (0°C to 70°C)
33	5 V ± 5%	AT40498-33	208Q	Commercial (0°C to 70°C)
50	5 V ± 5%	AT40498-50	208Q	Commercial (0°C to 70°C)



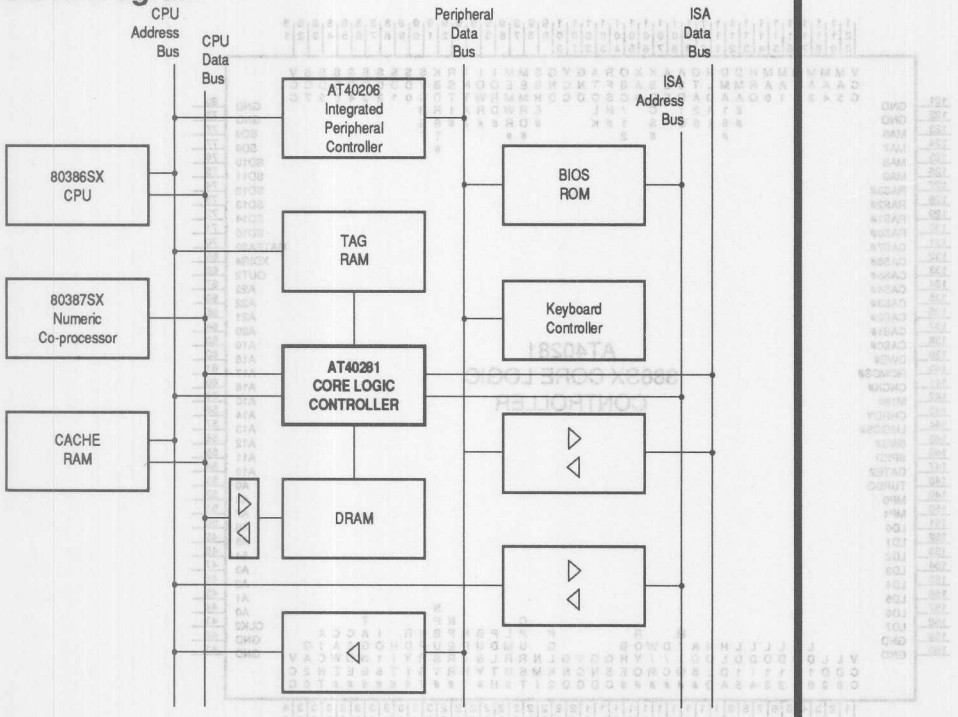
Package Type	
208Q	208 Lead, Plastic Gull Wing Quad Flat Package (PQFP)

Features

- One-Chip PC/AT Compatible Core Logic Controller for 80386SX Systems operating up to 33 MHz
- One 160-Pin Quad Flatpack, 1-Micron CMOS Technology
- CPU Interface and ISA Bus Control
- Direct Mapped Posted Write Cache Controller with Burst Cache Fill
- Numeric Co-processor Support
- OS/2 Alternate Hot Reset Support
- Programmable Clock Generator for the ISA Bus
- Port B Register and NMI Logic
- 256K, 1-Mbit and 4-Mbit DRAM Support
- Up to 16 Mbytes Platform Memory
- Shadow RAM Support
- Multiple Interleave Paging (MIP™) of Platform Memory

386SX Core Logic Controller

Block Diagram



Description

The Atmel AT40281 is a highly integrated single-chip core logic controller for 80386SX PC/AT systems operating up to 33 MHz. The chip integrates system control functions including reset logic and generation of the system clocks (CPU clock, ISA bus clock and the 1.19 MHz clock for the timer input), the local bus and ISA bus controllers, the memory controller and a direct mapped posted write cache controller.

The AT40281 decodes the CPU and ISA bus states to arbitrate among the various bus masters in the system. Data bus conversion, bus steering functions and data buffers and latches are all integrated on chip.

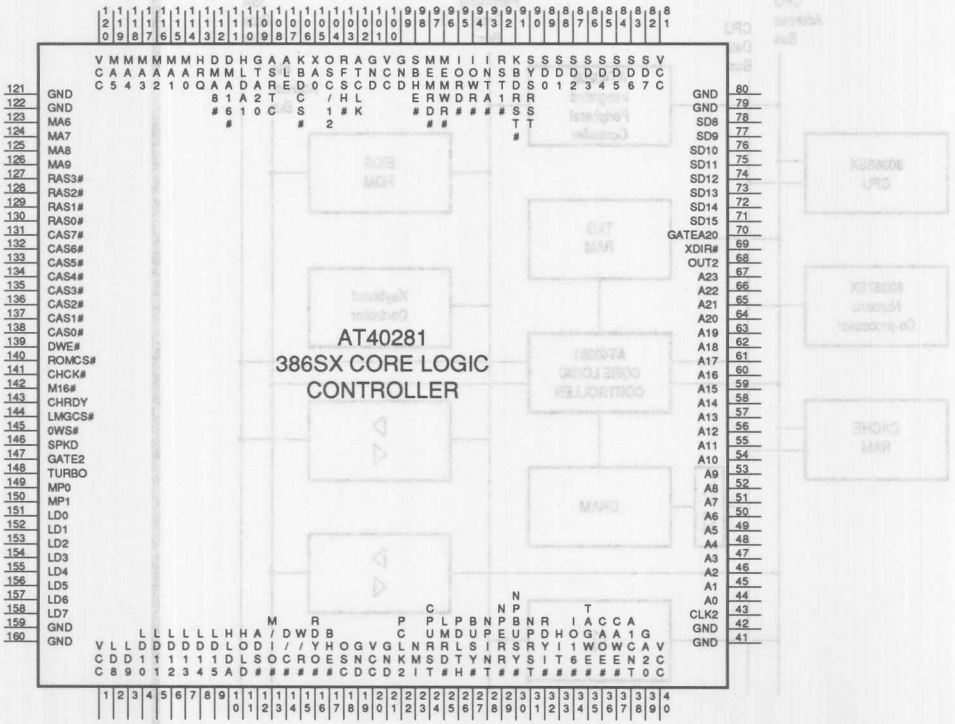
A variety of memory configurations and types of DRAMs can be used with the AT40281. Platform memory parity checking and generation are supported along with shadow RAM for BIOS, single ROM/EPROM for BIOS and address remapping of the unused memory between 640K and 1 Mbit to the top of memory.

The AT40281 also incorporates Multiple Interleaved Paging (MIP) of the platform memory which improves performance in both cache and cacheless configurations by minimizing the number of wait states required during DRAM accesses.

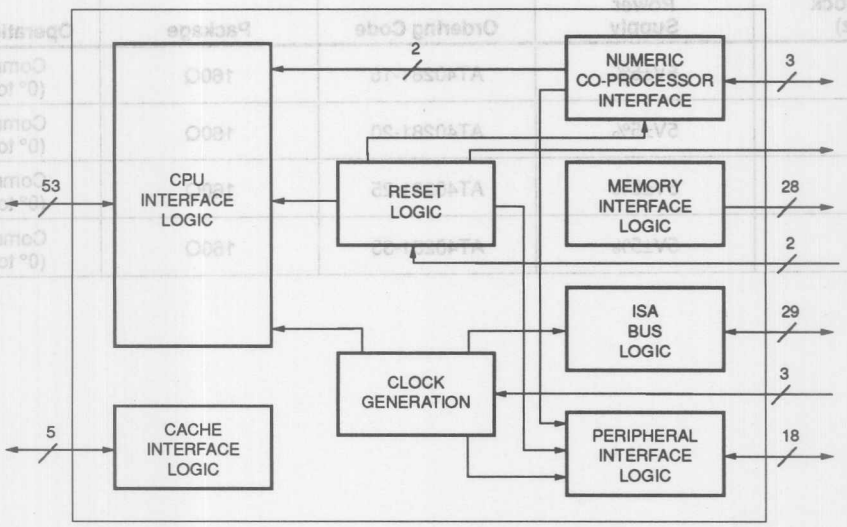
The programmable functions of the AT40281 are programmed through seven Configuration Registers.

Together with a standard peripheral controller such as the AT40206 IPC and a minimum number of other components, the AT40281 allows the use of a single board design for both cache and cacheless high performance, yet low cost, 80386SX PC/AT systems.

Pin Configuration



Core Logic Controller Block Diagram



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Ordering Information

CPU Clock (MHz)	Power Supply	Ordering Code	Package	Operation Range
16	5V±5%	AT40281-16	160Q	Commercial (0° to 70°C)
20	5V±5%	AT40281-20	160Q	Commercial (0° to 70°C)
25	5V±5%	AT40281-25	160Q	Commercial (0° to 70°C)
33	5V±5%	AT40281-33	160Q	Commercial (0° to 70°C)

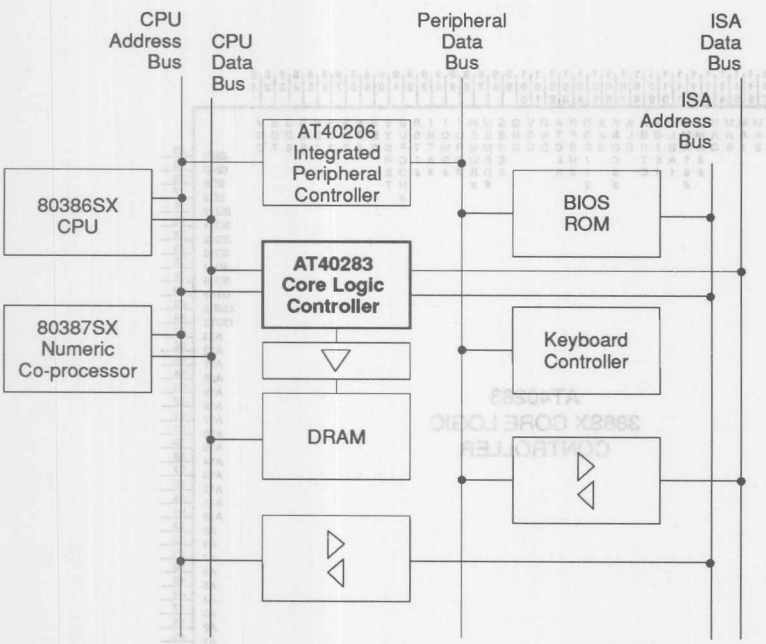
Package Type	
160Q	160 Lead, Plastic Gull Wing Quad Flat Package (Flatpack)

Features

- One-Chip PC/AT Compatible Core Logic Controller for 80386SX Systems operating up to 33 MHz
- One 160-Pin Quad Flatpack, 1-Micron CMOS Technology
- CPU Interface and ISA Bus Control
- Numeric Co-processor Support
- OS/2 Alternate Hot Reset Support
- Programmable Clock Generator for the ISA Bus
- Port B Register and NMI Logic
- 256K, 1-Mbit and 4-Mbit DRAM Support
- Up to 16 Mbytes Platform Memory
- Shadow RAM Support
- Multiple Interleave Paging (MIP™) of Platform Memory

386SX Core Logic Controller

System Block Diagram



Description

The Atmel AT40283 is a highly integrated single-chip core logic controller for 80386SX PC/AT systems operating up to 33MHz. The chip integrates system control functions including reset logic and generation of the system clocks (CPU clock, ISA bus clock and the 1.19 MHz clock for the timer input), the local bus and ISA bus controllers and the memory controller. The AT40283 decodes the CPU and ISA bus states to arbitrate among the various bus masters in the system. Data bus conversion, bus steering functions and data buffers and latches are all integrated on chip.

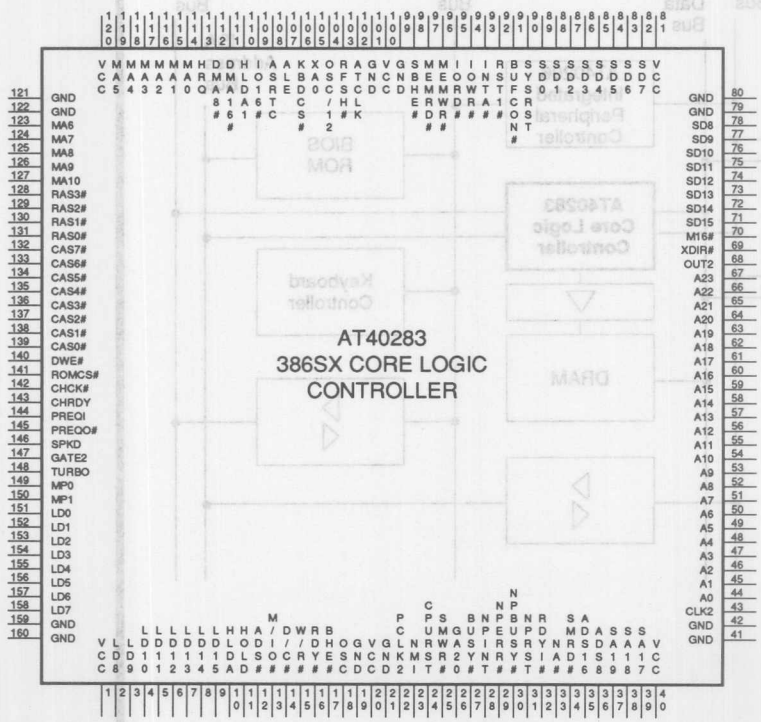
A variety of memory configurations and types of DRAMs can be used with the AT40283. Platform memory parity checking and generation are supported along with shadow RAM for BIOS, single ROM/EPROM for BIOS and address remapping of the unused memory between 640K and 1 Mbit to the top of memory.

The AT40283 also incorporates Multiple Interleaved Paging (MIP) of the platform memory which improves performance by minimizing the number of wait states required during DRAM accesses.

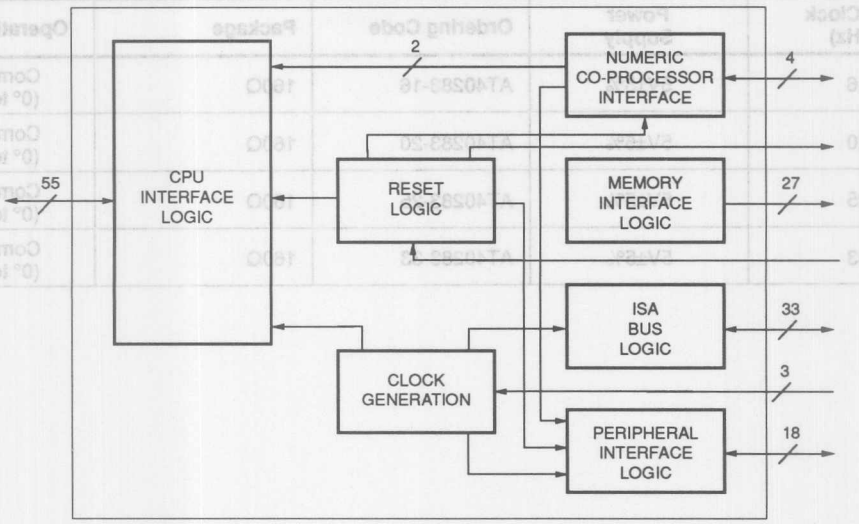
The programmable functions of the AT40283 are programmed through five Configuration Registers.

Together with a standard peripheral controller such as the AT40206 IPC and a minimum number of other components, the AT40283 implements a high performance, yet low cost, 80386SX PC/AT system.

Pin Configuration



Core Logic Controller Block Diagram



Ordering Information

CPU Clock (MHz)	Power Supply	Ordering Code	Package	Operation Range
16	5V±5%	AT40283-16	160Q	Commercial (0° to 70°C)
20	5V±5%	AT40283-20	160Q	Commercial (0° to 70°C)
25	5V±5%	AT40283-25	160Q	Commercial (0° to 70°C)
33	5V±5%	AT40283-33	160Q	Commercial (0° to 70°C)

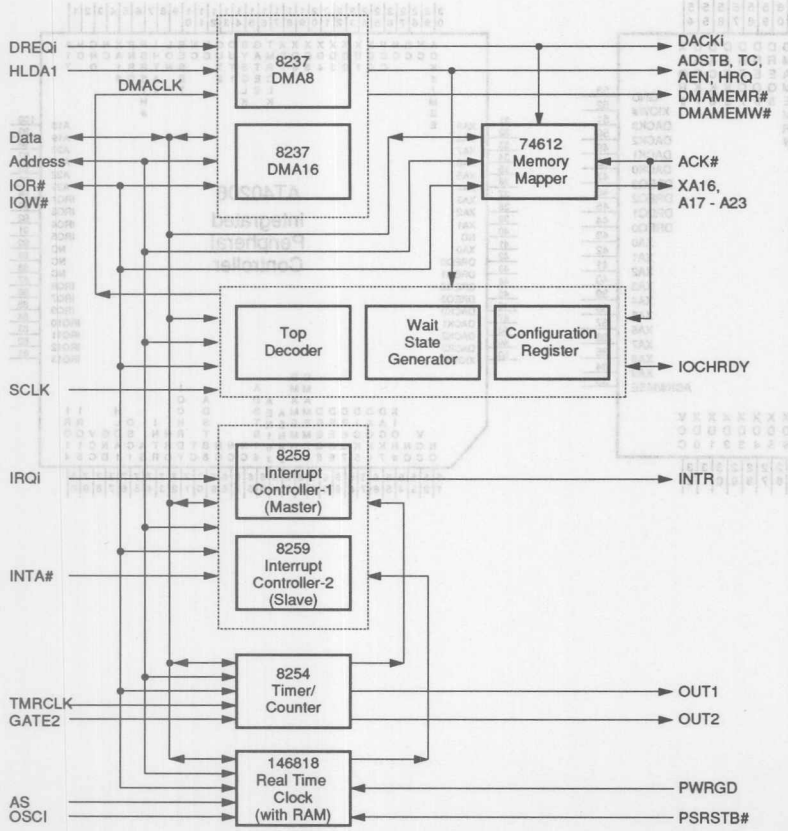
Package Type	
160Q	160 Lead, Plastic Gull Wing Quad Flat Package (Flatpack)

Features

- Fully Compatible with PC/AT Architecture
- Fully Compatible with 8237 DMA Controller, 8259 Interrupt Controller, 8254 Timer/Counter, and 146818 Real-Time Clock
- Provides 7 DMA Channels, 13 Interrupt Request Channels, 2 Timer/Counter Channels, and a Real-Time Clock
- Built-in 74LS612 Memory Mapper for DMA Page Address
- Provides 114 Bytes of CMOS RAM Memory
- 8-MHz DMA Clock with Programmable Internal Divider for 4-MHz Operation
- 16-Mbyte DMA Address Space
- Programmable Wait States for the DMA Cycle
- Reduced Recovery Time (120 ns) Between I/O Operations

PC/AT Integrated Peripheral Controller

System Block Diagram



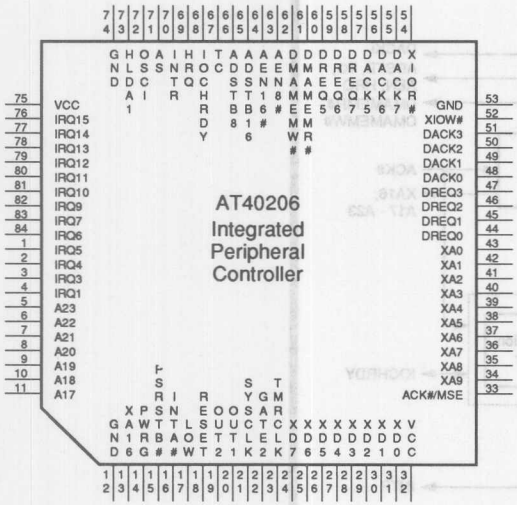
Description

The Atmel AT40206 integrated peripheral controller is a single chip integration of all the main peripherals attached to the XD bus of the PC/AT architecture including two 8237 DMA controllers, two 8259 interrupt controllers, one 8254 timer/counter, one MC146818 compatible real-time clock, an additional 64 bytes of CMOS RAM, one 74LS612 memory mapper, and some top-level decoder/configuration logic circuits.

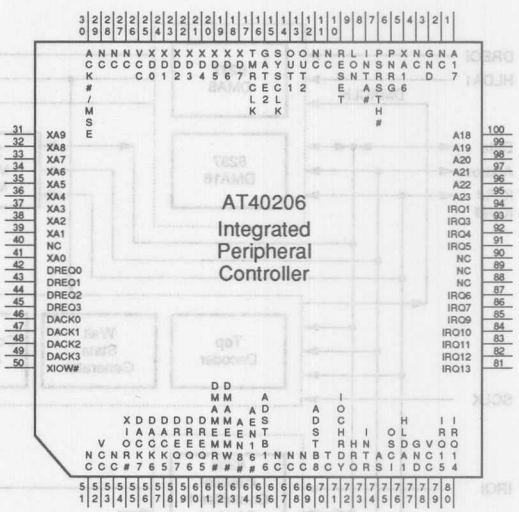
While providing full PC/AT architecture compatibility, the AT40206 also offers enhanced features and improved speed performance. These enhancements include an additional 64 bytes of user definable CMOS RAM and drastically reduced recovery time for the 8237, 8259 and 8254. A programmable wait state option is provided for use by the CPU, DMA or other bus masters when accessing this chip. The AT40206 also provides programmable 8-MHz or 4-MHz DMA clock selection. The AT40206 is implemented using advanced 1.5 micron CMOS technology and is packaged in either a 84-pin PLCC or a 100-pin PQFP.

Pin Configurations

84-Pin PLCC



100-Pin PQFP



Ordering Information

CPU Clock (MHz)	Power Supply	Ordering Code	Package	Operation Range
8	5V±5%	AT40206-8JC AT40206-8QC	84J 100Q2	Commercial (0° to 70°C)

Package Type	
84J	84 Lead, Plastic J-Leaded Chip Carrier (PLCC)
100Q2	100 Lead, Plastic Gull Wing Quad Flat Package, EIAJ (PQFP)

CPU Clock (MHz)	Power Supply	Ordering Code	Package	Operation Range
8	5V±5%	ATA0209-8JC ATA0209-8QC	84J 100Q2	Commercial (0° to 70°C)

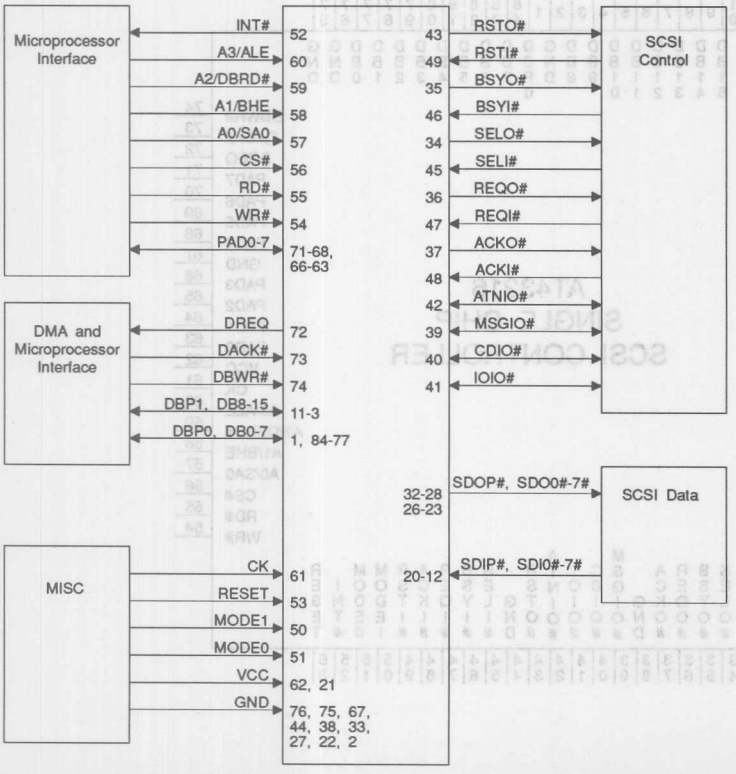
Package Type	
84J	84 Lead, Plastic J-Leaded Chip Carrier (PLCC)
100Q2	100 Lead, Plastic Gull Wing Quad Flat Package, EIAJ (PQFP)

Features

- One-Chip SCSI-2 Fast Architecture Controller for Host and 8-bit or 16-bit Peripheral Applications
- 84-Pin PLCC Package, Sub-Micron CMOS Technology
- Supports ANSI X3T9.2 SCSI Standard, with SCSI-2 Fast Architecture
- Functions as an Initiator or a Target
- Implements SCSI Bus Sequences without Host Processor Intervention
- Asynchronous Data Transfers up to 7 Mbytes/sec
- Synchronous Data Transfers up to 10 Mbytes/sec
- DMA Burst Transfers up to 20 Mbytes/sec
- Programmable Synchronous Transfer Period and Offset
- 24-Bit Transfer Counter
- Pipeline Command Structure
- 16-Byte, Parity Pass-through Data FIFO Between the DMA and SCSI Channels
- On-Chip 48-mA Single-Ended SCSI Transceivers

Single Chip SCSI Controller

System Block Diagram



9

Description

The AT43216 is a high performance single-chip SCSI-2 compatible controller that typically replaces SCSI interface circuitry consisting of discrete devices, external drivers, and a low performance SCSI interface chip.

The chip incorporates both initiator and target modes and can be used in host and peripheral applications. Bus arbitration, target selection, and initiator reselection are all handled on chip.

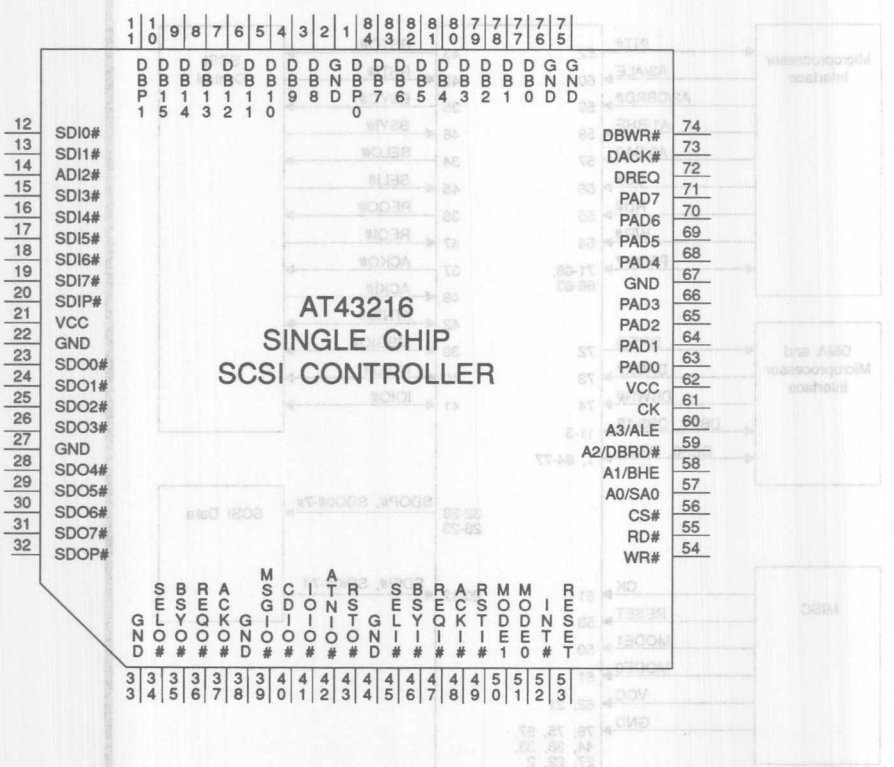
Overhead interaction with the host processor is minimized by use of an interrupt-driven architecture in conjunction with a command pipeline and a powerful instruction set that reduces common SCSI bus sequences to single commands. The chip controls message, command, status, and data transfers between the SCSI bus and the internal 16-byte FIFO.

In order to maximize throughput, the AT43216 architecture incorporates three independent buses: the 8-bit SCSI bus, the 8-bit or 16-bit with parity pass-through data bus (DB), and the 8-bit processor bus (PAD). The SCSI bus supports synchronous transfers of 5 Mbytes per second and 10 Mbytes per second in addition to asynchronous transfers up to 7 Mbytes per second. The data bus includes a high-speed DMA interface for burst transfer rates up to 20 Mbytes per second. The processor bus can be configured for multiplexed or non-multiplexed operation to simplify interfacing to the host processor.

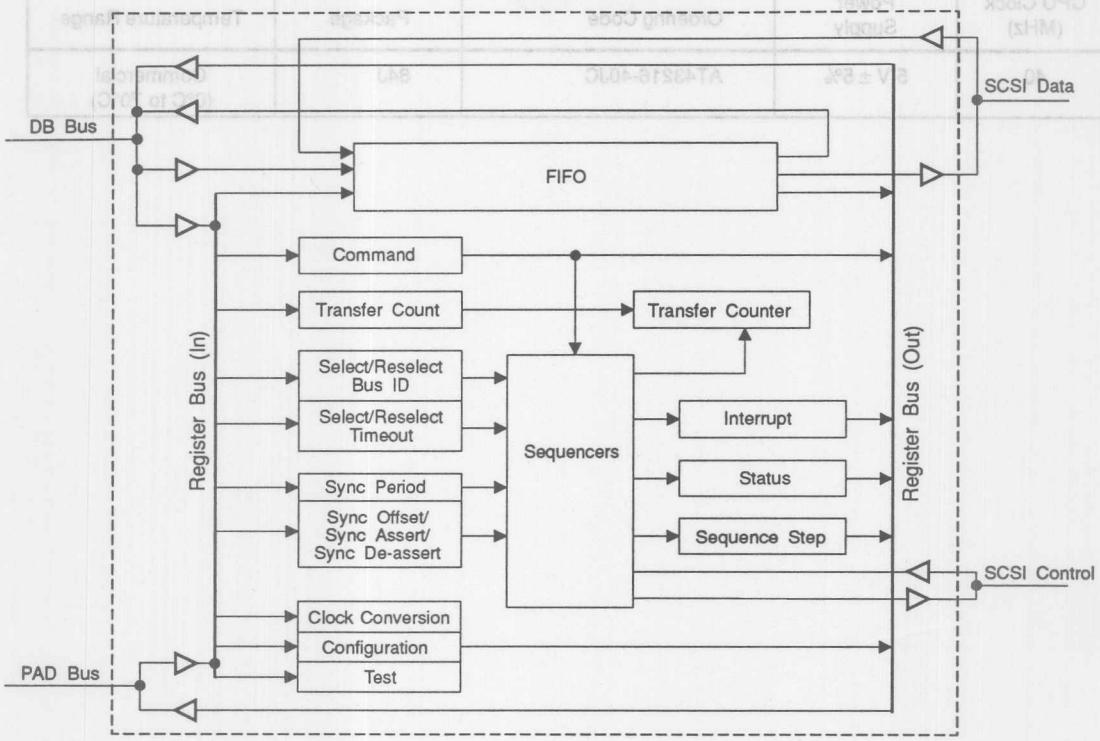
The AT43216 is designed for singled-ended operations with separate SCSI data input and output buses including on-chip 48-mA bus drivers.

Pin Configuration

84-PIN PLCC

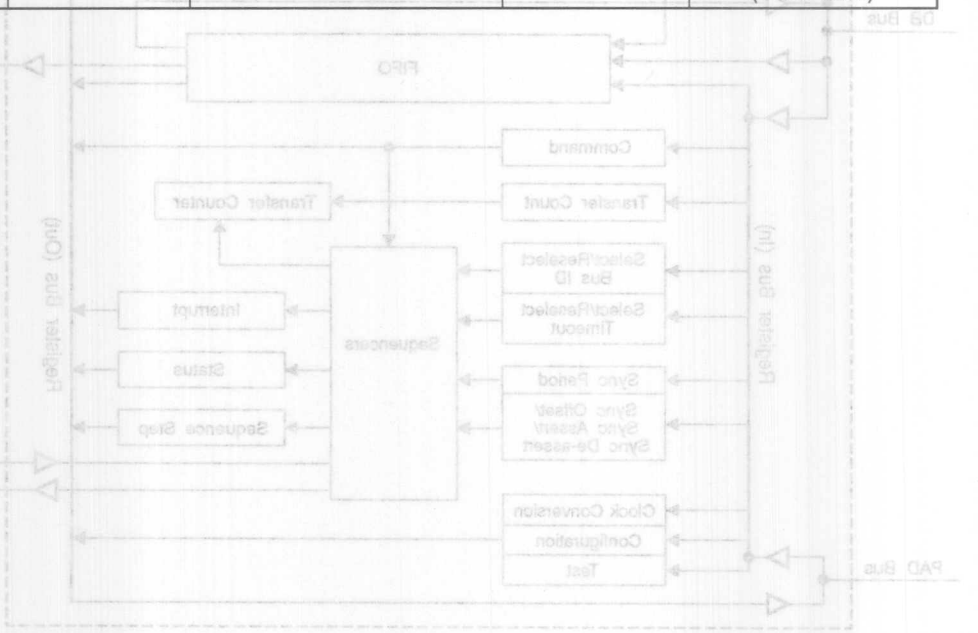


SCSI Controller Block Diagram



Ordering Information

CPU Clock (MHz)	Power Supply	Ordering Code	Package	Temperature Range
40	5 V ± 5%	AT43216-40JC	84J	Commercial (0°C to 70°C)



Package Type	
84J	84 Lead, J-Leaded Chip Carrier (PLCC)

Features

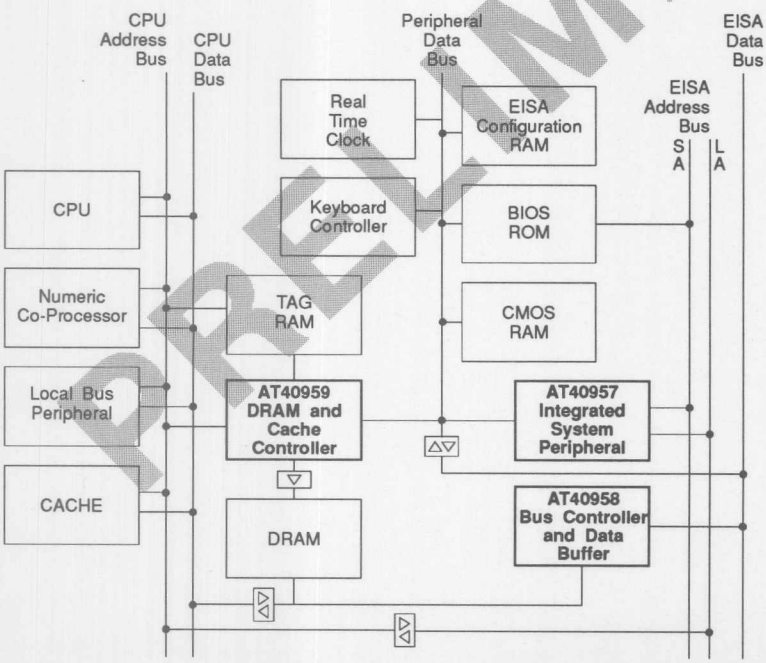
- Three-Chip EISA/ISA Compatible Chip Set for 80386/80486 Systems Operating up to 66 MHz
- One 160-Pin and Two 184-Pin Quad Flatpacks
  - AT40957 Integrated System Peripheral
  - AT40958 Bus Controller and Data Buffer
  - AT40959 DRAM and Cache Controller
- On-Chip Support for Direct-Mapped Write-Back Cache Sizes up to 1 Mbyte
- Asynchronous or Synchronous Cache SRAM
- On-Chip Tag Comparator
- Page Mode Platform Memory Sizes up to 256 Mbytes
- Posted Write Buffer for Write Miss Cycles
- BIOS Shadow and Cache Option
- Staggered Refresh to Reduce Power System Noise
- Hidden Refresh
- Eight ISA DMA Channels
- Six EISA Master Channels
- Fourteen Interrupt Channels
- Local Bus Peripheral Support

EISA/ISA PC/AT Chip Set

Preliminary

PRELIMINARY

Block Diagram



Description

The AT40957/AT40958/AT40959 chip set is an IBM PC/AT EISA/ISA compatible chip set for 80386 and 80486 based systems operating up to 66 MHz. The high integration and on-chip direct-mapped write-back cache controller design allows maximum system performance while requiring a minimum number of components to implement a complete motherboard.

The AT40957 integrated system peripheral incorporates the DMA controller, bus arbitrator, interrupt controller, numeric coprocessor interface, and EISA address latches and buffers. The DMA controller supports Type A, B, and C burst transfers at data rates up to 33 Mbytes/second and byte and word transfers for seven EISA DMA channels. The interrupt controller provides two 8259A-compatible interrupt controllers with 14 independently programmable channels for level- or edge-triggered interrupts. NMI logic includes a fail-safe timer.

The AT40958 bus controller and data buffer interfaces data to the CPU, DMA, master, and slave devices. Byte swaps, bus conversions, and data alignments are all done automatically. The AT40958 also includes parity generation and checking logic, as well as timers for watchdog, refresh, and speaker control.

The AT40959 DRAM and cache controller incorporates system reset logic, cache control, paged mode DRAM control, and BIOS interface logic. The cache controller is direct-mapped write-back with a 16-byte line and a maximum size of 1 Mbyte. An on-chip posted write buffer for write misses is included. The page mode DRAM controller generates and checks memory parity and supports up to eight banks of memory for memory sizes up to 128 Mbytes using 4-Mbit DRAMs, and 256 Mbytes using 16-Mbit DRAMs. The AT40959 also supports two non-cacheable areas in main memory and includes BIOS shadow and cache capabilities.

Ordering Information

CPU Clock (MHz)	Power Supply	Ordering Code	Package	Operation Range
33	5 V ± 5%	AT40957-33 AT40958-33 AT40959-33	184Q 184Q 160Q	Commercial (0°C to 70°C)
50	5 V ± 5%	AT40957-50 AT40958-50 AT40959-50	184Q 184Q 160Q	Commercial (0°C to 70°C)
66	5 V ± 5%	AT40957-66 AT40958-66 AT40959-66	184Q 184Q 160Q	Commercial (0°C to 70°C)

Package Type	
160Q	160 Lead, Plastic Gull Wing Quad Flat Package (PQFP)
184Q	185 Lead, Plastic Gull Wing Quad Flat Package (PQFP)

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1 Product Information
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3 PERROMs (Flash)
4 EPROMs
5 PROMs
6 SRAMs
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Section 10

CMOS Smart Card ICs

AT24C01/02/04/08/16 Fact Sheet 2-Wire, 1K/2K/4K/8K/16K Serial E²PROM 10-3
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AT88SC06 16 x 1 104-Bit Serial E²PROM with Security 10-7

AT88SC101/102 1024 x 1 1K Serial E²PROM with Security, with
1 or 2 Memory Zones 10-15

AT88SC200 2048 x 1 2K Serial E²PROM with Gate Array 10-27

AT88SC416 16K x 8 80C31 Microprocessor with 16K E²PROM
and Public Key Math Coprocessor 10-31

RF ID ASICs Analog, Digital and Memory on
Customer-Defined Single-Chip ASIC 10-39

Features

- AT24C01/02/04/08/16
- Two-wire Serial Interface
- Supports ISO/IEC 7816-3 Synchronous Protocol
- Additional SDA Pad for ISO Compliant Packaging
- Low Voltage Operation Available from 1.8 to 6.0 Volts
- High Reliability and Endurance
  - 100,000 Write/Erase Cycles
  - 100 Years Data Retention
- Background Wafer and Die are Available from 6 to 21 mils
- Test Programs are Available for Testing Die in Cards
- Small Die Size Increases Reliability and Reduces Cost

Description

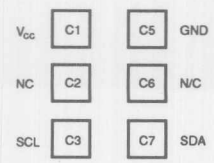
The AT24C01/02/04/08/16 provide 1024/2048/4096/8192/16384 bits of serial E²PROM (Electrically Erasable and Programmable Read Only Memory) organized as 128/256/512/1024/2048 words of 8 bits each. By grounding pins A2, A1, and A0, the devices can be used in smart card applications.

The AT24C01/02/04/08/16 is manufactured using low-power CMOS technology and features its own internal high voltage pump for single voltage supply operation. The devices are guaranteed to 100,000 write/erase cycles and 100 year data retention. The AT24C01 family supports the ISO/IEC 7816-3 synchronous protocol and is available in wafer, die, or standard package form.

ISO Card Configuration

Card Contact	Pin Name	Function
C1	V_{CC}	Operating Voltage
C2	NC	No Connect
C3	SCL	Serial Clock
C5	GND	Ground
C6	NC	No Connect
C7	SDA	Serial Data

2-Wire Card Module Contacts



Smart Card ICs

Using 2-Wire Serial E²PROMs In Smart Cards

AT24C01/02/04/08/16

Fact Sheet

10

Smart Card ICs

Using 2-Wire Serial E²PROMs In Smart Cards

ATZ4C01/02/04/08/16
Fact Sheet

10

Features

- AT93C46/56/57/66
- Organized as 8- or 16-bit Words
- User-Friendly Three-Wire Serial Protocol
- Comprehensive Instruction Set
- Low Voltage Operation Available from 1.8 to 6.0 Volts
- High Reliability and Endurance
  - 100,000 Write/Erase Cycles
  - 100 Years Data Retention
- Background Wafer and Die are Available from 6 to 21 mils
- Test Programs are Available for Testing Die in Cards
- Small Die Size Increases Reliability and Reduces Cost

Description

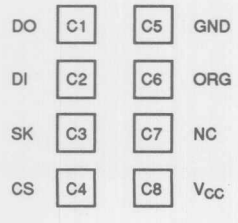
The AT93C46/56/57/66 provides 1024/2048/2048/4096 bits of serial E²PROM (Electrically Erasable Programmable Read Only Memory) organized as 64/128/256 words of 16 bits each when the ORG Pin is connected to V_{CC}, or 128/256/512 words of 8 bits each when it is tied to ground. The device is optimized for use in many smart card applications.

The AT93C46/56/57/66 is manufactured using low-power CMOS technology and features its own internal high voltage pump for single voltage supply operation. The devices are guaranteed to 100,000 erase/write cycles and 100 year data retention. The AT93C46/56/57/66 family is available in wafer, die, or standard package form.

ISO Card Configuration

Card Contact	Pin Name	Function
C1	DO	Serial Data Output
C2	DI	Serial Data Input
C3	SK	Serial Clock
C4	CS	Chip Select
C5	GND	Ground
C6	ORG	Internal Organization
C7	NC	No Connect
C8	V_{CC}	Operating Voltage

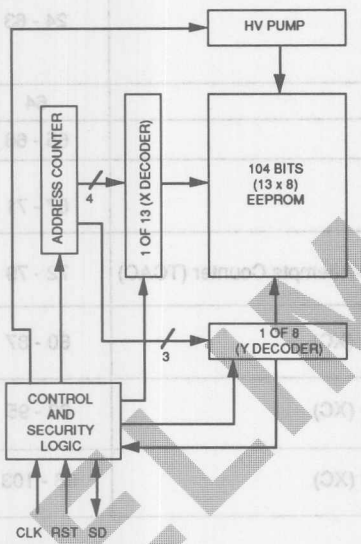
Card Module Contacts



Features

- 104 Bit E²PROM with Serial Control/Security Logic
- 13 x 8 (104) Bit Organization
- Operating Voltage (V_{CC} = 5.0V ± 19%)
- Dissipates 2.4 mW Read and 12.0 mW Max Write or Erase
- Provides Transport Code Security
- Counts up to 20480 Units Maximum
- Bi-directional Data Transfer for ISO/IEC 7816-3 Synchronous Protocol
- 1.5 ms Write or Erase Time
- ESD Immunity > 4 K Volts
- High Reliability and Endurance:
  - 100,000 Write/Erase Cycles
  - Data Retention: 100 Years Data Retention

Block Diagram



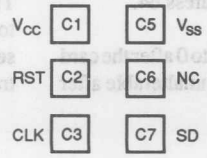
Description

The AT88SC06 provides 104 bits of serial E²PROM (Electrically Erasable and Programmable Read Only Memory) with security logic for use in secure smart card applications. The device has a register capacity of 20480 count units, and is internally organized as 13 eight-bit words for a total of 104 bits. Each bit is separately addressable by an internal seven-bit address counter for serial read and write

ISO Card Configuration

ISO Contact	Pad #	Pin Name	Description
C1	6	V_{CC}	Supply Voltage
C2	5	RST	Reset and Program Control
C3	4	CLK	Clock and Address Control
C5	1	V_{SS}	Ground
C6	2	NC	No Connect
C7	3	SD	Serial Data I/O

Card Module Contacts



PRELIMINARY

operations. Erase operations are allowed only by word after a bit-carry write has been performed.

The AT88SC06 is manufactured using low-power CMOS technology and features its own internal high-voltage pump for single-voltage supply operation. The devices are guaranteed to 100,000 erase/write cycles and 100 year data retention. Endurance up to one-million write cycles has been demonstrated. The AT88SC06 supports the ISO/IEC 7816-3 synchronous protocol and is available in wafer, die, or standard packaging.

AT88SC06 Memory Map

Memory Partitions			AT88SC06	
Primary Function		Secondary Function	Address	Bits
Chip Data (CHD)		(Read Only)	0 - 23	24
Issuer Data (ID)			24 - 63	40
Personalization Complete (PC)			64	1
Count Data	Test Bits (TB)		65 - 66	2
	Digit 5 (D5)		67 - 71	5
	Digit 4 (D4)	Transport Code Attempts Counter (TCAC)	72 - 79	8
	Digit 3 (D3)	Transport Code (XC)	80 - 87	8
	Digit 2 (D2)	Transport Code (XC)	88 - 95	8
	Digit 1 (D1)	Transport Code (XC)	96 - 103	8
TOTAL BITS				104

Definition of Memory Partitions

Chip Data (24 bits): Programmed by the manufacturer with a specific identifier for each customer. A fuse is blown by the manufacturer after programming the chip data, which makes this memory area unalterable.

Issuer Data (40 bits): Programmed by the card issuer during final personalization. The data stored in this memory area is unalterable after writing a 0 to address 64.

Personalization Complete (1 bit): Written to 0 after the card data has been personalized. Issuer data is unalterable after 0 is written to this bit.

Test Bits (2 bits): Allows pattern testing at this memory location.

Transport Code Attempts Counter (8 bits): Counts the number of attempted transport code compares. The device is locked after 8 compare attempts.

Transport Code (24 bits): Must be presented by the issuer to access circuit memory and personalize device before setting personalization complete bit. This secures transportation between the manufacturer and the issuer.

Pin Description

RESET (RST): The RST input is used to reset the memory counter to address zero or to indicate the intent to write or erase data. RST is pulled up to V_{CC} internally.

CLOCK (CLK): The CLK input is used to either increment the address counter and strobe data out or it is used to regulate the actual write or erase duration. CLK is also pulled up to V_{CC} internally.

SERIAL DATA (SD): The SD pin is bi-directional (open drain) for serial data transfer. During the transport code comparison, SD operates in a data input mode. During read operations, SD operates in a data output mode.

Transport Code Compare

Table 1 shows the access condition of the AT88SC06 when it is shipped from Atmel, and prior to comparing the transport code. A transport code compare is done by powering up the chip, setting the address location between 72-79 and writing a 0 into an erased ("1") location within this range. This write enables the transport code compare sequence which is valid until incrementing to address 0 or until the supply voltage is removed. Once the compare is enabled, the address counter is incremented to address 80, at which time SD will be the input for the 24 bit transport code entry, as shown in Figure 4.

If the enable and compare procedure was correct, the device will be enabled for initialization. If the compare was incorrect, additional compares may be attempted beginning with an address reset. A total of eight attempts are possible corresponding to the eight (initially high) bits in the address range of (72-79).

Device Operation Modes

Tables 2 and 3 indicate the access conditions of the AT88SC06 during device personalization and count mode, respectively. Once a correct transport code compare is made, the device is personalized and the initial counter value is assigned to reflect the desired user value. After the device is personalized, the personalization complete (PC) bit is set by writing a 0 to address 64. The device is in count mode. When all the bits in address range 67-103 are written, erasure is disabled and the device count is used up.

Table 1. AT88SC06 Access Conditions Prior to Transport Code Compare

Zones	PC	Read	Write 1 (Erase)	Write 0 (Prog)	Compare
CHD	1	YES	NO	NO	NO
ID	1	YES	NO	NO	NO
PC	1	YES	NO	NO	NO
TB	1	YES	NO	NO	NO
D5	1	YES	NO	NO	NO
TCAC (D4)	1	YES	NO	YES	NO
XC (D3 - D1)	1	NO	NO	NO	YES

Table 2. AT88SC06 Access Conditions During Personalization (Bit 64=1)[1]

Zones	PC	Read	Write 1 (Erase)	Write 0 (Prog)	Compare
CHD	1	YES	NO	NO	NO
ID	1	YES	NO	YES	NO
PC	1	YES	NO	YES	NO
TB	1	YES	NO	YES	NO
D5	1	YES	NO	YES	NO
D4 (TCAC)	1	YES	YES[2]	YES	NO
D3 - D1 (XC)	1	YES	YES[2]	YES	NO

Table 3. AT88SC06 Access Conditions After Personalization (Bit 64=0)[1]

Zones	PC	Read	Write 1 (Erase)	Write 0 (Prog)	Compare
CHD	0	YES	NO	NO	NO
ID	0	YES	NO	NO	NO
PC	0	YES	NO	NO	NO
TB	0	YES	NO	YES	NO
D5	0	YES	NO	YES	NO
D4 (TCAC)	0	YES	YES[2]	YES	NO
D3 - D1 (XC)	0	YES	YES[2]	YES	NO

Notes: 1. PC = personalization complete bit
2. Byte erase after bit-carry write

Device Operation

Address Reset and Read Data

(Refer to Figure 1)

To reset the address counter to address zero (0), first allow RST to go high followed by a CLK pulse (from low to high then back low). RST then must go low again such that it brackets CLK. Data (bit zero) is output on SD following RST going low. Each following pulse of CLK will increment the address counter (on rising edge) and strobe data out on SD (on falling edge). The address counter will roll-over, returning to zero after address 127.

Bit Write

(Refer to Figure 2)

With CLK low and RST low, a pulse of RST (from low to high and back to low) will enable a bit-write operation if the write is allowed at that address location. The next pulse of CLK will perform the write and regulate the write time duration. The address counter does not get incremented on this CLK write pulse, and the newly written data will be output on SD following the CLK write pulse. Data on SD will not be valid from the rising edge of RST until the falling edge of the write CLK pulse. A following CLK pulse with RST still low will increment the address counter as usual and strobe data our on SD.

Byte Erase After Bit-Carry Write

(Refer to Figure 3)

Byte erasures may be performed from addresses (72-103) on a byte-by-byte basis each preceded by a bit-carry write. The digit erased will always be the next lower digit than the digit the bit-carry write took place in. First, a bit write must be performed as shown in Figure 3. After the CLK write pulse is completed, RST is pulsed again which enables the word erase operation. A second CLK pulse is now given to perform the digit erase and regulate the erase time duration. The device control logic will verify that a bit-carry write (from "1" to "0") actually took place before erasing the next lower digit. Data on SD will not be valid from the rising edge of RST to the falling edge of the erase CLK pulse. The address counter will still be at the bit-carry write address following the byte erase.

Device Power up and Reset

After V_{CC} and V_{SS} have been contacted, powering up the device will internally reset the address counter to address zero. The internal power on reset circuit will reset the address counter if the device experiences dips in the supply voltage.

Count Principle

The address range (67-103) represents a five-digit non-resettable octal counter. The lower four octal digits are assigned a value between one and eight (addresses 72-103) during device initialization. The fifth and most significant digit is assigned values from one to five (addresses 67-71). This equates to (5 x 8E4=20480) count units. A single count unit is considered used (or cleared) when it is written to "0", and reset when erased during a byte, or digit, erase.

Changes in each digit by write and erase operations are driven by external software via the ISO protocol. Internal control logic governs allowed write and erase operations. Write operations, in the allowed address range, are unrestricted by the control log. Erase operations are not allowed until a bit in the next higher order count digit is written from a "1" to a"0". This is called a byte erase after bit-carry write as shown in Figure 3.

Figure 1. Address Reset and Read Timing Diagram

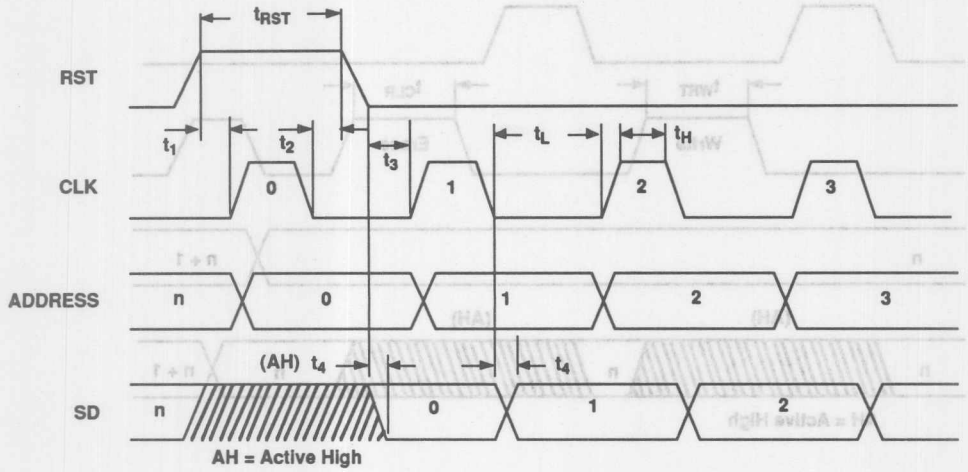
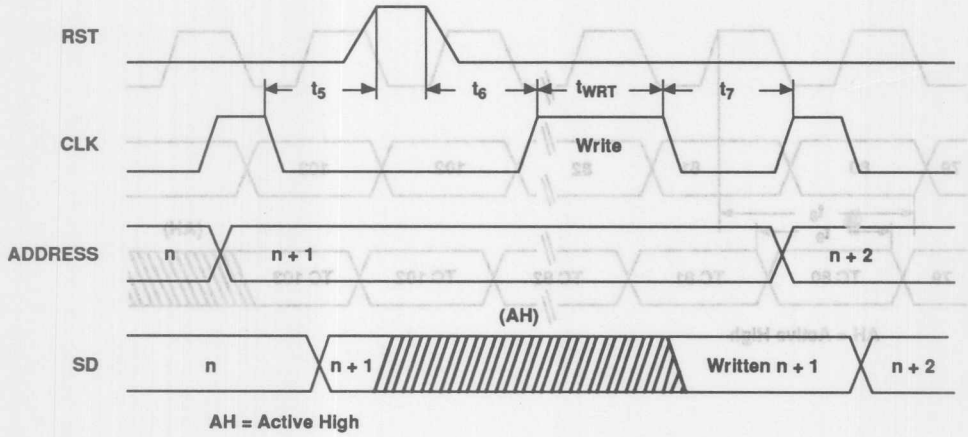


Figure 2. Bit Write Timing Diagram



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Figure 3. Byte Erase After Bit-Carry Write Timing Diagram

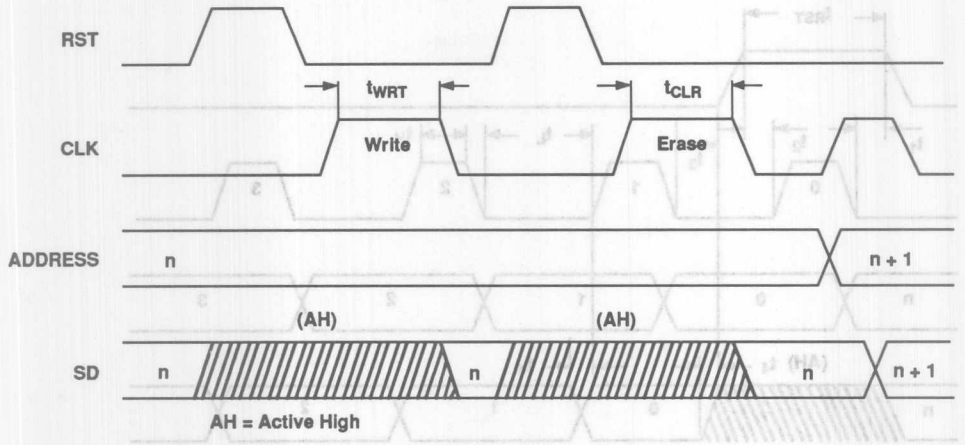
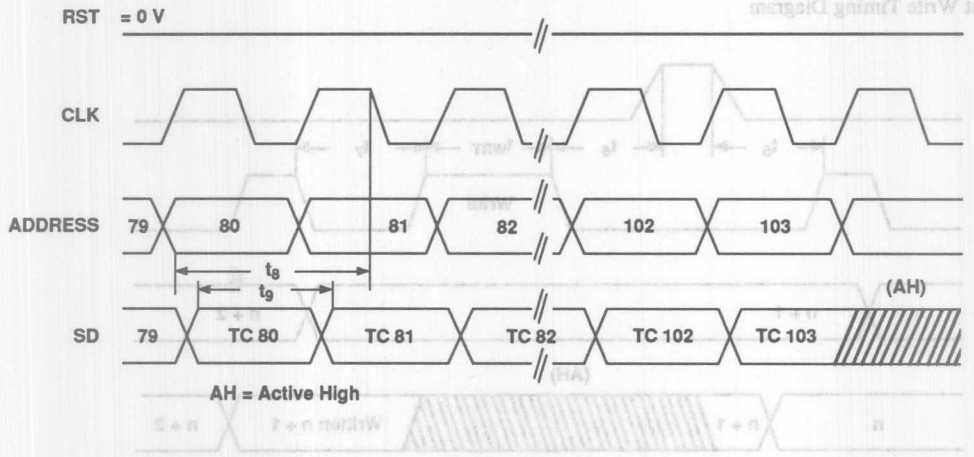


Figure 4. Transport Code Data Comparison Timing Diagram



Packaging

All Atmel smart card secure ICs are available in wafer, die, or standard packaging. All die can be tested and screened to either a commercial or industrial flow, and can be background to thicknesses of 6 to 21 mils, ± 0.2 mils. Standard packages include plastic DIPs, SOICs, PLCCs and micromodules.

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0 V to +7.0 V
Maximum Operating Voltage	6.6 V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics Die T_{AMB} = -40°C to + 85°C, V_{CC} = +5 V ± 10%, V_{SS} = 0V (Unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Suply Voltage	4.5	5.0	5.5	V
I_{CC1}	Supply Current (Read)	0.25	0.3	0.4	mA
I_{CC2}	Supply Current (Write)	1.0	1.5	2.0	mA
I_{SB}	Standby Current	1.0	9.0	12.0	µA
I_{IL}	Input Leakage Current			100.0	µA
I_{OL}	Output Leakage Current			10.0	µA
V_{IL}	Input Low Level(1)	-1.0		V_{DD} x 0.3	V
V_{IH}	Input High Level(1)	V_{SS} x 0.7		V_{DD} x 0.5	V
V_{OL}	Output Low Level (I_{OL} = 2.0 mA)			0.5	V

Note: 1. V_{IL} and V_{IH} max are reference only and are not tested.

AC Characteristics Die T_{AMB} = -40°C to + 85°C, V_{CC} = +5 V± 10%, V_{SS} = 0 V (Unless Otherwise Specified)

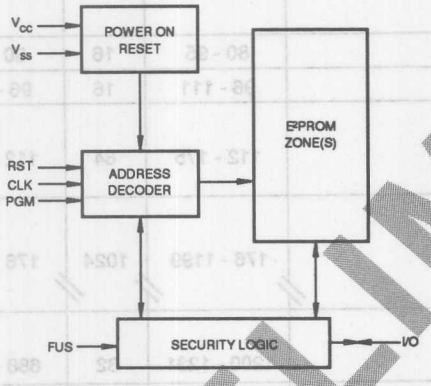
Symbol	Parameter	Min	Typ	Max	Unit
f_{RST}	Address Reset Pulse High	50			µs
t_R	Input Rise Time(1)			1	µs
t_F	Input Fall Time(1)			1	µs
t_L	CLK Pulse Low Width	10			µs
t_H	CLK Pulse High Width	10			µs
t_{WRT}	Write Operation Time	0.25	0.5	1.5	ms
t_{CLR}	Erase Operation Time	0.25	0.5	1.5	ms
t_1	Address Reset Setup Time	5			µs
t_2	Address Reset Hold Time	5			µs
t_3	CLK Low After Address Reset	10			µs
t_4	Data Propagation Delay	0.5			µs
t_5	RST Low After CLK Low	5			µs
t_6	CLK WRT Pulse After RST Low	5			µs
t_7	CLK Low After CLK WRT Pulse	10			µs
t_8	SD Valid For Input Data	0.1			µs
t_9	SD Input Data Setup Time	0.1			µs

Note: 1. This parameter is characterized and not 100% tested.
2. These write time parameters are the required minimum times depending on V_{CC} and temperature.

Features

- 1K x 1 Serial E²PROM With Security Logic
- Available in Two Memory Organizations:
  - AT88SC101 — 1 — 1K x 1 — Memory Zone
  - AT88SC102 — 2 — 512 x 1 — Memory Zones
- Supports ISO/IEC 7816-3 Synchronous Protocol
- Stores and Validates Security Codes
- Counts Incorrect Security Code Attempts
- Provides Transport Code Security
- Manufactured Using Low Power CMOS Technology
- V_{PP} Internally Generated
- 2 µs Read Access Time; 1 ms Write Cycle Time
- Temperature Range From -25°C to 70°C
- ESD Immunity > 4K Volts
- High Reliability:
  - 100,000 Write/Erase Cycles
  - 100 Years Data Retention
- Background Wafer and Die Available From 6 to 21 mils

Block Diagram



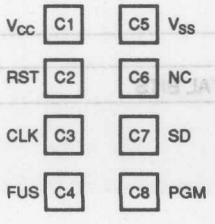
Description

The AT88SC101/102 family provides 1024 bits of serial E²PROM (Electrically Erasable and Programmable Read Only Memory) with additional security logic for use in secure smart card applications. The AT88SC101 is available in one 1024 x 1 bit memory zone, and the AT88SC102 is available in two 512 x 1 bit memory zones.

ISO Card Configuration

ISO Contact	Pad #	Pad Name	Description
C1	8	V_{CC}	Operating Voltage
C2	7	RST	Reset
C3	6	CLK	Clock and Address Control
C4	5	FUS	Identification Fuses
C5	1	V_{SS}	Ground
C6	2	NC	No Connect
C7	3	I/O	Bi-directional Data Port
C8	4	PGM	Programming Control

Card Module Contacts



Smart Card ICs

1K E²PROM with Security Logic

AT88SC101
AT88SC102
Preliminary

10

PRELIMINARY

The security features of Atmel's AT88SC101/102 include:

- data access only after validation of the security code
- permanent invalidation of device upon four consecutive false security code presentations
- read/write protection of certain memory zones
- device reset if power drops
- secure transport of devices using transport code compare sequence

The AT88SC101/102 is manufactured using low-power CMOS technology and features its own internal high-voltage pump for single voltage supply operation. The devices are guaranteed to 100,000 erase/write cycles and 100 year data retention. Endurance up to one-million Write cycles has been demonstrated. The AT88SC101/102 supports the ISO/IEC 7816-3 synchronous protocol.

AT88SC101 and AT88SC102 Memory Map

Memory Partitions	AT88SC101		AT88SC102	
	Address	Bits	Address	Bits
Fabrication Zone (FZ)	0 - 15	16	0 - 15	16
Issuer Zone (IZ)	16 - 79	64	16 - 79	64
Security Code (SC)	80 - 95	16	80 - 95	16
Security Code Attempts Counter (SCAC)	96 - 111	16	96 - 111	16
Code Protected Zone (CPZ)	112 - 175	64	112 - 175	64
Application Zone 1 (AZ1)	176 - 1199	1024	176 - 687	512
Application Zone 1 Erase Key (EZ1)	1200 - 1231	32	688 - 735	48
Application Zone 2 (AZ2)	---------	------	736 - 1247	512
Application Zone 2 Erase Key (EZ2)	---------	-----	1248 - 1279	32
Erase Counter (EC)	1232 - 1359	128	1280 - 1407	128
Memory Test Zone (MTZ)	1360 - 1375	16	1408 - 1423	16
TOTAL BITS		1376		1424

Definition of AT88SC101/102 Memory Partitions

FABRICATION ZONE (16 bits): Programmed by the manufacturer with a specific identifier for each customer. FUSE1 is blown by the manufacturer after programming the fabrication code, which makes the fabrication zone unalterable.

ISSUER ZONE (64 bits): Programmed by the issuer before finalizing personalization. The data stored in the issuer zone is unalterable after FUSE2 is blown.

SECURITY CODE (16 bits): Must be presented by the issuer to access circuit memory and personalize device before blowing FUSE2. This secures transportation between the manufacturer and the issuer. After the device is personalized and FUSE2 is blown, this code protects the access to the application zone(s) of the card.

SECURITY CODE ATTEMPTS COUNTER (16 bits): Counts the number of incorrect security code attempts. The device is locked after 4 false presentations.

USER PROTECTED ZONE (64 bits): Writing and erasing this zone is protected. The number of program/erase cycles is guaranteed up to 100,000.

APPLICATION ZONE(S) (1024 or 512 bits): Reading and programming the application zone(s) are controlled by the first 2 bits of the zone (PR, RD) and by the security code (Tables 1 and 2). The erasure of each zone is protected by an erase key specific to each zone.

APPLICATION ZONE ERASE KEY (32 or 48 bits): Must be presented to authorize the erasure of the application zone(s). The key(s) must be programmed during the personalization of the circuit.

ERASE COUNTER (128 bits): Limits the number of erasures of the last zone to 128 or less.

MEMORY TEST ZONE (16 bits): Allows pattern testing at this memory location.

Memory Access to AT88SC101 and AT88SC102

The access to the memory is controlled by the state of the internal fuses and by the voltage supply applied on the FUS pad:

FUS Pad Voltage	State of the FUSES		Access Conditions See:
	FUSE 1	FUSE 2	
0V	Either	Either	Table 2
5V	Blown	Not Blown	Table1
5V	Not Blown	Blown	Table 2

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Table 1. AT88SC101/102 Access Conditions During Personalization (FUSE 2 Not Blown)

Zones	SC	1PR	1RD	2PR	2RD	EZ1	EZ2	EC	READ	WRITE 1 (Erase)	WRITE 0 (PROG)	Compare
FZ	X	X	X	X	X	X	X	X	YES	NO	NO	NO
IZ	0	X	X	X	X	X	X	X	YES	NO	NO	NO
	1	X	X	X	X	X	X	X	YES	YES	YES	NO
SC	0	X	X	X	X	X	X	X	NO	NO	NO	YES
	1	X	X	X	X	X	X	X	YES	YES	YES	NO
SCAC	0	X	X	X	X	X	X	X	YES	NO	YES	NO
	1	X	X	X	X	X	X	X	YES	YES	YES	NO
CPZ	0	X	X	X	X	X	X	X	YES	NO	NO	NO
	1	X	X	X	X	X	X	X	YES	YES	YES	NO
AZ1	0	X	0	X	X	X	X	X	NO	NO	NO	NO
	0	X	1	X	X	X	X	X	YES	NO	NO	NO
	1	X	X	X	X	X	X	X	YES	YES	YES	NO
EZ1	0	X	X	X	X	X	X	X	NO	NO	NO	NO
	1	X	X	X	X	X	X	X	YES	YES	YES	NO
AZ2	0	X	X	X	0	X	X	X	NO	NO	NO	NO
	0	X	X	X	1	X	X	X	YES	NO	NO	NO
	1	X	X	X	X	X	X	X	YES	YES	YES	NO
EZ2	0	X	X	X	X	X	X	X	NO	NO	NO	NO
	1	X	X	X	X	X	X	X	YES	YES	YES	NO
EC	0	X	X	X	X	X	X	X	YES	NO	YES	NO
	1	X	X	X	X	X	X	X	YES	YES	YES	NO
MTZ	X	X	X	X	X	X	X	X	YES	YES	YES	NO

Notes:

SC: SC = 1 after validation of security code
1PR: 1st bit of AZ1 (Bit 176)
1RD: 2nd bit of AZ1(Bit 177)
2PR: 1st bit of AZ2 (Bit 736) - AT88SC102 only
2RD: 2nd bit of AZ2 (Bit 737) - AT88SC102 only
EZ1: EZ1 = 1 after a valid presentation of erase key 1
EZ2: EZ2 = 1 after a valid presentation of erase key 2
EC: EC = 1 when the counter is not empty.

Table 2. AT88SC101/102 Access Conditions After Personalization (FUSE 2 Blown)

Zones	SC	1PR	1RD	2PR	2RD	EZ1	EZ2	EC2	READ	WRITE 1 (Erase)	WRITE 0 (PROG)	Compare
FZ	X	X	X	X	X	X	X	X	YES	NO	NO	NO
IZ	X	X	X	X	X	X	X	X	YES	NO	NO	NO
SC	0	X	X	X	X	X	X	X	NO	NO	NO	YES
	1	X	X	X	X	X	X	X	NO	YES	YES	NO
SCAC	0	X	X	X	X	X	X	X	YES	NO	YES	NO
	1	X	X	X	X	X	X	X	YES	YES	YES	NO
CPZ	0	X	X	X	X	X	X	X	YES	NO	NO	NO
	1	X	X	X	X	X	X	X	YES	YES	YES	NO
AZ1	0	X	0	X	X	X	X	X	NO	NO	NO	NO
	0	X	1	X	X	X	X	X	YES	NO	NO	NO
	1	0	X	X	X	0	X	X	YES	NO	NO	NO
	1	0	X	X	X	1	X	X	YES	YES	NO	NO
	1	1	X	X	X	0	X	X	YES	NO	YES	NO
	1	1	X	X	X	1	X	X	YES	YES	YES	NO
EZ1	X	X	X	X	0	X	X	X	NO	NO	NO	YES
AZ2	0	X	X	X	0	X	X	X	NO	NO	NO	NO
	0	X	X	X	1	X	X	X	YES	NO	NO	NO
	1	X	X	0	X	X	0	X	YES	NO	NO	NO
	1	X	X	0	X	X	X	0	YES	NO	NO	NO
	1	X	X	0	X	X	1	1	YES	YES	NO	NO
	1	X	X	1	X	X	0	X	YES	NO	YES	NO
	1	X	X	1	X	X	X	0	YES	NO	YES	NO
	1	X	X	1	X	X	1	1	YES	YES	YES	NO
EZ2	0	X	X	X	X	X	X	X	NO	NO	NO	YES
EC	X	X	X	X	X	X	X	X	YES	NO	YES	NO
MTZ	X	X	X	X	X	X	X	X	YES	YES	YES	NO

Notes:

SC: SC = 1 after validation of security code
1PR: 1st bit of AZ1 (Bit 176)
1RD: 2nd bit of AZ1(Bit 177)
2PR: 1st bit of AZ2 (Bit 736) - AT88SC102 only
2RD: 2nd bit of AZ2 (Bit 737) - AT88SC102 only
EZ1: EZ1 = 1 after a valid presentation of erase key 1
EZ2: EZ2 = 1 after a valid presentation of erase key
EC: EC = 1 when the counter is not empty.

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Modes of Operation

The AT88SC101/102 has four operation modes selected by PGM, RST, CLK, and by the internal counter:

Inputs Micro Instructions	PGM	RST	CLK	Definitions
RESET	X	⌝_	0	The address counter is reset to 0 and the first bit of the memory is available on I/O after RST and CLK hit 0. Note: The INC instruction is disabled when RST is high (Figure 1). Address counter is reset on the falling edge of RESET.
INC (INC/READ)	0	0	⌝⌜	The address counter is incremented and the first bit is available on I/O after the falling edge of the clock (unless reading is forbidden) (Figure 2). Address increments on falling edge of CLK. Data is released after the falling edge of CLK.
CMP (INC/CMP)	0	0	⌝⌜	Comparison of the bit presented to the card to the internal bit of the memory (for secret codes only). The bit should stay stable on I/O during the time CLK is low. The address counter is incremented on the falling edge of the CLK (Figure 3).
WRITE	1	0	_⌜	I/O must be positioned on 0 for programming or on 1 for erasure before the rising edge of CLK which must stay on 1 for at least 5ms. The bit addressed (which will be written) is available on I/O after the falling edge of the CLK (Figure 4).
VERIFY	0	0	⌝_	

Notes:
1. Output is disabled (Hi state) on addresses where read is disabled.
2. If V_{DD} falls between approximately 3V and 4V the chip will execute a power-on reset.
3. The 2 instructions CMP and UP are coded (0,0) on CLK and PGM. The circuit will distinguish between the 2 instructions by testing the internal address counter (CMP can only be done with the addresses corresponding to the security code or erase key.
4. The internal address counter counts up to 1519 for 101and 1567 for 102. An additional INC sets the counter to 0.

Table 5. AT88SC101/102 Micro Instructions

Instruction	Bit	Word	Application Zone	Global (When Fuse 2 = 1)
READ	RESET n INC; position counter on bit	-------	-------	-------
WRITE (WRITE 0)	RESET n INC; position counter on bit WRITE 0 INC; go to next bit WRITE 0;...	-------	-------	RESET n INC; n = 1392 (101) n = 1440 (102) WRITE 0
ERASE (WRITE 1)	-------	RESET n INC; position counter on any bit in word WRITE 1 n INC; position counter on any bit in next word WRITE 1...	verify erase keys AT88SC101 Zone 1/88SC102 Zone 2: RESET 32 CMP n INC; n = 1232 (101), n = 1280 (102) VERIFY 1; verify 1 in EC WRITE 0; write 0 in EC WRITE 1; erase application zone AT88SC102 Zone 1: RESET 48 CMP n INC; n = 736 WRITE 1; erase application zone	RESET n INC; n = 1392 (101) n = 1440 (102) WRITE 1
CMP • SECURITY CODE	-------	RESET 79 INC; position counter on bit preceding SC 16 CMP; verify security code n INC; If none of the 1st 4 bits of the FAC is 1, then 4 unsuccessful attempts have been made to verify SC, and the device is inoperable. If any of the 1st 4 bits is a 1, then: WRITE 0 WRITE 1; Reset the FAC	-------	-------
CMP • ERASE KEYS	-------	RESET n INC; position counter on bit preceding access code or erase key n CMP; verify access code or erase key ; n = 32 or 48 bits	-------	-------

Figure 1. Reset

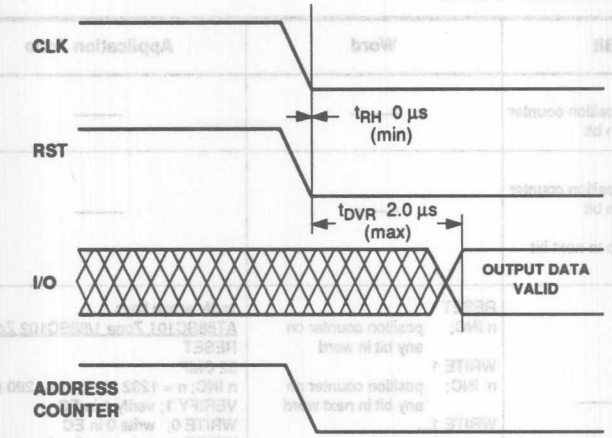


Figure 2. Read Timing

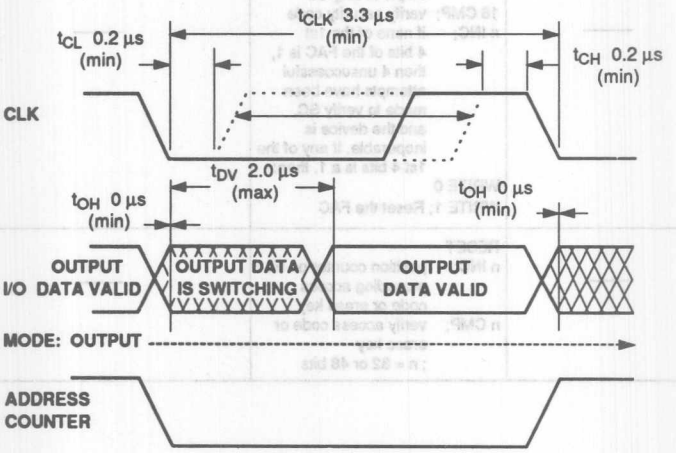


Figure 3. Compare Timing

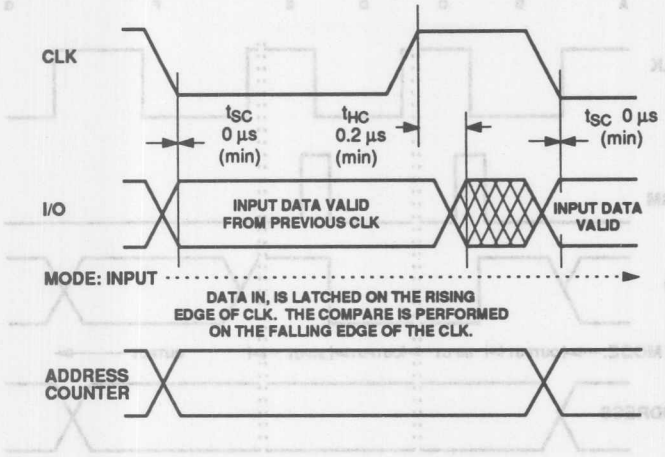
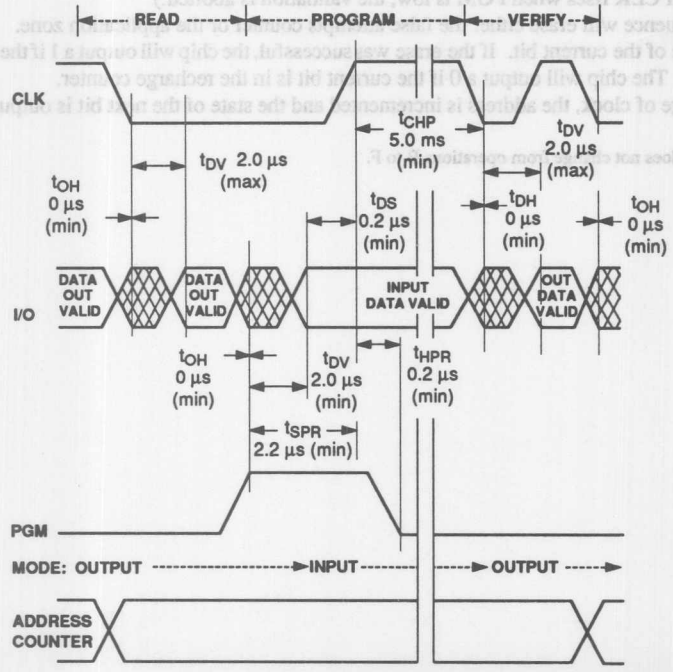
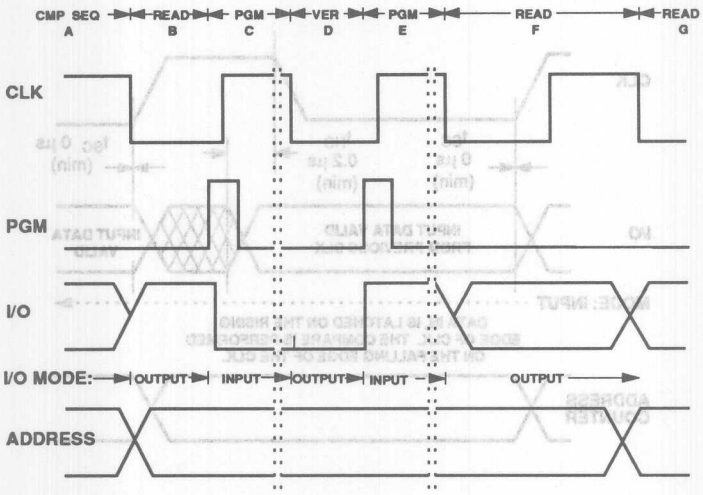


Figure 4. Program Timing



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Figure 5. SC and EZ1/EZ2 Validation for AT88SC101/102



A) Compare sequence of the security code or the application zone erase key.
B) First bit which is at a logic 1, in the false attempts counter to validate SC, or in the recharge counter to validate EZ.
C) Program sequence attempts to write a 0 over the 1 currently at this address.
D) The chip outputs the new state of the bit. If a 0 has been successfully programmed, SC or EZ is set on the rising edge of PGM. (Note: If CLK rises when PGM is low, the validation is aborted.)
E) This program sequence will erase either the false attempts counter or the application zone.
F) Chip outputs state of the current bit. If the erase was successful, the chip will output a 1 if the current bit is in the false attempts counter. The chip will output a 0 if the current bit is in the recharge counter.
G) On the falling edge of clock, the address is incremented and the state of the next bit is output.

Note: 1. The address does not change from operations B to F.

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0 V to +7.0 V
Maximum Operating Voltage	6.6 V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Die T_{AMB} = –25°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0 V (unless otherwise specified)

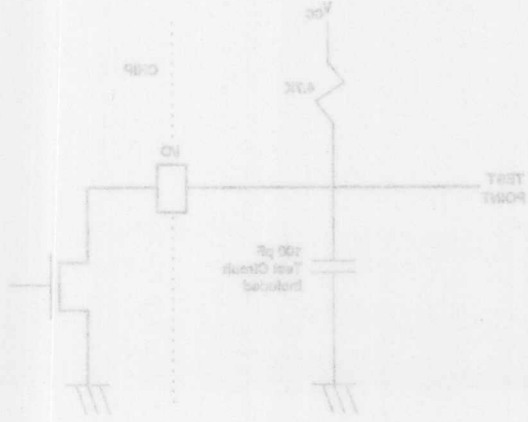
Symbol	Characteristics	Min	Typ	Max	Unit
I_{CC}	Supply Current on V_{CC} out of	-	-	3.0	mA
	Program (t_{AMB} = + 25 C).				
I_{CCP}	Supply Current on V_{CC} during	-	-	4.0	mA
	Program (t_{AMB} = + 25 C).				
I_{CCSB}	Standby Current on V_{CC}	-	-	100	µA
	(RST @ V_{CC}, FUS, CLK, PGM @ V_{SS}				
	I_{IO} = 0µA. f_{CLK} = 0 KHz).				
V_{IL}	Input Low Level	–0.3	-	0.8	V
V_{IH}	Input High Level	2.0	-	V_{CC}+1	V
V_{OL}	Output Low Level (I_{OL} = 1mA)	-	-	0.4	V
I	I/O Leakage Current	-50	-	50	µA

Notes: 1. There is a pullup on pin RST.
2. There are pulldowns on pins FUS, CLK and PGM.

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Packaging

All Atmel smart card secure ICs are available in wafer, die, or standard packaging. All die can be tested and screened to either a commercial or industrial flow, and can be background to thicknesses of 6 to 21 mils, ± 0.2 mils. Standard packages include plastic DIPs, SOICs, PLCCs and micromodules.



AC Characteristics

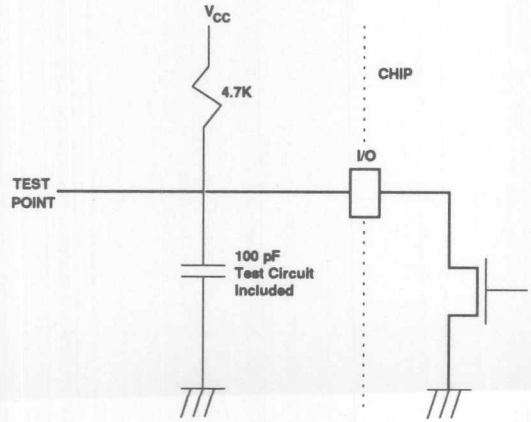
Die T_{AMB} = –25°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V (unless otherwise specified).

Symbol	Characteristics	Min	Typ	Max	Unit
f_{CLK}	Clock Frequency	-	-	300	KHz
t_{CLK}	Clock Cycle Time	3.3	-	-	µs
t_{RH}	RST Hold Time	0	-	-	µs
t_{DVR}	Data Valid Reset to Address 0	-	-	2.0	µs
t_{CH}	CLK Pulse Width (High)	0.2	-	-	µs
t_{CL}	CLK Pulse Width (Low)	0.2	-	-	µs
t_{DV}	Data Access	-	-	2.0	µs
t_{OH}	Data Hold	0	-	-	µs
t_{SC}	Data In Setup (CMP Instruction)	0	-	-	µs
t_{HC}	Data In Hold (CMP Instruction)	0.2	-	-	µs
t_{CHP}	CLK Pulse Width (High in Programming)	5.0	-	-	ms
t_{DS}	Data In Setup	0.2	-	-	µs
t_{DH}	Data In Hold	0	-	-	µs
t_{SPR}	PGM Setup	2.2	-	-	µs
t_{HPR}	PGM Hold	0.2	-	-	µs
t_{DH}	Data Hold from CLK	0	-	-	µs

Conditions of Dynamic Tests

The circuit has an output with open drain. An external resistance is thus necessary between V_{CC} and I/O in order to load the output.

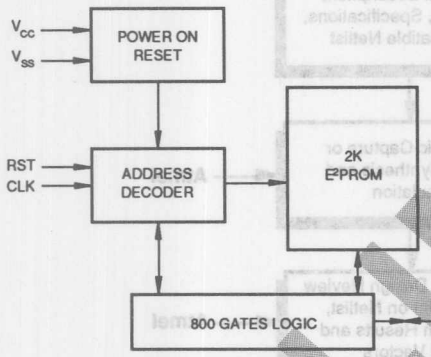
Pulse Levels of the Input:	V_{ss} to 3.0V
Reference Levels in Input:	0.8V and 2.0V
Reference Levels in Output:	0.8V and 2.0V
Rising and Falling Time of Signals:	5ns



Features

- 2K x 1 Serial E²PROM
- 800 Usable Gates
- Low Voltage Operation (3.0 to 6.0 Volts)
- Memory can be Segmented and Protected
- Performs Block Functions on 8-, 16-, 32-, and 64-Bit Words
- Five E²PROM Fuses for Control and Security
- Manufactured Using Low Power CMOS Technology
- V_{PP} Internally Generated
- 2 µs Read Access Time; 1 ms Write or Erase Time
- Temperature Range from -40°C to 85°C
- ESD Immunity > 4K Volts
- High Reliability and Endurance:
  - 100,000 Write/Erase Cycles
  - 25 Years Data Retention
- High Voltage Capability for RF Interface
- Ideal for Smart Cards, ID Tags, Keys, and Other Secure, Portable, Applications

Block Diagram



Description

The AT88SC200 provides 2048 bits of serial E²PROM (Electrically Erasable and Programmable Read Only Memory) with 800 gates of usable CMOS for use as personalization, security, and glue logic. The AT88SC200 is ideal for high-volume applications requiring 2K E²PROM with custom logic, such as smart cards, ID tags, keys, and other secure, portable applications.

Pad Configuration

Pad #	Pad Name	Description
1	V_{SS}	Ground
2	U/D	User Defined
3	U/D	User Defined
4	U/D	User Defined
5	U/D	User Defined
6	CLK	Clock and Address Control
7	RST	Reset
8	V_{CC}	Operating Voltage

Smart Card ICs

2K Serial E²PROM with Gate Array

AT88SC200 Preliminary

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PRELIMINARY

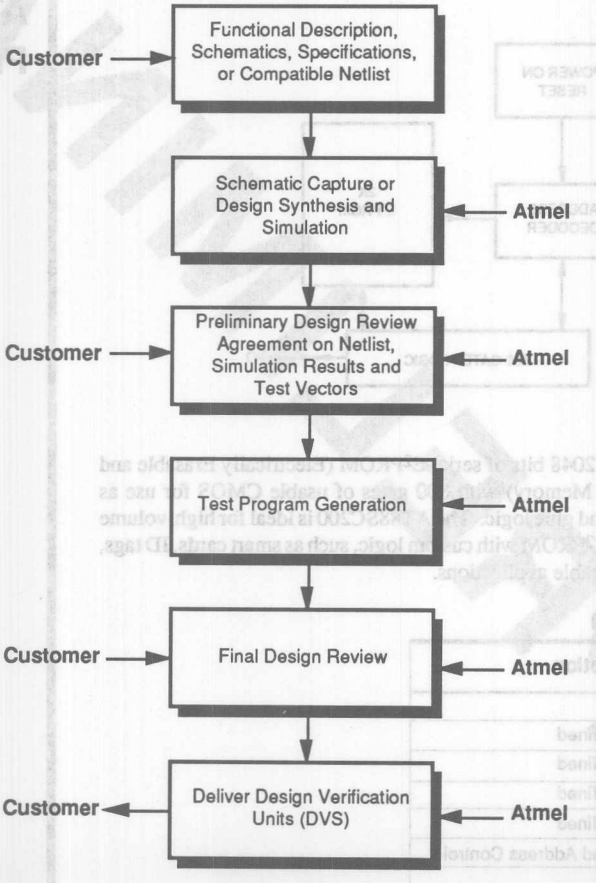
The outputs of the AT88SC200 can sink and source up to 7 mA. The inputs are TTL compatible and use a Schmitt Trigger design. The device also provides pull-down and pull-up capability for floating signals. The AT88SC200 is manufactured using low-power CMOS technology and features its own internal high voltage pump for single voltage supply operation. The devices are guaranteed to 100,000 erase/write cycles and 100 year data retention. Endurance up to one–million write cycles has been demonstrated.

Atmel will personalize the 800 gates of logic as described in Figure 1. The customer's design will be accepted in one of three formats:

- Functional Description
- Schematic
- Compatible Netlist

Compatible netlists can be generated from Mentor™, Cadence™, Viewlogic™, Dasix™ and Valid Tools™. The personalized devices are available in wafer, die, micromodule, or standard packages.

Figure 1. AT88SC200 Design Flow



Cadence, Dasix, Mentor, Valid Tools and Viewlogic may be trademarks of others.

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0 V to +7.0 V
Maximum Operating Voltage	6.6 V
DC Output Current	5.0 mA

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DC Characteristics

Die T_{AMB} = –40°C to +85°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V (unless otherwise specified)

Symbol	Characteristics	Min	Typ	Max	Unit
I_{CC}	Supply Current on V_{CC} out of Program (t_{AMB} = + 25°C).	-	-	3.0	mA
I_{CCP}	Supply Current on V_{CC} during Program (t_{AMB} = + 25°C).	-	-	4.0	mA
V_{IL}	Input Low Level	–0.3	-	0.8	V
V_{IH}	Input High Level	2.0	-	V_{CC}+1	V
V_{OL}	Output Low Level (I_{OL} = 7 mA)	-	-	0.4	V
V_{OH}	Output High Level (I_{OH} = 7 mA)	2.4	-	-	V
I_L	I/O Leakage Current	-50	-	50	µA

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Packaging

All Atmel smart card secure ICs are available in wafer, die, or standard packaging. All die can be tested and screened to either a commercial or industrial flow, and can be background to thicknesses of 6 to 21 mils, ± 0.2 mils. Standard packages include plastic DIPs, SOICs, PLCCs and micromodules.

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V_{OL}	Output Low Level (I_{OL} = 7 mA)	-	-	0.4	V
V_{OH}	Output High Level (I_{OH} = 7 mA)	2.4	-	-	V
I_L	I/O Leakage Current	-50	-	50	µA

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Packaging

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Features

- Enhanced Intel 80C31 Microcontroller Offers Maximum Security for High Security Smart Card Applications
- 8 Kbytes E²PROM Program Memory Provides Higher Level of Security than Traditional ROM
- 8 Kbytes E²PROM Application/Data Memory
- 768 Bytes Internal RAM
- 512-bit Public Key Math Coprocessor Performs Modular Exponentiation in 2.0 Seconds
- Supports Public Key Protocols-RSA, DSA, and Diffie-Hellman
- Optional OS Implements Secure Hashing Functions, DES, Access Control Protocols, Digital Signatures, and Key Management Schemes
- 100% Field-Programmability Provides Maximum Flexibility
- Advanced Internal Security Allows New Applications to be Downloaded and Executed Without Compromising System Security
- Programmable Memory Access Control Protects Critical Sections of Program/Data Memory
- ISO/IEC 7816-3 Compliant

Description

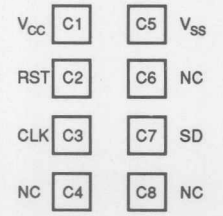
The AT88SC54C is an 80C31-based smart card device designed specifically for the high-security, public key cryptosystem marketplace. In addition to an enhanced 80C31 core, the device contains a 512-bit public key math coprocessor (PKC) that performs a 512-bit modular exponentiation in 1.5 seconds. The coprocessor includes a built-in random number generator and contains 3 Kbits of additional RAM for operands to enable CPU independent operation.

The AT88SC54C contains a total of 16 Kbytes of Electrically Erasable and Programmable Read Only Memory (E²PROM) and 768 bytes of RAM. 8 Kbytes of E²PROM is available for program memory, which provides a higher level of code security than traditional ROM. Using E²PROM for program memory also provides additional flexibility by allowing the application code to be programmed at either the wafer or card level. The remaining 8 Kbytes of E²PROM is available for application/data memory.

ISO Card Configuration

ISO Contact	Pad #	Pad Name	Description
C1	8	V_{CC}	Operating Voltage
C2	7	RST	Reset
C3	6	CLK	Clock
C4	5	NC	No Connect
C5	1	V_{SS}	Ground
C6	2	NC	No Connect
C7	3	I/O	Bi-directional Data Port
C8	4	NC	No Connect

Card Module Contacts



Smart Card ICs

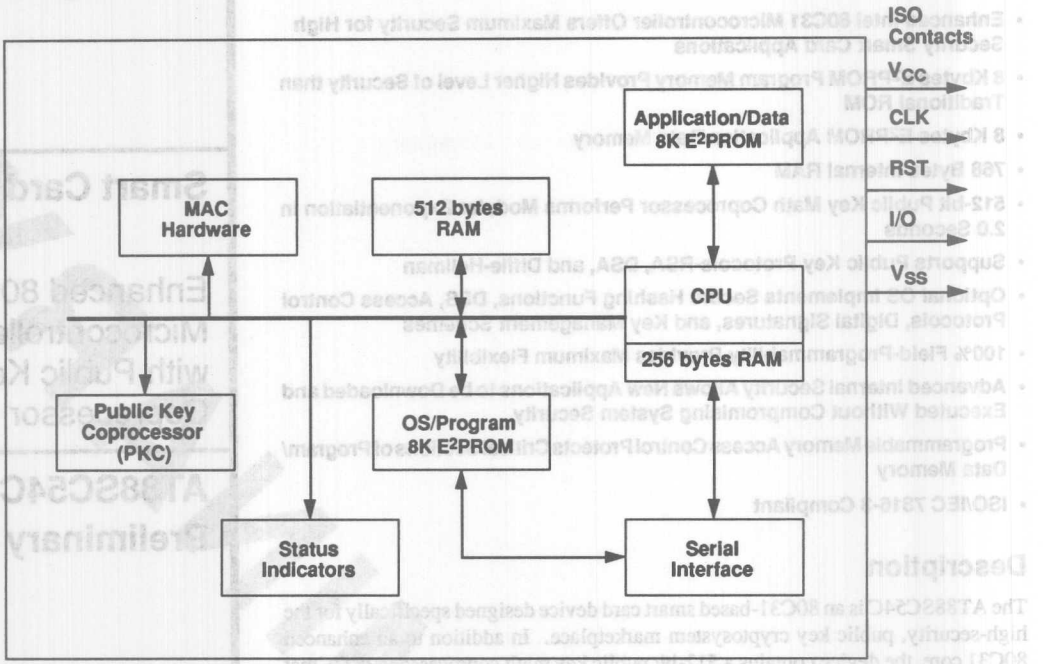
Enhanced 80C31 Microcontroller with Public Key Coprocessor

AT88SC54C Preliminary

PRELIMINARY

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Block Diagram



The device is compatible with the industry standard 80C31 microcontroller instruction set. The AT88SC54C contains 256 bytes of scratch pad RAM, two 16-bit timer/counters and a five-source, two-level interrupt architecture The AT88SC54C supplies all the necessary timing and high voltage functions required for programming the E²PROM and no external support circuits are required.

The 8K bytes of E²PROM are guaranteed to 100,000 Write/Erase cycles and 100 years data retention. Endurance up to one-million write cycles has been demonstrated.

The AT88SC54C is specifically designed to meet the rigorous security demands of the high-security smart card marketplace. The public key coprocessor (PSC) supports the public key algorithms of RSA, Diffie-Hellman, DSA, etc. Software libraries are available to implement secure hashing functions, DES, access control protocols, digital signatures and key management schemes.

The AT88SC54C, combined with advanced security software, is ideal for high-security applications such as public key digital signature generation and verification, access control, personal identification and authentication, cryptographic key management, payment systems and off-line transactions.

Table 1. AT88SC54C Memory Map

Device /Memory Module	Memory Type
Public Key Coprocessor (PKC)	Data
8K x 8 E²PROM	Program/OS
8K x 8 E²PROM	Application/Data
512 Bytes RAM	Data
I/O Module	Data
Memory Access Controller (MAC)	Data
OS Entry Point Control Module	Data
Status Indicators	OTP
Fuses	OTP

Functional Description

At the core of AT88SC54C is an enhanced 80C31 microcontroller. The E²PROM, RAM and public key coprocessor are integrated with the 80C31 microcontroller into a single chip. Several enhancements to the operation of 80C31, along with the built-in programmable memory access controller, OS entry point controller, and one-time programmable status indicators achieve the security objectives of the AT88SC54C.

Enhanced 80C31 Microcontroller meets the advanced security objectives of the AT88SC54C. The 80C31 enhancements include:

- Detection of program execution from address range 0 to 1FFFh.
- Detection of MOVC, LCALL, RET, RETI, LJMPand JMP instructions.
- Loads a 0FFh into accumulator when a MOVC instruction is executed from address range beyond 1FFFh and the source of the constant is in address range 0 to 1FFFh.
- A memory access or OS entry point violation or execution of the instructions LCALL, RET, RETI, LJMP and JMP by the code in the application program space generates a non-maskable interrupt. An interrupt service routine can be written to take appropriate action.

Public Key Math Coprocessor (PKC) provides processing capability for public key cryptography math.

8K x 8 Program Memory E²PROM contains 8K bytes of OS, program, or OS and application code. The OS is loaded at the wafer level, and the application code can be programmed at the wafer level or can be serially programmed using the OS and the serial port of the AT88SC54C.

8K x 8 Data Memory E²PROM can be used as either application or data memory, and contains fuses for write/erase protection as well as test and status fuses. This memory can be segmented and protected in 512 byte blocks if more than 8K of program memory is needed.

512 Bytes RAM provides additional scratch pad memory for the OS, RSA and other application code. Since the address decoding circuitry partitions the memory in 4K blocks, images of the 512 byte RAM occupy the entire 4K range at intervals of 512 bytes.

I/O Module consists of an 8-bit buffer and an 8-bit latch. Data can be read or written from these ports.

MAC Module can be programmed to prevent access to a contiguous block of memory. When programmed, the MAC controls access to memory from program code that is executed from an address range beyond 1FFFh.

OS (Internal Code Space) Entry PointControll Module provides the ability to control the point of entry into the OS code space by programming an entry point address.

Status Indicators can only be written with a value of 1. These indicators are accessible by the codeexecuted in the address range 0 to 1FFFh. There are 8 status indicators. These can be used by the OS code to provide additional security features.

Fuses are available for memory protection, test, and other security features.

Public Key Math Coprocessor

The public key math coprocessor (PKC) accelerates the computations required to implement public key cryptography. The coprocessor can perform addition, multiplication, and exponentiation modulo an arbitrary integer. This capability can be used for implementing public key algorithms such as RSA, DSA, and Diffie-Hellman, for digital signature and key management purposes.

The PKC can handle operands up to 512 bits in length. A modular exponentiation using 512-bit operands will typically take less than 2.0 seconds when using an input clock frequency of 11.0592 MHz. By using a higher input clock rate, as well as other mathematical techniques depending on the particular cryptosystem being implemented, this time can be significantly reduced.

The PKC contains 3000 bits of dedicated RAM for operand and result storage. Computations require no intervention by the 80C31 microcontroller other than loading the operands and starting the desired calculation by writing to the correct address. The PKC indicates completion of the calculation by setting a "READY" bit which the application code can poll for.

As part of its design, the PKC incorporates logic to facilitate the implementation of a high-quality digital pseudorandom number generator. The PKC operates by repeatedly squaring a secret seed value modulo a large prime. After each squaring operation, the least-significant bit of the result is shifted into a holding register 1. These bits are then available for use by an application requiring "random" data. For example, this feature is useful when implementing challenge-response protocols or certain types of digital signature schemes. The strength of the generator depends *on keeping the seed value secret. Facilities for secure* storage of data are built into the memory access control architecture of the AT88SC54C.

1 For more information on this technique please see: Blum L., Blum M., and Shub M., "Comparison of two pseudorandom number generators", Proceedings of CRYPTO '82, Plenum Press, 1983, pp. 61-78

Serial Programming Interface

The OS code can be loaded at the wafer or card level by using a 3-wire serial programming interface that requires the control input pins of RST, CLK and I/O.

Serial programming operations are controlled by five instructions issued by the user. A valid instruction consists of a start bit (logic '1') followed by the appropriate op code and the desired memory address code and data bits.

READ (READ): The READ instruction contains the address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location are available at the serial I/O pin. Output data changes are synchronized with the falling edges of clock (CLK).

ERASE/WRITE ENABLE (EWEN): To assure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An EWEN instruction must be executed first before any programming instructions can be carried out. Please note that once in the EWEN state, programming remains enabled until an EWDS instruction is executed or V_{DD} power is removed from the part.

WRITE (WRITE): The WRITE instruction contains the 8 bits of data to be written into the specified memory location. The self-timed programming cycle starts after the last bit of data is received. The I/O pin outputs a 'Low' to indicate that E2PROM programming is still in progress and goes into high impedance state when programming is completed.

ERASE/WRITE DISABLE (EWDS): The EWDS instruction disables all programming modes and should be executed after all programming operations. The operation of the READ instruction is independent of both the EWEN and EWDS instructions and can be executed any time.

ERASE ALL (ERAL): The ERAL instruction programs every bit in the memory array to the logic '1' state. The ERAL instruction is externally timed by keeping the I/O pin at V_{SS} level for 10 ms after the op code. The ERAL instruction must be executed before any of the memory array can be re-programmed.

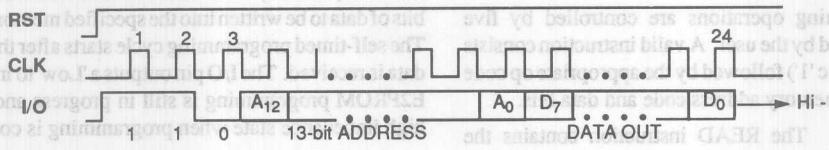
Instruction Set For Serial Programming Interface

Instruction	Smart Bit	OP Code	Address MSB LSB	Data MSB LSB
READ	1	10	A12 - A0	D7 - D0 (out)
EWEN	1	00	11XXXXXXXXXX	
WRITE	1	01	A12 - A0	D7 - D0 (in)
EWDS	1	00	00XXXXXXXXXX	
ERAL	1	00	10XXXXXXXXXX	

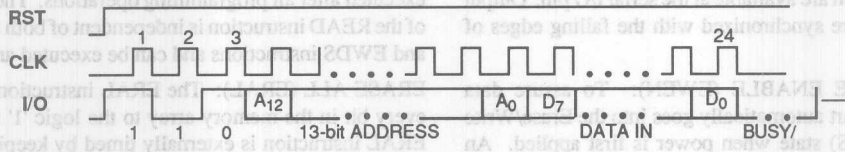
Notes:
1. All instructions must be supplied with the exact number of clock cycles.
2. Invalid instructions will not be executed.
3. I/O pin must be held low during normal reset operation if boot fuse is not blown.

Serial Programming Interface Timing

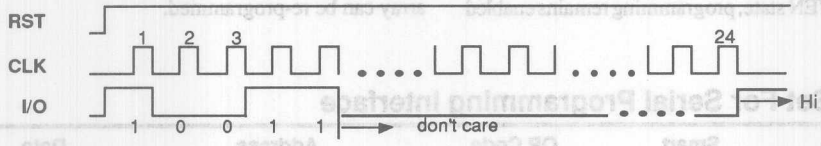
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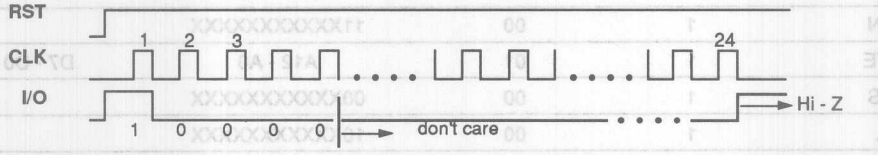
WRITE:



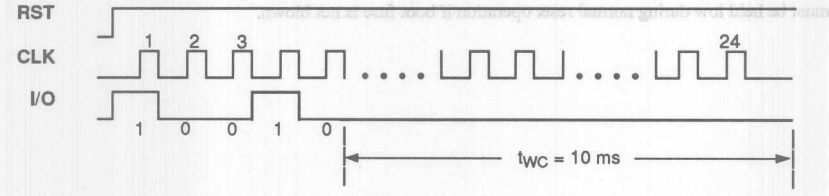
EWEN:



EWDS:



ERAL:



Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0 V to +7.0 V
Maximum Operating Voltage	6.6 V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ISO Contact Electrical Characteristics

DieT_{AMB} = -40°C to + 85°C, V_{DD} = 5 V ±10%, V_{SS} = 0 (Unless Otherwise Specified)

Symbol	Parameter	Min	Max	Unit
I/O Contact				
V_{IH}	I_{IH} max = +/-500 µA	2.0	V_{CC}	V
	I_{IH} max = +/-20 µA	0.7 x V_{CC}		
V_{IL}	I_{IL} max = -1 mA	0	0.8	V
V_{OH}	I_{OH} max = -100 µA	2.4	V_{CC}	V
	I_{OH} max = -20 µA	3.8		
V_{OL}	I_{OL} max = +1 mA	0	0.4	V
t_R, t_F	C_{IN}, C_{OUT} = 30 pF		1	µsec
Clock Contact				
V_{IH}	I_{IH} max = +/-200 µA	2.4	V_{CC}	V
	I_{IH} max = +/-20 µA	0.7 x V_{CC}		
	I_{IH} max = +/-10 µA	V_{CC} - 0.7	V_{CC}	V
V_{IL}	I_{IL} max = +/-200 µA	0	0.5	V
t_R, t_F	C_{IN} = 30 pF		9% of period max = 0.5	µsec
RST Contact				
V_{IH}	I_{IH} max = +/-200 µA	4	V_{CC}	V
	I_{IH} max = +/-10 µA	V_{CC} - 0.7		
V_{IL}	I_{IL} max = +/-200 µA	0	0.6	V
V_{CC} Contact				
V_{CC}		4.75	5.25	V
I_{CC}			200	mA

10

Packaging

All Atmel smart card secure ICs are available in wafer, die, or standard packaging. All die can be tested and screened to either a commercial or industrial flow, and can be background to thicknesses of 6 to 21 mils, ± 0.2 mils. Standard packages include plastic DIPs, SOICs, PLCCs and micromodules.

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V_{OH}	I_{OH} max = -100 µA	2.4	V_{CC}	V
	I_{OH} max = -20 µA	3.8		
V_{OL}	I_{OL} max = +1 mA	0	0.4	V
t_R, t_F	C_{IN}, C_{OUT} = 20 pF		1	µsec
Clock Contact				
V_{IH}	I_{IH} max = +/-200 µA	2.4	V_{CC}	V
	I_{IH} max = +/-20 µA	0.7 x V_{CC}		
	I_{IH} max = +/-10 µA	V_{CC} - 0.7	V_{CC}	V
V_{IL}	I_{IL} max = +/-200 µA	0	0.8	V
t_R, t_F	C_{IN} = 20 pF		8% of period max = 0.8	µsec
RST Contact				
V_{IH}	I_{IH} max = +/-200 µA	4	V_{CC}	V
	I_{IH} max = +/-10 µA	V_{CC} - 0.7		
V_{IL}	I_{IL} max = +/-200 µA	0	0.8	V
V_{CC} Contact				
V_{CC}		4.75	5.25	V
I_{CC}			200	mA

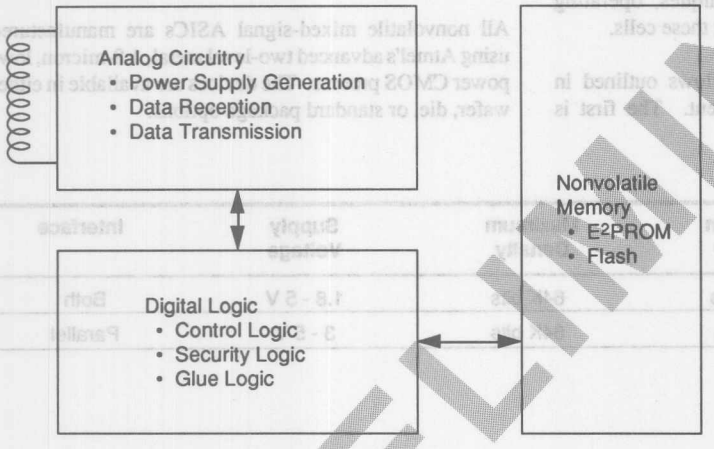
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Features

- Single Chip Solution-Analog + Digital + Memory
- Option to Eliminate External Components (Batteries, Capacitors, Coils)
- Customized Security Features
- Optimized Analog Cells:
  - Voltage Rectifier
  - Voltage Regulator
  - Operational Amplifier
  - Bandgap Voltage Reference
  - Phase Locked Loop
  - Voltage Controlled Oscillator
- Enhanced Digital Library with Boundary Scan, Logic Macrocells, and 80C31 Microcontroller Cell
- Advanced E²PROM and Flash Memory Technology
- Choice of COT or Turnkey Design Flow
- Ideal for Contactless Smart Cards, Electronic Tags, Electronic Keys
- Used in Identification, Access, and Monetary Value Applications:
  - Toll Usage
  - Parking
  - Mass Transit
  - ID Tags
  - Vending Machines
  - Sensors

Block Diagram



Description

Atmel's nonvolatile, mixed-signal ASICs are ideal for the emerging radio frequency (RF) identification (ID) marketplace. These ASICs combine nonvolatile memory, digital logic, and analog circuitry on a single chip to meet the requirements of contactless, nonvolatile data storage and retrieval devices. These monolithic devices can be packaged in contactless smart cards, and electronic keys, tokens and tags for a variety of applications, including road tolls, parking, mass transit, ID tags, and vending machines.

A unique silicon design capability allows customers to design monolithic RF ASICs with the option of eliminating all external components (batteries and capacitors) and all physical electrical contacts. Depending upon the application, the ASICs can interface with external coils, or use a relatively new "coil-on-chip" technology for power supply generation and for data reception and transmission. This level of integration and miniaturization provides the ideal monolithic, low-cost device that is required by the RF ID marketplace.

PRELIMINARY

Atmel's nonvolatile, mixed-signal ASICs are comprised of three distinct components: 1) nonvolatile memory, 2) digital logic, and 3) analog circuitry. The nonvolatile memory is available in E²PROM or Flash in the densities shown in Table 1. The memories feature an internal high-voltage pump for single voltage operation, and are guaranteed from 1,000 to 100,000 erase/write cycles and up to 100 years data retention, depending on which memory type is used. The E²PROM and Flash memories also support applications that have low-power and low-voltage requirements, with supply voltages ranging from 1.8 to 6 volts, again depending on the memory type and the circuit design.

Several analog cells have been designed and optimized to meet the needs of RF ID applications. These cells and their specifications are listed in Table 2. Atmel currently designs and manufactures nonvolatile, mixed-signal ASICs that cover a variety of modulation techniques, operating frequencies, and operating ranges using these cells.

Atmel supports two primary design flows outlined in Figure 1. and a third is in development. The first is customer owned tooling (COT). Atmel supplies design rules, electrical rules, SPICE™ models, and any analog or digital cells that are required. After the design is completed, the customer provides a design database tape in GDSII™ format, as well as a test program and test vectors, then Atmel drops in the appropriate nonvolatile memory.

In a turnkey design, also shown in Figure 1, the customer provides a firm product specification and schematics, and Atmel performs the design in conjunction with third party design houses located throughout the world. The third design flow entails the development of a mixed-signal, nonvolatile library that will be ported to several popular workstations in the future. Atmel's digital library is currently available on Mentor Graphics™, Cadence™, and Viewlogic™ workstations. The library supports boundary scan and includes over a hundred gates, muxes, latches, flip-flops, and buffers, as well as several logic macro cells.

All nonvolatile mixed-signal ASICs are manufactured using Atmel's advanced two-level metal, 1.8-micron, low-power CMOS process. The devices are available in either wafer, die, or standard package options.

Table 1.

Memory Type	Minimum Density	Maximum Density	Supply Voltage	Interface
E²PROM	104 bits	64K bits	1.8 - 5 V	Both
Flash	1K bits	64K bits	3 - 5 V	Parallel

Cadence, GDSII, Mentor Grpahics, SPICE and Viewlogic may be trademarks of others.

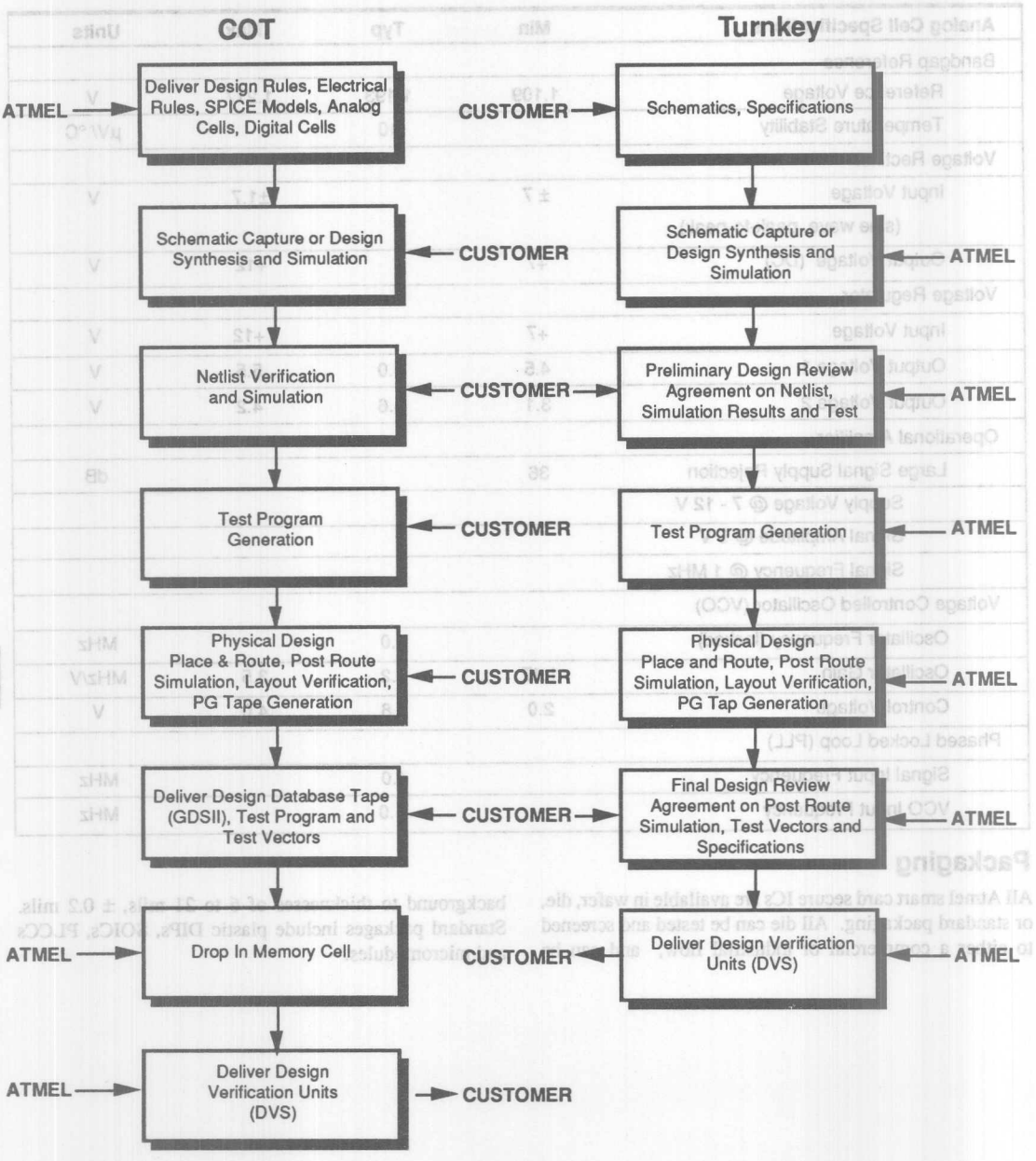
Table 2.
$Die T_{AMB}$ = -25°C to +85°C

Analog Cell Specifications	Min	Typ	Max	Units
Bandgap Reference				
Reference Voltage	1.109	1.193	1.277	V
Temperature Stability		10		µV/ °C
Voltage Rectifier				
Input Voltage (sine wave, peak-to-peak)	± 7		±1.7	V
Output Voltage (DC)	+7		+12	V
Voltage Regulator				
Input Voltage	+7		+12	V
Output Voltage 1	4.5	5.0	5.5	V
Output Voltage 2	3.1	3.6	4.2	V
Operational Amplifier				
Large Signal Supply Rejection	36			dB
Supply Voltage @ 7 - 12 V				
Signal Amplitude @ 5 V				
Signal Frequency @ 1 MHz				
Voltage Controlled Oscillator (VCO)				
Oscillator Frequency (locked)		4.0		MHz
Oscillator Gain	1.47	2.2	3.5	MHz/V
Control Voltage	2.0	2.8	4.0	V
Phased Locked Loop (PLL)				
Signal Input Frequency		4.0		MHz
VCO Input Frequency		4.0		MHz

Packaging

All Atmel smart card secure ICs are available in wafer, die, or standard packaging. All die can be tested and screened to either a commercial or industrial flow, and can be background to thicknesses of 6 to 21 mils, ± 0.2 mils. Standard packages include plastic DIPs, SOICs, PLCCs and micromodules.

Figure 1. RF ID ASIC Design Flows



Product Information 1
E^2PROMs 2
PEROMs (Flash) 3
EPROMs 4
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1 Product Information
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Contents

Section 11

CMOS Mixed Signal

AT76C10	4 kHz	Programmable, Phone Line Equalizer	11-3
AT76C10E	4 kHz	Programmable, Phone Line Equalizer with On-Board E^2PROM	11-11
AT76C120	96 kHz	Dual Channel 16/18-Bit A/D Converters	11-19
AD-120		Analog Interface System	11-27
AT76C176	66 MHz	Triple, 6-Bit Color Palette DAC	11-31
AT76C176A	50-110 MHz	Triple, 6-Bit Color Palette DAC with Power-Down	11-43

Mixed Signal Application Notes

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AT76C176A Color Palette DAC 11-65

11

CMOS Programmable Amplifier Delay Equalizer

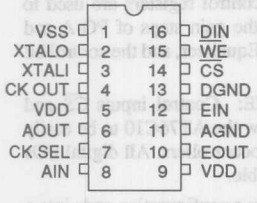
Features

- High Accuracy Programmable Gain Amplifiers
  - ± 0.02 dB Accuracy (Typical)
  - 31.5 dB Range in 0.5 dB Steps
- Software Programmable Group Delay Equalizer For Leased and Dial-Up Lines
- High Dynamic Range - over 90 dB
- On-Chip Anti-Aliasing Filters
- Microcomputer Interface with Serial Data Port
- Three Convenient Clock Options
  - 11.0592 MHz
  - 3.6864 MHz
  - 2.4576 MHz (or 2.56 MHz)
- Operates from ± 5 V Supplies
- Low Power Standby Mode - 100 µA (Typical)
- TTL and CMOS Compatible Digital Interface
- Economical 16-Lead Package
- Full Military, Commercial and Industrial Temperature Ranges

Description

The AT76C10 integrates two Programmable Gain Amplifiers and a Programmable Telephone Line Group Delay Equalizer on a monolithic substrate. It is fabricated in a state-of-the-art, low power CMOS process. The Gain and Group Delay steps are controlled by a seven-bit configuration code which can be programmed in real time. The AT76C10 is implemented in an advanced switched-capacitor technology and is designed to provide precise Gain and Group Delay compensation for low bit-error-rate data transmission over dial-up and leased lines. Anti-alias and clock filters are included on-chip as the AT76C10 employs sampled-data techniques, and external filters are not required for most applications.

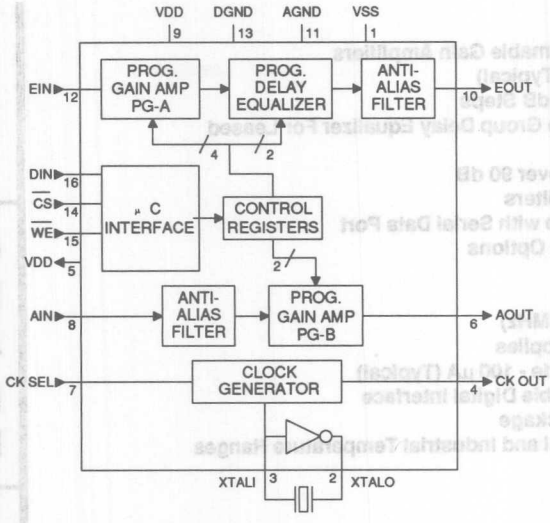
Pin Configuration



Pin Definitions

No.	Pin Name	Function
1	VSS	Negative Power Supply. Nominal -5 Volts.
2	XTALO	Crystal Oscillator Output.
3	XTALI	Crystal Oscillator Input.
4	CK OUT	Sampling Clock Output. (Open Drain)
5	VDD	Connect to VDD.
6	AOUT	PG-B Analog Signal Output.
7	CK SEL	Clock Select. Selects one of the 3 recommended Clock frequencies.
8	AIN	PG-B Analog Signal Input.
9	VDD	Positive Power Supply. Nominal +5 Volts.
10	EOUT	Delay Equalizer Analog Signal Output.
11	AGND	Analog Ground.
12	EIN	Delay Equalizer Analog Signal Input.
13	DGND	Digital Ground.
14	$\overline{CS}$	Chip Select Control Input.
15	$\overline{WE}$	Write Enable Control Input.
16	DIN	Serial Data Input.

Block Diagram



Device Operation

The AT76C10 is designed for use in the signal paths of a modem or voice/data phone to minimize the bit-error-rate over dial-up and leased lines. Gain and Group Delay response of the AT76C10 are controlled by a serial seven-bit configuration code. D1 and D0 of the configuration code are the address bits which select one of the three control registers. Bits D2 to D5 set the gain and delay equalizer steps. D6 is an option bit which controls the power down mode. All the functions associated with the configuration code are summarized in Tables 1 to 4.

Configuration Code Format

D6	D5	D4	D3	D2	D1	D0
Option Select	Control Code				Address	

This chip can be used as part of an adaptive equalizer for medium to high speed modems (1200 bps to greater than 19.2K bps). The configuration code is loaded into the chip at a serial data input port and updated in real time. The amplitude response of the equalizer is nominally at 0 dB with negligible ripple. The AT76C10 can also be used as a fixed compromise delay equalizer.

PROGRAMMABLE GAIN AMPLIFIER: The AT76C10 provides two high dynamic range amplifiers for maximizing signal-to-noise ratio. Amplifier PG-A offers 16 programmable gain steps from 0 dB to 7.5 dB in 0.5 dB steps. Amplifier PG-B provides -8 to 16 dB of gain in 8 dB steps. The two amplifiers can be cascaded to provide 31.5 dB range of programmable gain in 0.5 dB steps. The Programmable Amplifiers can be used as an Automatic Gain Control Circuit or as a fixed gain adjustment.

PROGRAMMABLE GROUP DELAY EQUALIZER: The Group Delay Equalizer is designed to provide programmable compromise group delay compensation to achieve low bit-error-rate data transmission. Four group delay responses are provided to accommodate the majority of conditioned as well as unconditioned lines. The first three responses are recommended for line types C2 and C1, while the fourth response can be used for 3002-type lines. Two or more AT76C10s can be cascaded to obtain additional group delay compensation.

CONTROL REGISTERS: Four control registers are used to store the configuration codes for the gain steps of PG-A and PG-B, the delay steps of the Delay Equalizer, and the control bit for the power-down mode.

MICROCOMPUTER INTERFACE: Control inputs $\overline{CS}$ and $\overline{WE}$ and serial data input DIN allow the AT76C10 to be easily interfaced with most popular microcontrollers. All digital I/Os are TTL as well as CMOS compatible.

WRITE OPERATION: To program a configuration code into a particular control register, the voltage at $\overline{CS}$ has to be brought low while the data bits appearing at DIN are strobed in at the rising edge of $\overline{WE}$. At the rising edge of $\overline{CS}$, the last seven input data bits are latched into the control registers.

POWER-DOWN MODE: To minimize power consumption for battery powered applications and in certain linecard applications, the AT76C10 provides a low power standby mode of operation. In the power-down mode, the analog outputs go into a high impedance state. The power-down mode is initiated by writing a "0" into the power-down register. Once in the power-down mode, the AT76C10 can be reactivated by writing a "1" into the power-down register. It should be noted that upon powering up the AT76C10 for the first time, it automatically goes into the normal active mode of operation.

CRYSTAL OSCILLATOR: Internal timing of the chip is generated either by connecting a crystal across pins XTALI and XTALO of the on-chip oscillator, or by applying an external clock at pin XTALI. In the latter case, pin XTALO should be left unconnected. To accommodate different applications, three clock options: 2.4576 MHz, 3.6864 MHz and 11.0592 MHz, can be selected via control pin CK SEL. For applications in a linecard environment, a 2.56 MHz clock can be used instead of the 2.4576 MHz clock. The 153.6 kHz (160 kHz with 2.56 MHz clock) sampling clock is available as an open drain output at CK OUT for synchronization or driving other circuits, e.g. the transmit or receive filters, or A/D and D/A converters.

CK SEL	Recommended XTAL Frequency	CK OUT
VDD	11.0592 MHz	153.6 kHz
DGND	3.6864 MHz	153.6 kHz
VSS	2.4576 MHz	153.6 kHz
VSS	2.56 MHz	160.0 kHz

Group Delay Characteristics (Microseconds)

Fs = 153.6 kHz

Frequency (Hz)	Step #1	Step #2	Step #3	Step #4
300	158	278	416	284
600	188	336	502	386
900	237	463	681	680
1200	325	671	985	1360
1500	431	890	1330	1791
1700	462	938	1382	1838
1900	435	897	1305	1810
2100	372	777	1144	1510
2400	266	542	808	683
2700	181	361	534	342
3000	136	250	368	213
3300	102	182	267	148

Table 1. Option Selection

Address D1	Address D0	Option Bit D6	Function
0	0	1	Updates Control Registers
0	1	1	
1	0	1	
1	1	0	Power Down Mode
1	1	1	Active Mode

Table 2. Equalizer Selection

Address D1	Address D0	Control Code D5	D4	D3	D2	Equalizer Step No.	Recommened Line Condition
0	0	X	X	0	0	1	C2
0	0	X	X	0	1	2	C1
0	0	X	X	1	0	3	C1
0	0	X	X	1	1	4	3002

Table 3. Programmable Gain Amplifier, PG-A

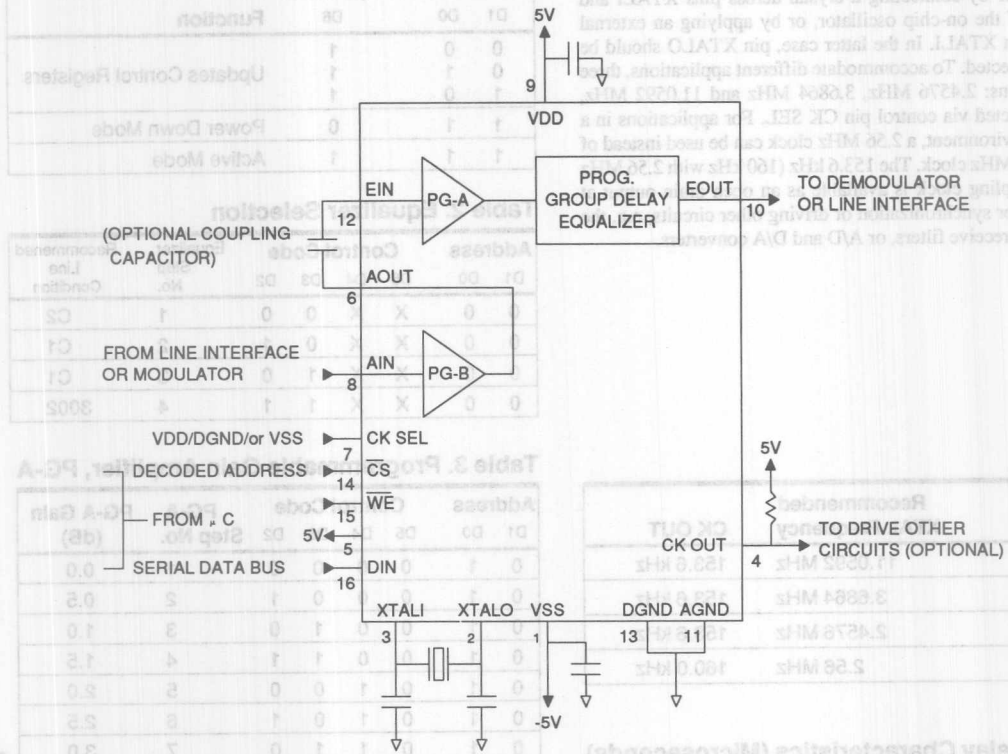
Address D1	Address D0	Control Code D5	D4	D3	D2	PG-A Step No.	PG-A Gain (dB)
0	1	0	0	0	0	1	0.0
0	1	0	0	0	1	2	0.5
0	1	0	0	1	0	3	1.0
0	1	0	0	1	1	4	1.5
0	1	0	1	0	0	5	2.0
0	1	0	1	0	1	6	2.5
0	1	0	1	1	0	7	3.0
0	1	0	1	1	1	8	3.5
0	1	1	0	0	0	9	4.0
0	1	1	0	0	1	10	4.5
0	1	1	0	1	0	11	5.0
0	1	1	0	1	1	12	5.5
0	1	1	1	0	0	13	6.0
0	1	1	1	0	1	14	6.5
0	1	1	1	1	0	15	7.0
0	1	1	1	1	1	16	7.5

Table 4. Programmable Gain Amplifier, PG-B

Address D1	Address D0	Control Code D5	D4	D3	D2	PG-B Step No.	PG-B Gain (dB)
1	0	X	X	0	0	1	0.0
1	0	X	X	0	1	2	8.0
1	0	X	X	1	0	3	16.0
1	0	X	X	1	1	4	-8.0

X = Don't Care

11



Absolute Maximum Ratings*

Temperature Under Bias	-55° C to 125° C
Storage Temperature	-65° C to 150° C
Voltage on Pins AGND and DGND with Respect to VSS	-0.6 V to 6.25 V
All Voltages with Respect to VSS	-0.6 V to VDD + 0.6 V

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D.C. and A.C. Operating Range

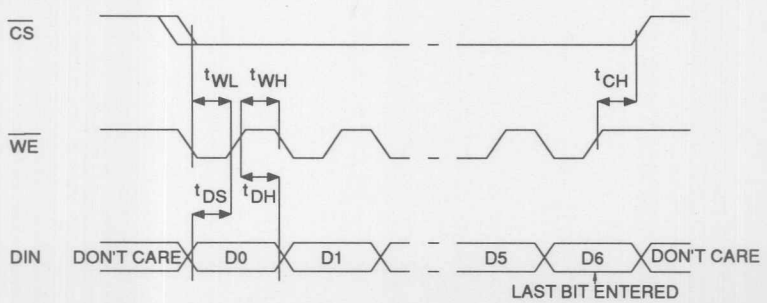
	Operating Temperature (Case)	VDD / VSS Power Supplies
Commercial	0° C - 70° C	5 V / -5 V ±10%
Industrial	-40° C - 85° C	5 V / -5 V ±10%
Military	-55° C - 125° C	5 V / -5 V ±5%

Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DDO}	VDD Quiescent Current (active mode)			3	6	mA
I_{SSO}	VSS Quiescent Current (active mode)			3	6	mA
I_{DDP}	VDD Quiescent Current (power-down mode)			100	500	µA
I_{SSP}	VSS Quiescent Current (power-down mode)			100	500	µA
R_{IA}	Input Resistance at AIN		100			kohm
R_{IE}	Input Resistance at EOUT	F_S=153.6 kHz	1			Mohm
C_I	Input Capacitance				20	pF
ROA	Ouput Resistance at AOUT				1	kohm
ROE	Ouput Resistance at EOUT				200	ohm
F_O	Center Frequency			1700		Hz
DT	Group Delay Tolerance		-1.5		+1.5	%
GT	Gain Tolerance		-0.05		0.05	dB
G_O	Insertion Loss		-0.15		0.15	dB
V_O	Output Voltage	RL = 20 kohm	VSS		VDD	V
V_N	Output Noise	BW = F_S/2			200	µVrms
THD	Total Harmonic Distortion	RL = 20 kohm V_O = 8 Vpp		0.1	0.5	%
F_S	Sampling Frequency			153.6		kHz
V_{FT}	Clock Feedthrough				5	mVpp

11

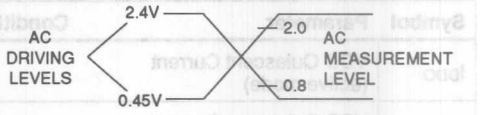
Configuration Code Write Waveform



Digital Timing Parameters

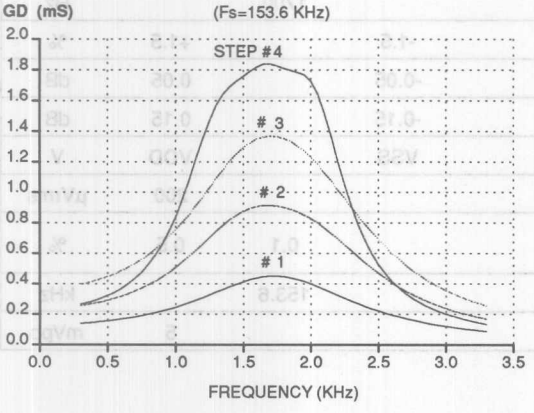
Symbol	Parameter	Min	Max	Units
t_{WL}	Write Enable Low	50		ns
t_{WH}	Write Enable High	50		ns
t_{CH}	$\overline{CS}$ Hold Time	100		ns
t_{DS}	Data Setup Time	40		ns
t_{DH}	Data Hold Time	40		ns

Input Test Waveform

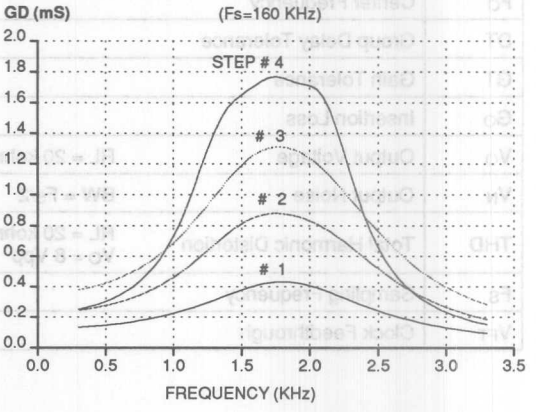


t_R, t_F < 20 ns (10% to 90%)

Typical Group Delay Response



Typical Group Delay Response



Ordering Information

Delay (ms)	Gain (dB)	Power Supply	Bandwidth (KHz)	Ordering Code	Package	Operation Range
1.8	31.5	±10%	4	AT76C10-PC AT76C10-SC	16P3 16S	Commercial (0°C to 70°C)
				AT76C10-PI AT76C10-SI	16P3 16S	Industrial (-40°C to 85°C)
1.8	31.5	±5%	4	AT76C10-DM	16D3	Military (-55°C to 125°C)

Package Type	
16D3	16 Lead, 0.300" Wide Non-Windowed, Ceramic Dual Inline Package (Cerdip)
16P3	16 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
16S	16 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)

Delay (ns)	Gain (dB)	Power Supply	Bandwidth (10Hz)	Ordering Code	Package	Operation Range
1.8	31.5	±10%	4	ATT86C10-PC ATT86C10-SC	16P3 16S	Commercial (0°C to 70°C)
				ATT86C10-PI ATT86C10-SI	16P3 16S	Industrial (-40°C to 85°C)
1.8	31.5	±5%	4	ATT86C10-DM	16D3	Military (-55°C to 125°C)

Package Type	
16D3	16 Lead, 0.300" Wide Non-Windowed, Ceramic Dual Inline Package (Cerdip)
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16S	16 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)

CMOS E²PROM Programmable Amplifier Delay Equalizer

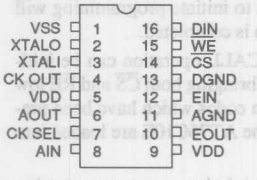
Features

- **High Accuracy Programmable Gain Amplifiers**
  - **± 0.02 dB Accuracy (Typical)**
  - **31.5 dB Range in 0.5 dB Steps**
- **Software Programmable Group Delay Equalizer For Leased and Dial-Up Lines**
- **High Dynamic Range - over 90 dB**
- **On-Chip Anti-Aliasing Filters**
- **On-Chip E²PROM Configuration Code Memory**
- **Microcomputer Interface with Serial Data Port**
- **Three Convenient Clock Options**
  - **11.0592 MHz**
  - **3.6864 MHz**
  - **2.4576 MHz (or 2.56 MHz)**
- **Operates from ± 5 V Supplies**
- **Low Power Standby Mode - 100 µA (Typical)**
- **TTL and CMOS Compatible Digital Interface**
- **Economical 16-Lead Package**
- **Full Military, Commercial and Industrial Temperature Ranges**

Description

The AT76C10E integrates two Programmable Gain Amplifiers and a Programmable Telephone Line Group Delay Equalizer on a monolithic substrate. It is fabricated in a state-of-the-art, low power CMOS process. The Gain and Group Delay steps are controlled by a seven-bit configuration code which can be programmed in real time and can also be stored permanently in on-chip E²PROMS. The AT76C10E is implemented in an advanced switched-capacitor technology and is designed to provide precise Gain and Group Delay compensation for low bit-error-rate data transmission over dial-up and leased lines. Anti-alias and clock filters are included on-chip as the AT76C10E employs sampled-data techniques, and external filters are not required for most applications.

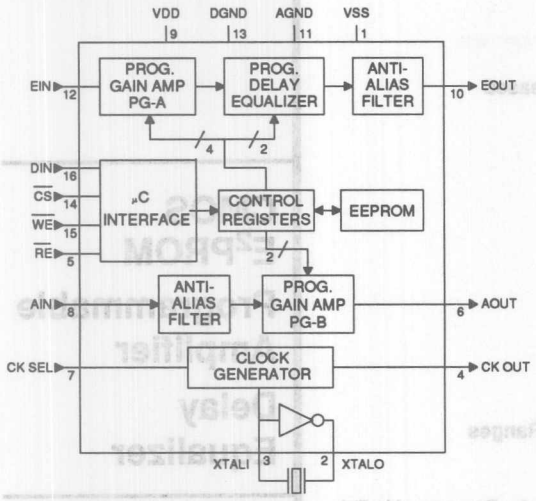
Pin Configuration



Pin Definitions

No.	Pin Name	Function
1	VSS	Negative Power Supply. Nominal -5 Volts.
2	XTALO	Crystal Oscillator Output.
3	XTALI	Crystal Oscillator Input.
4	CK OUT	Sampling Clock Output. (Open Drain)
5	$\overline{RE}$	Recall Enable Input. Loads Configuration into Control Registers from On-Chip E²PROM.
6	AOUT	PG-B Analog Signal Output.
7	CK SEL	Clock Select. Selects one of the 3 recommended Clock frequencies.
8	AIN	PG-B Analog Signal Input.
9	VDD	Positive Power Supply. Nominal +5 Volts.
10	EOUT	Delay Equalizer Analog Signal Output.
11	AGND	Analog Ground.
12	EIN	Delay Equalizer Analog Signal Input.
13	DGND	Digital Ground.
14	$\overline{CS}$	Chip Select Control Input.
15	$\overline{WE}$	Write Enable Control Input.
16	DIN	Serial Data Input.

Block Diagram



Device Operation

The AT76C10E is designed for use in the signal paths of a modem or voice/data phone to minimize the bit-error-rate over dial-up and leased lines. Gain and Group Delay response of the AT76C10E are controlled by a serial seven-bit configuration code. D1 and D0 of the configuration code are the address bits which select one of the three control registers. Bits D2 to D5 set the gain and delay equalizer steps. D6 is an option bit which determines whether the configuration code will update one of the control registers only, or also be stored in on-chip non-volatile memory (E^2PROM) of the AT76C10E. All the functions associated with the configuration code are summarized in Tables 1 to 4.

Configuration Code Format

D6	D5	D4	D3	D2	D1	D0
Option Select	Control Code				Address	

This chip can be used as part of an adaptive equalizer for medium to high speed modems (1200 bps to greater than 19.2K bps). The configuration code is loaded into the chip at a serial data input port and updated in real time. It can also be stored permanently in on-chip E^2PROMS and updated periodically. The high performance Atmel E^2PROM process together with redundancy circuits allows over 10E6 write cycles. The amplitude response of the equalizer is nominally at 0 dB with negligible ripple. The AT76C10E can also be used as a fixed compromise delay equalizer.

PROGRAMMABLE GAIN AMPLIFIER: The AT76C10E provides two high dynamic range amplifiers for maximizing signal-to-noise ratio. Amplifier PG-A offers 16 programmable gain steps from 0 dB to 7.5 dB in 0.5 dB steps. Amplifier PG-B provides -8 to 16 dB of gain in 8 dB steps. The two amplifiers can be cascaded to provide 31.5 dB range of programmable gain in 0.5 dB steps. The Programmable Amplifiers can be used as an Automatic Gain Control Circuit or as a fixed gain adjustment.

PROGRAMMABLE GROUP DELAY EQUALIZER: The Group Delay Equalizer is designed to provide programmable compromise group delay compensation to achieve low bit-error-rate data transmission. Four group delay responses are provided to accommodate the majority of conditioned as well as unconditioned lines. The first three responses are recommended for line types C2 and C1, while the fourth response can be used for 3002-type lines. Two or more AT76C10Es can be cascaded to obtain additional group delay compensation.

CONTROL REGISTERS: Four control registers are used to store the configuration codes for the gain steps of PG-A and PG-B, the delay steps of the Delay Equalizer, and the control bit for the power-down mode. All the control bits, except the power down-bit, can also be programmed into on-chip non-volatile memories of the AT76C10E.

MICROCOMPUTER INTERFACE: Control inputs $\overline{CS}$, $\overline{WE}$, $\overline{RE}$ and serial data input DIN allow the AT76C10E to be easily interfaced with most popular microcontrollers. All digital I/Os are TTL as well as CMOS compatible. For stand alone operation, $\overline{CS}$ should be tied to VDD while $\overline{WE}$, $\overline{RE}$ and DIN should be tied to ground.

WRITE OPERATION: To program a configuration code into a particular control register, the voltage at $\overline{CS}$ has to be brought low while the data bits appearing at DIN are strobed in at the rising edge of $\overline{WE}$. At the rising edge of $\overline{CS}$, the last 7 input data bits are latched into the control registers. Therefore, if the first bit of an update byte is a "start bit," it will be ignored. If a "0" was inserted at D6 of the input code, the configuration code will also be immediately written into on-chip E^2PROM of the AT76C10E. As all timing signals and programming voltages are generated internally, writing the E^2PROM is transparent to the user. However, while the E^2PROM is being programmed, which takes 1.5 mS, any further attempt to initiate programming will be ignored until the first operation is completed.

RECALL OPERATION: A RECALL operation can be initiated any time during operation by bringing both $\overline{CS}$ and $\overline{RE}$ low simultaneously. The configuration codes which have been preprogrammed in the E^2PROM of the AT76C10E are loaded into the control registers.

POWER-DOWN MODE: To minimize power consumption for battery powered applications and in certain linecard applications, the AT76C10E provides a low power standby mode of operation. In the power-down mode, the analog outputs go into a high impedance state. The power-down mode is initiated by writing a "0" into the power-down register. Once in the power-down mode, the AT76C10E can be reactivated by writing a "1" into the power-down register or performing a RECALL operation. It should be noted that upon powering up the AT76C10E for the first time, it automatically goes into the normal active mode of operation.

CRYSTAL OSCILLATOR: Internal timing of the chip is generated either by connecting a crystal across pins XTALI and XTALO of the on-chip oscillator, or by applying an external clock at pin XTALI. In the latter case, pin XTALO should be left unconnected. To accommodate different applications, three clock options: 2.4576 MHz, 3.6864 MHz and 11.0592 MHz, can be selected via control pin CK SEL. For applications in a linecard environment, a 2.56 MHz clock can be used instead of the 2.4576 MHz clock. The 153.6 kHz (160 kHz with 2.56 MHz clock) sampling clock is available as an open drain output at CK OUT for synchronization or driving other circuits, e.g. the transmit or receive filters, or A/D and D/A converters.

CK SEL	Recommended XTAL Frequency	CK OUT
VDD	11.0592 MHz	153.6 kHz
DGND	3.6864 MHz	153.6 kHz
VSS	2.4576 MHz	153.6 kHz
VSS	2.56 MHz	160.0 kHz

Group Delay Characteristics (Microseconds)

Fs = 153.6 kHz

Frequency (Hz)	Step #1	Step #2	Step #3	Step #4
300	158	278	416	284
600	188	336	502	386
900	237	463	681	680
1200	325	671	985	1360
1500	431	890	1330	1791
1700	462	938	1382	1838
1900	435	897	1305	1810
2100	372	777	1144	1510
2400	266	542	808	683
2700	181	361	534	342
3000	136	250	368	213
3300	102	182	267	148

Table 1. Option Selection

Address D1	Address D0	Option Bit D6	Function
0	0	0	Writes Control Code into
0	1	0	E^2PROM and updates
1	0	0	Control Registers
0	0	1	
0	1	1	Updates Control
1	0	1	Registers Only
1	1	0	Power Down Mode
1	1	1	Active Mode

Table 2. Equalizer Selection

Address D1	Address D0	Control Code D5	D4	D3	D2	Equalizer Step No.	Recommened Line Condition
0	0	X	X	0	0	1	C2
0	0	X	X	0	1	2	C1
0	0	X	X	1	0	3	C1
0	0	X	X	1	1	4	3002

Table 3. Programmable Gain Amplifier, PG-A

Address D1	Address D0	Control Code D5	D4	D3	D2	PG-A Step No.	PG-A Gain (dB)
0	1	0	0	0	0	1	0.0
0	1	0	0	0	1	2	0.5
0	1	0	0	1	0	3	1.0
0	1	0	0	1	1	4	1.5
0	1	0	1	0	0	5	2.0
0	1	0	1	0	1	6	2.5
0	1	0	1	1	0	7	3.0
0	1	0	1	1	1	8	3.5
0	1	1	0	0	0	9	4.0
0	1	1	0	0	1	10	4.5
0	1	1	0	1	0	11	5.0
0	1	1	0	1	1	12	5.5
0	1	1	1	0	0	13	6.0
0	1	1	1	0	1	14	6.5
0	1	1	1	1	0	15	7.0
0	1	1	1	1	1	16	7.5

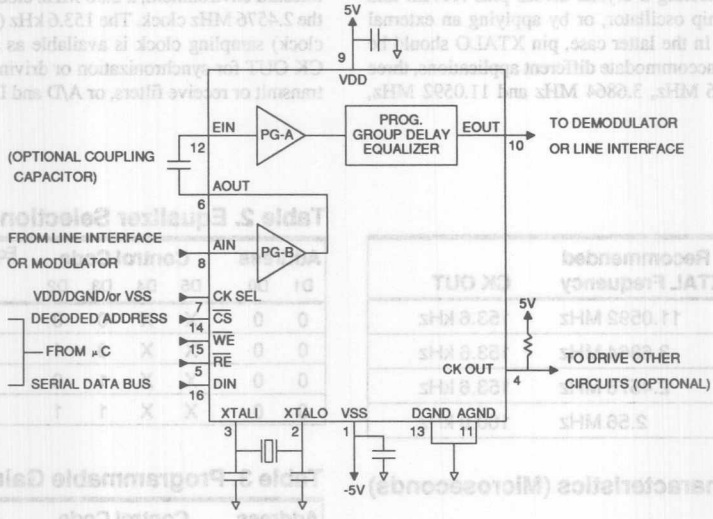
Table 4. Programmable Gain Amplifier, PG-B

Address D1	Address D0	Control Code D5	D4	D3	D2	PG-B Step No.	PG-B Gain (dB)
1	0	X	X	0	0	1	0.0
1	0	X	X	0	1	2	8.0
1	0	X	X	1	0	3	16.0
1	0	X	X	1	1	4	-8.0

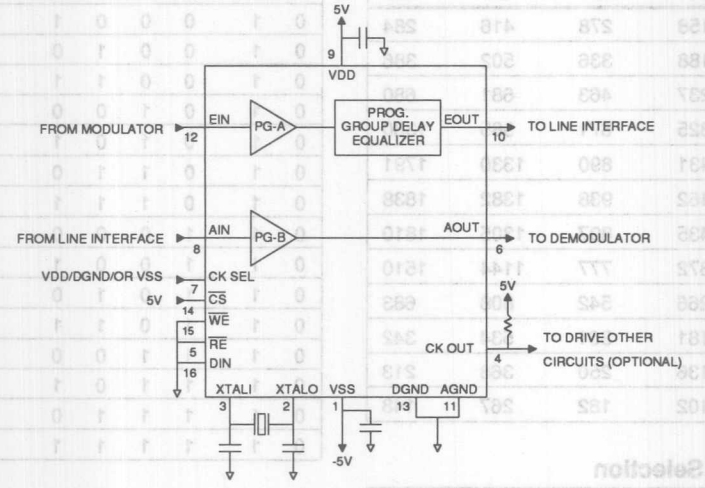
X = Don't Care

11

Sample Connection for Typical Application



Stand Alone Operation Example



Absolute Maximum Ratings*

Temperature Under Bias	-55° C to 125° C
Storage Temperature	-65° C to 150° C
Voltage on Pins AGND and DGND with Respect to VSS	-0.6 V to 6.25 V
All Voltages with Respect to VSS	-0.6 V to VDD + 0.6 V

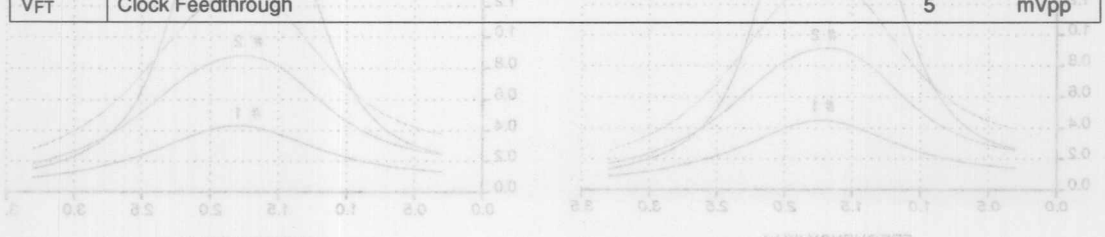
*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

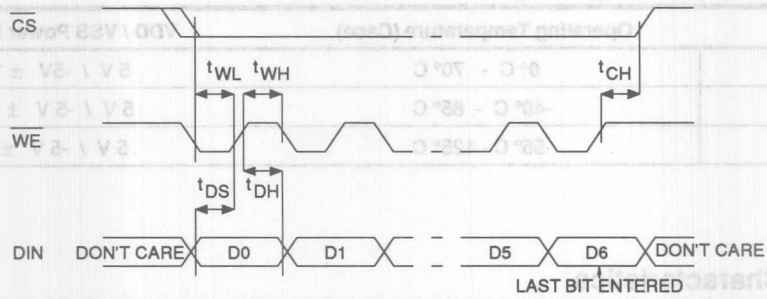
D.C. and A.C. Operating Range

	Operating Temperature (Case)	VDD / VSS Power Supplies
Commercial	0° C - 70° C	5 V / -5V ± 10%
Industrial	-40° C - 85° C	5 V / -5 V ± 10%
Military	-55° C - 125° C	5 V / -5 V ± 5%

Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DDO}	VDD Quiescent Current (active mode)			3	6	mA
I_{SSO}	VSS Quiescent Current (active mode)			3	6	mA
I_{DDP}	VDD Quiescent Current (power-down mode)			100	500	µA
I_{SSP}	VSS Quiescent Current (power-down mode)			100	500	µA
R_{IA}	Input Resistance at AIN		100			kohm
R_{IE}	Input Resistance at EOUT	F_S=153.6 KHz	1			Mohm
C_I	Input Capacitance				20	pF
ROA	Ouput Resistance at AOUT				1	kohm
ROE	Ouput Resistance at EOUT				200	ohm
F_O	Center Frequency			1700		Hz
DT	Group Delay Tolerance		-1.5		+1.5	%
GT	Gain Tolerance		-0.05		0.05	dB
G_O	Insertion Loss		-0.15		0.15	dB
V_O	Output Voltage	RL = 20 kohm	VSS		VDD	V
V_N	Output Noise	BW = F_S/2			200	µVrms
THD	Total Harmonic Distortion	RL = 20 kohm V_O = 8 Vpp		0.1	0.5	%
F_S	Sampling Frequency			153.6		kHz
V_{FT}	Clock Feedthrough				5	mVpp

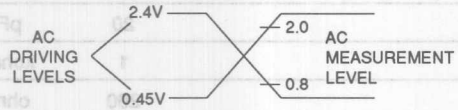




Digital Timing Parameters

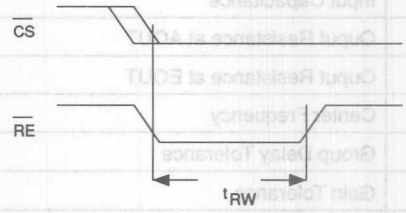
Symbol	Parameter	Min	Max	Units
t_{WL}	Write Enable Low	50		ns
t_{WH}	Write Enable High	50		ns
t_{CH}	$\overline{CS}$ Hold Time	100		ns
t_{DS}	Data Setup Time	40		ns
t_{DH}	Data Hold Time	40		ns

Input Test Waveform

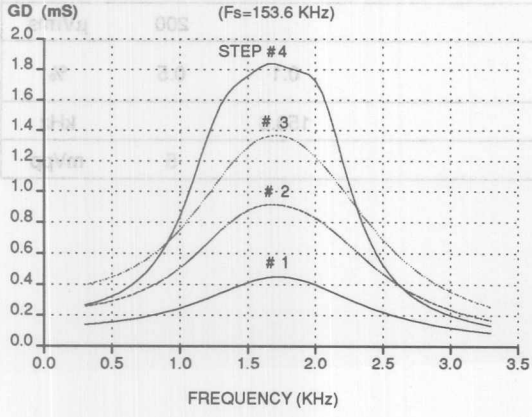


t_R, t_F < 20 ns (10% to 90%)

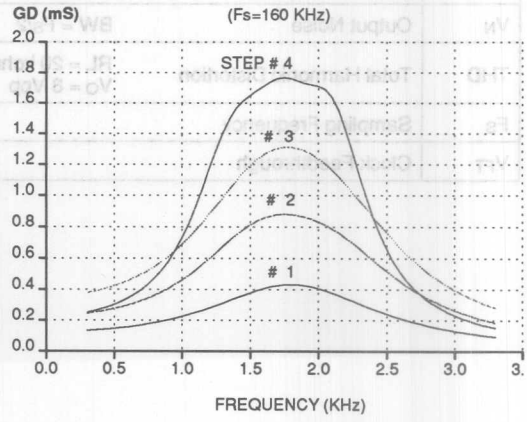
Configuration Code Recall Waveform



Typical Group Delay Response



Typical Group Delay Response



Ordering Information

Delay (ms)	Gain (dB)	Power Supply	Bandwidth (KHz)	Ordering Code	Package	Operation Range
1.8	31.5	±10%	4	AT76C10E-PC AT76C10E-SC	16P3 16S	Commercial (0°C to 70°C)
				AT76C10E-PI AT76C10E-SI	16P3 16S	Industrial (-40°C to 85°C)
1.8	31.5	±5%	4	AT76C10E-DM	16D3	Military (-55°C to 125°C)

11

Package Type	
16D3	16 Lead, 0.300" Wide Non-Windowed, Ceramic Dual Inline Package (Cerdip)
16P3	16 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
16S	16 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)

Delay (ms)	Gain (dB)	Power Supply	Bandwidth (GHz)	Ordering Code	Package	Operation Range
1.8	31.5	±10%	4	ATT6C106E-PC ATT6C106E-SC	16P3 16S	Commercial (0°C to 70°C)
				ATT6C106E-PI ATT6C106E-SI	16P3 16S	Industrial (-40°C to 85°C)
1.8	31.5	±5%	4	ATT6C106E-DM	16D3	Military (-55°C to 125°C)

Package Type	
16D3	16 Lead, 0.300" Wide Non-Windowed, Ceramic Dual Inline Package (Cerdip)
16P3	16 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
16S	16 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)

Features

- **Monolithic Dual-Channel 16/18-Bit A/D Converters**
  - **On-Chip Sample/Hold**
  - **Automatic Linearity Error Correction**
- **High Conversion Rates to 96K Samples Per Second at 18 Bits for Each Channel**
- **Capable of Single or Continuous Conversions**
- **Operates from a Single 5 V ± 10% Supply**
- **High Signal-to-Noise Ratio: 90 dB**
- **Single Multiplexed Serial Data Output**
- **High Reliability CMOS Technology**
- **Full Military, Commercial and Industrial Temperature Ranges**

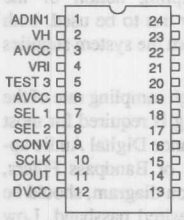
CMOS Dual-Channel 16/18-Bit A/D Converters

Description

The AT76C120 provides two complete Analog-to-Digital (A/D) Converters integrated on a monolithic substrate. It is designed for Digital Audio and Signal Processing applications as well as Industrial Control and Datacommunication. The Sample/Hold function is incorporated in both A/D channels. Each channel can independently perform 96K 18-Bit conversions per second. The AT76C120 needs a minimum of external components and provides a simple and cost effective solution for applications requiring high resolution A/D conversion.

The AT76C120 is fabricated in a state-of-the-art, low power CMOS process and operates from a single 5 V supply. A modified successive approximation algorithm is used to optimize conversion speed. The AT76C120 can perform a single conversion at random or continuous conversions. Linearity errors caused by tap weight variations are automatically compensated by adding a correction factor to each A/D conversion result. The optimum correction factors are factory programmed into each individual chip. The digital output code is presented serially, in 2's complement format.

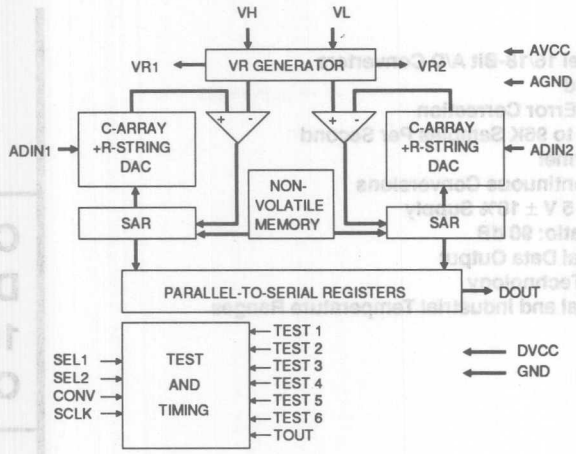
Pin Configuration



Pin Name	Function
AGND, GND	Analog Ground, Ground
ADIN1	Analog Input for Channel-1
ADIN2	Analog Input for Channel-2
AVCC	+5 V Analog Supply Input
DOUT	Digital Data Output
DVCC	+5 V Digital Supply Input
CONV	Convert Clock Input
SCLK	System Clock Input
SEL1	DOUT Mode Select Input
SEL2	16/18-Bit Mode Select Input
TEST 1,2,3,4,5,6	Test Inputs
TOUT	Test I/O
V_H,V_L	Reference Voltage Inputs
VR1,VR2	Channel-1,-2 Reference Voltage Outputs

11

Block Diagram



Device Operation

Each analog input to the AT76C120 is sampled and held simultaneously once every CONV clock period. As shown in the block diagram, the AT76C120 uses a combination of binary ratioed double-polysilicon Capacitor Arrays and Resistor String networks to generate the analog decision levels (or tap weights). The Capacitor Arrays also provide the internal Sample-and-Hold function. A high-gain auto-zeroed Comparator is used to compare an analog input with the decision levels. The Vr Generator supplies internal reference voltages equal to (VH + VL)/2 used by the comparators.

A/D conversion is accomplished through 18-bit Successive Approximation Registers (SARs). An improved successive approximation scheme is used to optimize conversion speed. The A/D output codes are stored in Parallel-to-Serial Shift Registers and are available at a single multiplexed serial data output port.

System Clock input, SCLK, provides the internal timing reference and the Convert Clock, input CONV, initiates an A/D conversion. The Test and Timing circuits shown in the block diagram generate all the timing control signals from SCLK and CONV for sample-and-hold, A/D conversion and tap weight error correction during normal operation as well as tap weight error calibration at the factory.

A minimum of 64 SCLK clock cycles are required for one A/D conversion. The maximum SCLK clock frequency is 6.144 MHz. The minimum 18-bit conversion time for each channel is 10.4 µs, which corresponds to a maximum conversion rate of 96 kHz, making 2X sampling in Digital Audio applications possible.

To minimize overall system cost while achieving high resolution, the AT76C120 compensates for linearity errors caused by tap weight variations by adding a correction factor to each A/D conversion result. This operation is done automatically without the intervention of the host processsor. The optimum correction factors are factory programmed into on-chip nonvolatile storage.

The AT76C120 requires only a single 5-volt supply for operation.

System Implementation Considerations

POWER SUPPLY DECOUPLING AND GROUNDING: To obtain the highest performance possible with the AT76C120, critical signal paths, power supply lines and ground planes on the circuit board should be laid out carefully to minimize noise coupling or aliasing into sensitive analog paths. As illustrated in the diagram showing a Sample Connection for Typical Application, a separate AVCC line decoupled to AGND with a tantalum capacitor in parallel with a smaller ceramic chip capacitor should be used for the analog circuits on the AT76C120. Similarly, a separate analog ground return, AGND, which is connected to the most quiet point in the system ground plane, should be used.

For best results, four layer PC boards with separate ground and power supply planes are recommended. The AGND plane should be laid out as an island or tub underneath pins 1 to 6 and pins 19 to 24.

High frequency noise on the power and ground lines can be aliased into the passband by the sampling action of the AT76C120. If a switching power supply has to be used, both AVCC and AGND need to be isolated from the system supplies with inductors of appropriate values.

ANALOG INTERFACE: Due to the high sampling rate of the AT76C120, little if any anti-alias filtering is required for most industrial applications. For high performance Digital Audio applications, external Anti-Alias Lowpass or Bandpass Filters, shown as AAFs' in the Sample Connection diagram, should be used to eliminate signals outside the desired passband. Low noise op amps with low output impedances should also be used to supply the analog inputs.

The A/D full-scale range is determined by the voltage applied across pins VH and VL, i.e. (VH - VL). VL is normally connected to the analog ground, AGND, while VH should be supplied by a stable voltage reference.

The internal reference voltage appearing at output pins VR1 and VR2 is nominally (VH + VL)/2.

If the voltage of the input signal can swing below ground, it is necessary to apply an offset to the input to make the AC ground correspond to the mid point of the full scale range, (VH + VL)/2. Outputs VR1 and VR2 provide the AC ground reference as shown in the diagram for Sample Connection.

SYSTEM TIMING: Internal and output data timing of the AT76C120 are synchronized with the system clock, SCLK. To avoid possible synchronization and aliasing problems, deriving the convert clock, CONV, by dividing SCLK by 64 is recommended.

The AT76C120 samples both analog inputs, ADIN1 and ADIN2, once every CONV period. Both inputs are sampled simultaneously, i.e. in-phase. The AT76C120 then performs an A/D conversin on both samples and returns the two resulting 18-bit codes at the serial data output pin, DOUT, during the following CONV clock period.

The convert clock, CONV, is used inside the AT76C120 to initiate sample-and-hold and can also be used by the host processor to latch in the serial 16-bit or 18-bit wide output data.

DIGITAL INTERFACE: The AT76C120 uses a single multiplexed serial data output pin, DOUT. CH-1 and CH-2 data bits are synchronized with SCLK and are available during either the "High" or the "Low" period of convert clock, CONV. A logic "1" at DOUT Mode Select, SEL1, results in the AT76C120 returning the A/D output of CH-1 during the CONV "Low" period, and CH-2 output during the CONV "High" period. A logic "0" at SEL1 results in CH-1 output during the CONV "High" period and CH-2 output during the CONV "Low" period.

The convert clock, CONV, if equal to SCLK divided by 64, makes a transition from "High" to "Low" or vice versa after the LSB is shifted out of DOUT. This allows the serial data to be easily latched into most popular D/A converters or digital signal processors by using CONV rising or falling edges. To further enhance digital interface compatibility, DOUT Mode Select Input, SEL1, allows the user to choose either CONV transitions for both channels.

The AT76C120 allows the user to choose either 16-bit wide or 18- bit wide A/D outputs in 2's complement format. A logic "1" at 16/18 Mode Select Input, SEL2, returns two 18-bit codes at DOUT, while a logic "0" results in 16-bit output codes at CONV rising or falling edges as shown in Input/Output Timing diagram.

In Digital Audio and many signal processing applications, the A/D outputs are further processed by a digital filter. The 18-bit output mode provides better dynamic range and resolution than 16- bit outputs. However, for applications with a 8-bit or 16-bit host microprocessor, 16-bit wide data are more convenient to manage.

SINGLE CONVERSION MODE: When using the AT76C120 in a single conversion mode, please note that the first 15 SCLK periods in each CONV cycle is used for internal sample-and-hold for both channels CH-1 and CH-2. Since the AT76C120 returns the digital conversion results in a subsequent CONV cycle, two CONV periods are in general required to perform a random A/D conversion.

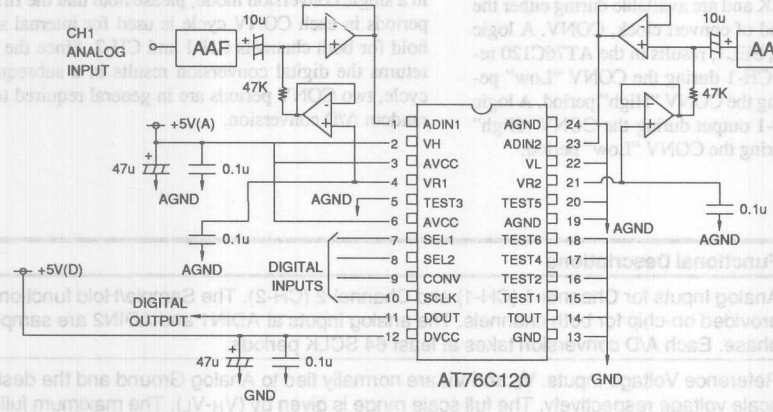
Pin Definitions

	Symbol	Functional Descriptions
Analog Interface	ADIN1 ADIN2	Analog Inputs for Channel-1 (CH-1) and Channel-2 (CH-2). The Sample/Hold function is provided on-chip for both channels. The analog inputs at ADIN1 and ADIN2 are sampled in-phase. Each A/D conversion takes at least 64 SCLK periods.
	V_L V_H	Reference Voltage Inputs. V_L and V_H are normally tied to Analog Ground and the desired full-scale voltage respectively. The full scale range is given by (V_H-V_L). The maximum full-scale voltage can be as high as AVCC.
	VR1 VR2	Reference Voltage Outputs for CH-1 and CH-2. The nominal value at these pins is (V_H+V_L)/2.
Digital Interface	CONV	Convert Clock Input. CONV is normally obtained by dividing the system clock SCLK by 64. The internal Sample/Hold pulse and A/D data output are synchronized with CONV.
	DOUT	Serial Digital Output. DOUT returns two 18-bit serial outputs for CH-1 and CH-2 in 2's complement format. The output data bits are synchronized with SCLK. Please refer to DOUT Timing Diagram for detailed timing relationship with CONV and SCLK.
	SCLK	System Clock Input. The maximum frequency for 18-bit operation is 6.144 MHz. This corresponds to a minimum conversion time of 10.4 µs.
	SEL1	DOUT Mode Select Input. i) SEL1 = "1", CH-1 data output during CONV "Low" CH-2 data output during CONV "High" ii) SEL1 = "0", CH-1 data output during CONV "High" CH-2 data output during CONV "Low"
	SEL2	16/18-Bit Mode Select. i) SEL2 = "1" selects 18-bit A/D mode, ii) SEL2 = "0" selects 16-bit A/D mode.

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	Symbol	Functional Descriptions
Test Interface	TEST1 TEST2 TEST3 TEST4 TEST5 TEST6	Test Inputs. Normally tied to Ground for TEST 1, 2, 4, 6 and to AGND for TEST 3, 5. These inputs are used for testing and calibration at the factory and are not required for normal A/D operations.
	TOUT	Test I/O. Normally tied to Ground. Like the Test Input pins, this pin is not used for normal A/D operations.
Power Supply	AVCC	Analog Power Input. Nominal 5 Volts. AVCC should be connected to a filtered system supply and kept separate from the Digital Supply.
	DVCC	Digital Power Input. Nominal 5 Volts.
	AGND	Analog Ground. AGND should be kept separate from the digital Ground.
	GND	Digital Ground.

Sample Connection for Typical Application



Notes: 1. AVCC, AGND, +5V (A)— analog supply
2. DVCC, GND, +5V (D)— digital supply
3. Use high quality 0.1-µF ceramic chip capacitors.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to 125°C
Storage Temperature	-65°C to 150°C
Voltage on Any Pin with Respect to AGND and GND	-2.0 V to 7.0 V(1)
Power Dissipation	1 W
Reference Current	10 mA
Analog Input Current	10 mA
DC Digital Output Current	25 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
1. Minimum voltage is -0.6 V DC which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is AVCC/DVCC+0.75 V DC which may overshoot to 7.0 V for pulses of less than 20 ns.

D.C. and A.C. Operating Range

		AT76C120-1	AT76C120-2	AVCC/DVCC Power Supplies
Operating Temperature Range(Case)	Com.	0° C - 70° C	0° C - 70° C	5 V ± 10%
	Ind.	-40° C - 85° C	-40° C - 85° C	5 V ± 10%
	Mil.	-55° C -125° C	-55° C -125° C	5 V ± 5%

D.C. Characteristics

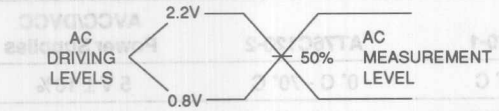
Symbol	Parameter	Conditions	Min	Max	Units
I_{LI}	Digital Input Load Current	V_{IN} = -0.1 V to DVCC+0.1 V		10	µA
I_{LO}	Digital Output Leakage Current	V_{OUT} = -0.1 V to DVCC+0.1 V		10	µA
I_{CCD}	Digital Supply Current			40	mA
I_{CCA}	Analog Supply Current			10	mA
I_{REF}	Reference Input Current			5	mA
V_{IL}	Digital Input Low Voltage		-0.5	0.8	V
V_{IH}	Digital Input High Voltage		2.2	DVCC+0.5	V
V_{OL}	Digital Output Low Voltage	IO = 5 mA		0.4	V
V_{OH}	Digital Output High Voltage	IO = -5 mA	2.4		V
V_{AIN}	Analog Input Voltage		V_L	V_H	V
V_H	Analog Input Voltage at V_H Pin		AVCC-0.5	AVCC	V
V_L	Analog Input Voltage at V_L Pin		0.0	0.5	V

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Analog Characteristics (AVCC = DVCC = 5 V, Ta = 25° C)

Symbol	Parameter	Conditions	AT76C120-1 Min	AT76C120-1 Typ	AT76C120-1 Max	AT76C120-2 Min	AT76C120-2 Typ	AT76C120-2 Max	Units
RES	A/D Resolution			18			18		bits
ILE	Integral Linearity Error				±0.006			±0.01	% FSR
Fs	A/D Sampling Frequency	18-Bit Mode			96			96	kHz
FSE	Full Scale Error				±0.15			±0.15	% FSR
THD	Total Harmonic Distortion	0dB, 1kHz Input			0.01			0.02	%
		-20dB, 1kHz Input			0.02			0.04	%
		-60dB, 1kHz Input			2			4	%
S/N	Signal-to-Noise Ratio				90			84	dB

Input Test Waveforms



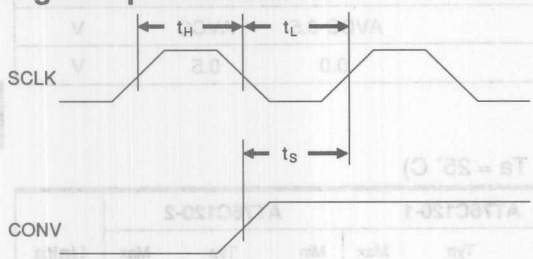
Notes: 1. tR, tF < 30 ns (10% to 90%)
2. Input timing reference is at 1.5 V

Digital Output Codes vs. Analog Inputs

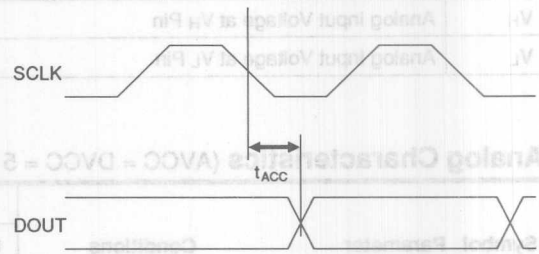
Analog Input	Digital Output Codes MSB...																	...LSB
V_H	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
V_H - 1 LSB(1)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
.																		
.																		
$(V_H + V_L) / 2 + 1$ LSB	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
$(V_H + V_L) / 2$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$(V_H + V_L) / 2 - 1$ LSB	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
.																		
.																		
$V_L + 1$ LSB	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
V_L	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note: 1. 1 LSB = $(V_H-V_L)/262, 144$ in 18-bit mode.

Digital Input Waveforms



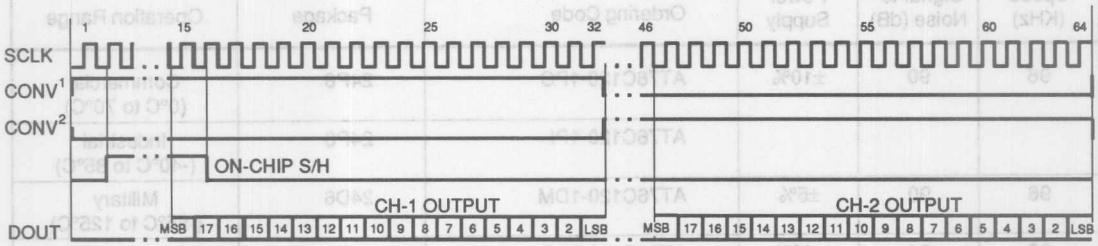
Digital Output Timing Waveforms



Digital Timing Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
t_R	Input Rise Time			30	ns
t_F	Input Fall Time			30	ns
t_H	SCLK High Width		50		ns
t_L	SCLK Low Width		50		ns
t_S	CONV Setup Time		40		ns
t_{ACC}	DOUT Access Time	C_{LOAD} = 30 pF		50	ns
T_{CONV}	CONV Period		10.4		µs
T_{SCLK}	SCLK Period		162		ns

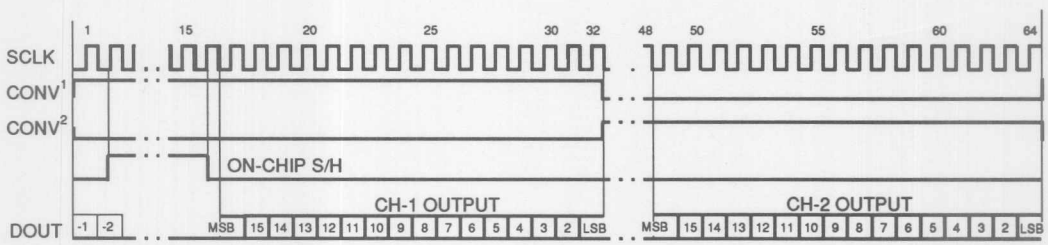
Input/Output Timing for 18-Bit Mode (SEL2 = "1")



i) SEL1 = "0", CONV 1
ii) SEL1 = "1", CONV 2

Notes: CONV = Fs (96 kHz Max)
SCLK = CONV x 64

Input/Output Timing for 16-Bit Mode (SEL2 = "0")



i) SEL1 = "0", CONV 1
ii) SEL1 = "1", CONV 2

Notes: CONV = Fs (96 kHz Max)
SCLK = CONV x 64

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Ordering Information

Speed (KHz)	Signal-to-Noise (dB)	Power Supply	Ordering Code	Package	Operation Range
96	90	±10%	AT76C120-1PC	24P6	Commercial (0°C to 70°C)
			AT76C120-1PI	24P6	Industrial (-40°C to 85°C)
96	90	±5%	AT76C120-1DM	24D6	Military (-55°C to 125°C)
96	84	±10%	AT76C120-2PC AT76C120-2RC	24P6 24R	Commercial (0°C to 70°C)
			AT76C120-2PI AT76C120-2RI	24P6 24R	Industrial (-40°C to 85°C)
96	84	±5%	AT76C120-2DM	24D6	Military (-55°C to 125°C)

Package Type	
24D6	24 Lead, 0.600" Wide, Non-Windowed (OTP), Ceramic Dual Inline Package (Cerdip)
24P6	24 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
24R	24 Lead, 0.330" Wide, Plastic Gull Wing Small Outline (SOIC)

Features

- Dual-Channel 16/18-bit A/D Converter
- Expandable to 16 Channels
- Conversion Frequency up to 96 kHz Both Channels
- Programmable Gain and Offset Control
- Precision Voltage Reference
- Programmable Low-Pass Filter
- Wide Input Range from 0 V to 226 V
- Serial Digital Output
- Embedded Microcontroller
- 128-Kbyte Internal RAM Expandable to 512 Kbyte
- PC Bus or RS-232 Operation
- DOS and Windows 3.X Software Package
- Special Wire Wrap Area for Prototyping

AD-120 Analog Interface System

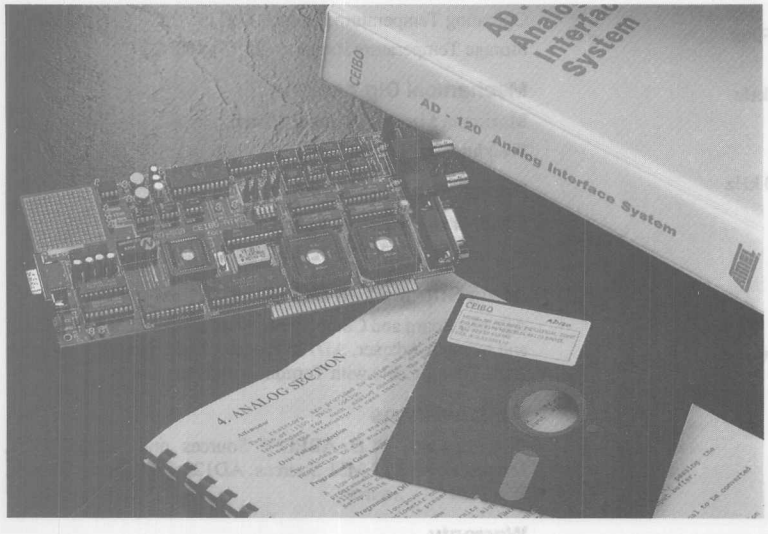
Description

Atmel's AD-120 Analog Interface System is a high-performance development tool dedicated to Atmel's high resolution AT76C120 A/D converter. It provides an easy-to-use instrument which reduces the evaluation, learning, development, and debugging cycle, and enables the development engineer to solve hardware and software problems quickly and efficiently.

AD-120 operates with an IBM PC/XT/AT or compatible personal computer and carries out a set of functions selected by an embedded microcontroller. The system may be plugged into a PC slot or operated as a stand-alone unit controlled through an RS-232 link.

The system provides the control lines to expand the analog inputs up to 16 channels by means of an external multiplexer.

AD-120 is a complete package of software and hardware components. Most of the parts are standard items supplied with every system. Software sources, PLD formulas, and PCB layouts are available upon request and are optional items.



Applications

- Evaluation of the AT76C120 A/D Converter
- Hardware and Software Implementations
- Prototyping Unit
- Process Control
- OEM Analog-to-Digital System
- Data Logging and Signal Analysis

Specifications

Analog Inputs

Channels: 2 Single-Ended
Input Ranges: 0 V to ± 226 V
Coding: Two's Complement and True Binary
Input Current: 1.5 µA maximum at 25°C
Trigger Source: Software Command or External Signal

A/D Converter

A/D Converter Type: Atmel's AT76C120
Resolution: 16 or 18 Bits
Conversion Time: 10.4 µs min.
Channel Crosstalk: 90 dB at 1 kHz
Linearity: ±0.15%
Signal-to-Noise Ratio: 90 dB at 1 kHz

Reference

Reference Voltage: 5 V ± 20 mV
Temperature Drift: 25 ppm/°C
Maximum Noise: 4 µV

Filter

Type: Second Order Butterworth LP Filter
DC Low Pass Gain: ±0.2 dB
Clock Deviation Ratio: ±1.5% at 250 kHz
Q Error: ±6% maximum
Q Factor: 0.74
Cutoff Frequency: 1.875 Hz to 30.720 kHz

Gain Amplifier

Gain: x1 to x20.8 in Steps of 0.2
Amplifiers: One for Each Channel

Offset Control

Offset: 0 V to 5 V in Steps of 0.0505 V
Controls: One for Each Channel

Attenuator

Attenuation: 1:1 or 1:101
Controls: One for Each Channel

Digital Output

Serial Output: Bit Stream

DOS Software

Source Language: QuickBasic
Command Set: Acquisition, Setup, View, Files, Quit
Acquisition Menu: Start, Stop, Do Forever
Setup Menu: Cutoff Frequency, Gain, Resolution, etc.
View Menu: All, Range, First, Last, Graphics
Files: Save, Filename

Windows 3.X Software

Source Language: C++
Command Set: Acquisition, Setup, View, Files, Help
Acquisition Menu: Start, Stop, Do Forever
Setup Menu: Cutoff Frequency, Gain, Resolution, etc.
View Menu: Table, Graphics Info.
Files: Load, Save

Microcontroller Software

Source Language: PLM51
Procedures: Initialization, Communications, Output, Process

Host Characteristics

AD120 Program: IBM PC/XT/AT or compatible, 256 Kbyte of RAM, one floppy disk drive, one optional RS-232 interface board if used as a remote host, PC-DOS 2.0 or later

WAD120 Program: IBM PC/XT/AT or compatible, One Mbyte of RAM, one hard disk, VGA color display, Microsoft Windows 3.0 or later, DOS 5.0 or later, one optional RS-232 interface board if used as a remote host

Environment

Operating Temperature Range: 0°C to 70°C
Storage Temperature Range: -25°C to 85°C

Mechanical Dimensions

Maximum Size: 120 mm x 20 mm
Weight: 265 grams

Power Requirements

Stand-Alone Mode: 5 VDC/1.5 A
PC Mode: 5 VDC/1.5 A, 12 V/50 mA

Items Supplied as Standard

AD-120 Board and Components, User's Manual, RS-232 Cable and nine-pin Adapter, AD120 Program Disk, WAD120 Program Disk, Power Cable with Terminals and Package

Optional Items

PCB Layouts, PLD ABEL™ Sources and JEDEC Files, Microcontroller PLM51 Sources, AD120 QuickBasic Sources, WAS120 C++ Sources

Warranty

Six months limited warranty, parts and labor

Ordering Information

Speed (KHz)	Signal-to-Noise (dB)	Power Supply	Ordering Code	Operation Range
96	84	±10%	AD-120	Commercial (0°C to 70°C)

Ordering Information

Speed (KHz)	Signal-to-Noise (dB)	Power Supply	Ordering Code	Operation Range
96	84	±10%	AD-120	Commercial (0°C to 70°C)

Features

- Personal System/2* and VGA* Compatible
- Pixel Rates to 66 MHz
- Triple 6-Bit DACs Display 256K Possible Colors
- Pixel Word Mask and Composite Blank on All Three Channels
- 18-Bit Wide Color Palette Stores 256 Colors
- RGB Video Outputs Drive 37.5 Ohm Loads Directly
- Low Power, Low Glitch Operation
- Asynchronous MPU Read/Write to All Internal Registers
- Available in Standard 28-Pin DIP and 32-Pin LCC
- Full Military, Commercial and Industrial Temperature Ranges

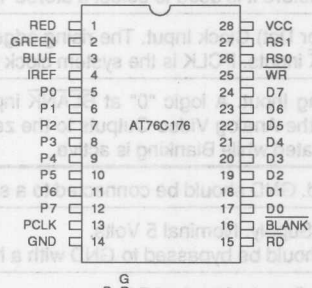
CMOS
Triple Video DAC
Color Palette

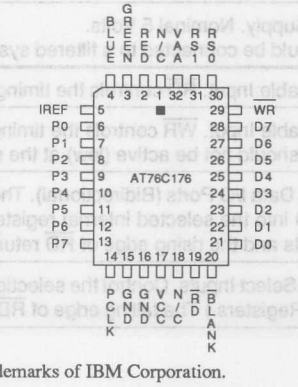
Description

The AT76C176 is a second generation color palette DAC which provides direct drives for RGB color displays. The AT76C176 integrates three high performance SIX-bit video DACs (Digital-to-Analog Converters), an advanced 256 x 18 Color Palette (Color Look-up Table) and a versatile microprocessor interface on a monolithic substrate.

The AT76C176 supports the RS170 video standard and graphics controllers compatible with the VGA standard. This device allows 256 colors to be displayed out of a total of 262,144 colors. The AT76C176 provides composite blank outputs on all three channels. Additional advanced features include on-chip pixel mask logic which allows displayed colors to be modified in a single write cycle rather than by altering the contents of the color palette.

Pin Configurations



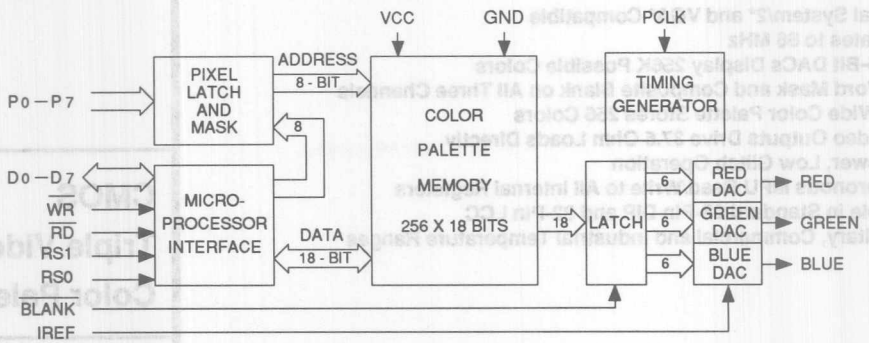


Pin Name	Function
RED GREEN BLUE	Analog Video Outputs for R,G,B Guns
IREF	Reference Current Input
P0-P7	Pixel Address Inputs
PCLK	Pixel Clock Input
GND	Ground
$\overline{RD}$	Read Enable Input
$\overline{BLANK}$	Video Blanking Input
D0-D7	Program Data I/O
$\overline{WR}$	Write Enable Input
RS0,RS1	Register Select Inputs
VCC	+5 Volts Supply Input
VAA	+5 Volts Analog Supply Input
N/C	No Connect

* Personal System/2 and VGA are registered trademarks of IBM Corporation.

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Block Diagram



Pin Definitions

	Symbol	Functional Descriptions
Video Interface	RED GREEN BLUE	Analog Video Outputs. These are the outputs of the triple video DACs. The 18-bit wide color palette output and the $\overline{\text{BLANK}}$ input drive the DAC inputs.
	IREF	Reference Current Input. The Reference Current sets the full scale current sourced by each DAC.
	P0-P7	Pixel Address Inputs. The 8-bit Pixel Address is logically AND'ed with the Pixel Mask value before it is used to select a stored 18-bit color value from the palette.
	PCLK	Pixel (or Dot) Clock Input. The rising edge of PCLK samples the Pixel Address and $\overline{\text{BLANK}}$ inputs. PCLK is the system clock for the palette DAC pipeline.
	$\overline{\text{BLANK}}$	Blanking Input. A logic "0" at $\overline{\text{BLANK}}$ input overrides the current color value and forces the Analog Video Outputs to the zero (or Blank) level. The Color Palette can be updated while Blanking is active.
Power Supply	GND	Ground. GND should be connected to a solid ground plane in the system.
	VCC	Digital Supply. Nominal 5 Volts. VCC should be bypassed to GND with a high-frequency capacitor.
	VAA	Analog Supply. Nominal 5 Volts. VAA should be connected to a filtered system supply.
Microprocessor Interface	$\overline{\text{RD}}$	Read Enable Input. $\overline{\text{RD}}$ controls the timing of microprocesssor Read operations.
	$\overline{\text{WR}}$	Write Enable Input. $\overline{\text{WR}}$ controls the timing of microprocessor Write operations. $\overline{\text{RD}}$ and $\overline{\text{WR}}$ should not be active (low) at the same time.
	D0-D7	Program Data I/O Ports (Bidirectional). The rising edge of $\overline{\text{WR}}$ latches Program Data at D7-D0 into the selected internal register. The falling edge of $\overline{\text{RD}}$ enables D7-D0 as outputs and the rising edge of $\overline{\text{RD}}$ returns D7-D0 to a high impedance state.
	RS0, RS1	Register Select Inputs. Control the selection of internal registers. (See description on Internal Registers.) The falling edge of $\overline{\text{RD}}$ or $\overline{\text{WR}}$ latches in the value at RS1, RSO.

Internal Registers

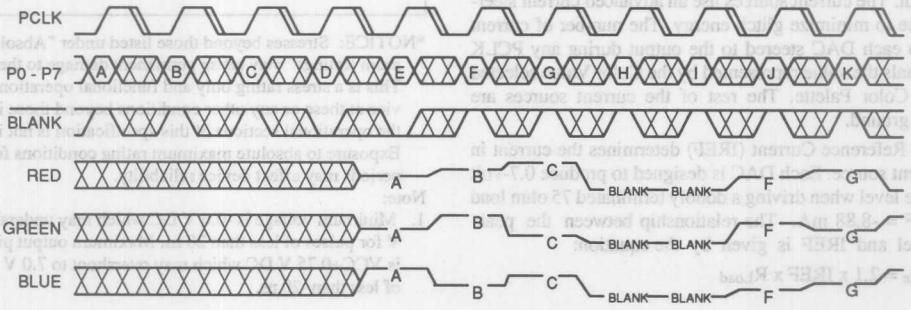
RS1	RS0	Bits	Register Name	Functional Description
0	0	8	Pixel Address (Write Mode)	The Pixel Address Register is accessed via Register Address (0,0) or (1,1). Reading the Pixel Address value from (0,0) is the same as reading from (1,1). A pixel address value is normally written to Pixel Address Register at (0,0) before one or more color values are written to the Color Palette. A pixel address value is normally written to Pixel Address Register at (1,1) before one or more color values are read from the Color Palette.
1	1	8	Pixel Address (Read Mode)	
0	1	18	Color Value	The Color Value Register acts as a buffer between the 18-bit wide Color Palette and the 8-bit microprocessor interface. Each READ and WRITE at (0,1) consists of three byte transfers in the order of RED first, GREEN second and BLUE last. Only the LSBs D5-D0 of each byte are used, the two MSBs are set to "0" when a color value is read. The Pixel Address Register automatically increments after each 18-bit color value Read or Write operation. Each color value READ or WRITE operation overrides the pixel stream for one PCLK period.
1	0	8	Pixel Mask	The Pixel Mask value is bitwise AND'ed with the Pixel Address value at P7-P0. A "1" in a position of the Pixel Mask will not change the corresponding bit in the Pixel Address, while a "0" sets that bit to "0". Pixel Address supplied via the microprocessor interface is not affected by the Pixel Mask.

Device Operation

COLOR PALETTE: The AT76C176 provides an 18-bit wide by 256 word deep color palette static RAM array for storing the desired color intensity values. Each word is divided into three fields for the RED, GREEN and BLUE video DACs respectively. The eight-bit wide Pixel Address is decoded and used to select a particular location in the RAM array. The color value retrieved from that location is then used as inputs to the three video DACs which convert the digital color code into analog color intensity values.

The AT76C176 achieves low power, high speed operation by using an advanced pipelined palette DAC architecture. Delay from Pixel Address to color intensity value out is three PCLK periods.

Video Pipeline Timing Diagram



MPU INTERFACE: The AT76C176 provides a standard microprocessor interface which allows the host display controller to access the Color Palette RAM and all internal registers of the AT76C176. MPU READ and WRITE operations are internally synchronized with the video pipeline and therefore can take place asynchronously from the normal pixel mapping operation. An on-chip address counter allows the MPU to READ or WRITE the Color Palette in a Block Mode.

COLOR PALETTE READ AND WRITE: Four MPU operations are required to write (i.e. store a Color Value) to a specific location in the Color Palette RAM. The desired RAM address is first written into the internal Pixel Address register by executing a WRITE operation at register address (0,0). A new Color Value is next written into the internal Color Value register at register address (0,1) by three consecutive WRITE operations, with the RED color first, GREEN second and BLUE last. Only LSBs D5-D0 of each byte transferred are used. The new Color Value is then automatically written into the designated address in the Color Palette RAM.

Similarly, four MPU operations are required to read a Color Value from a specific location in the Color Palette RAM. The RAM address is written into the internal Pixel Address register by executing a WRITE operation at register address (1,1). The Color Value stored in that particular RAM location is automatically transferred to the internal Color Value Register. Three consecutive READ operations are then required to read the retrieved Color Value in three bytes, with the RED color first, GREEN second and BLUE last. Only the last six LSBs D5-D0 contain valid data, the two MSBs are set to "0".

BLOCK READ AND WRITE MODE: The on-chip Pixel Address Register automatically increments by one after each complete Color Value READ or WRITE operation. This useful feature allows an entire block of the Color Palette RAM to be accessed by simply writing the starting address into the Pixel Address register at the appropriate register address. Subsequent READ or WRITE operations require only three-byte transfers at D7-D0.

TRIPLE VIDEO DAC: Each of the three video DACs on the AT76C176 consists of an array of current sources tied to a common output. The current sources use an advanced current steering scheme to minimize glitch energy. The number of current sources in each DAC steered to the output during any PCLK period equals the value represented by the Color Value selected from the Color Palette. The rest of the current sources are steered to ground.

The input Reference Current (IREF) determines the current in each current source. Each DAC is designed to produce 0.7-volt peak white level when driving a doubly terminated 75 ohm load with IREF = -8.88 mA. The relationship between the peak white level and IREF is given by the equation:

$V_{Peak\ White} = 2.1 \times IREF \times R_{Load}$

BLANKING: The AT76C176 supports composite blanking at all three RED, GREEN and BLUE video outputs. The $\overline{BLANK}$ input is latched on the rising edge of PCLK and affects the analog video outputs after three PCLK periods. An internal pipelined delay circuit is used to synchronize the $\overline{BLANK}$ input with the normal pixel pipeline. A logic "0" at $\overline{BLANK}$ input overrides the current color value and forces the analog video outputs to the zero (or Blank) level. The $\overline{BLANK}$ circuit has no effect on the MPU interface and the Color Palette remains accessible via READ and WRITE.

PIXEL MASK: The AT76C176 features an advanced on-chip Pixel Mask which is very useful for cursor control, flashing objects, and animation. The Pixel Mask value stored in internal register (1,0) is bitwise AND'ed with the input Pixel Address value at P7-P0 to form the actual RAM address for the Color Palette. A "1" in a position of the Pixel Mask will not change the corresponding bit in the Pixel Address, while a "0" sets that bit to "0". Pixel Addresses supplied via the MPU interface are not affected by the Pixel Mask.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to 125°C
Storage Temperature	-65°C to 150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to 7.0 V(1)
Power Dissipation	1.5 W
Reference Current	-15 mA
Analog Output Current	45 mA
DC Digital Output Current	25 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
1. Minimum voltage is -0.6 V DC which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is VCC+0.75 V DC which may overshoot to 7.0 V for pulses of less than 20 ns.

D.C. and A.C. Operating Range

		AT76C176-66	AT76C176-50	AT76C176-40	VCC/VAA Power Supplies
Operating Temperature Range(Case)	Com.	0° C - 70° C			5 V ± 5%
			0° C - 70° C	0° C - 70° C	5 V ± 10%
	Ind.		-40° C - 85° C	-40° C - 85° C	5 V ± 10%
	Mil.			-55° C -125° C	5 V ± 5%

D.C. Characteristics

Symbol	Parameter	Conditions	All Min	40 MHz Max	50 MHz Max	66 MHz Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1 V to V_{CC}+0.1 V		10	10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1 V to V_{CC} + 0.1 V		10	10	10	µA
I_{CC}	Power Supply Current	IO = 21 mA Digital Outputs Open		160	170	190	mA
I_{REF}	Reference Current		-7	-10	-10	-10	mA
V_{IL}	Input Low Voltage		-0.5	0.8	0.8	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}+0.5	V_{CC}+0.5	V_{CC}+0.5	V
V_{OL}	Output Low Voltage	IO = 5 mA		0.4	0.4	0.4	V
V_{OH}	Output High Voltage	IO = -5 mA	2.4				V
V_{REF}	Voltage at IREF Input		V_{CC}-3	V_{CC}	V_{CC}	V_{CC}	V

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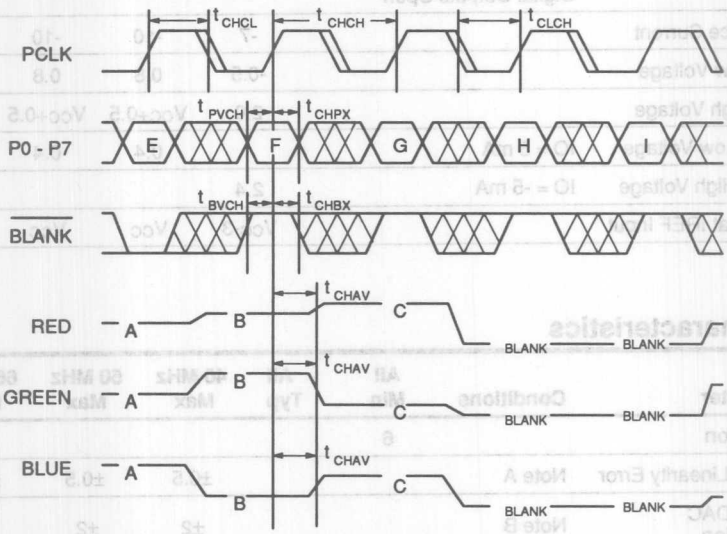
Video DAC Characteristics

Symbol	Parameter	Conditions	All Min	All Typ	40 MHz Max	50 MHz Max	66 MHz Max	Units
RES	Resolution		6					bits
ILE	Integral Linearity Error	Note A			±0.5	±0.5	±0.5	LSB
COR	DAC to DAC Correlation	Note B			±2	±2	±2	%
FSE	Full Scale Error	Note C			±5	±5	±5	%
DVT	Glitch Energy	Notes D, E		75				pVsec
IO	Output Current	VO < 1 V		18.6	21	21	21	mA
VO	Output Voltage	IO < 21 mA		0.7	1.5	1.5	1.5	V
t_{DR}	Rise Time (10% to 90%)	Notes D, E			8	8	6	ns
t_{DF}	Full Scale Settling Time	Notes D, E, F			25	20	15	ns

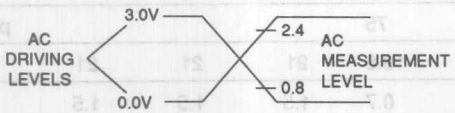
Video Timing Characteristics

Symbol	Parameter	Conditions	All Max	40 MHz Min	50 MHz Min	66 MHz Min	Units
t_{CHCH}	PCLK Period (τ)		10000	28	20	15	ns
Δt_{CHCH}	PCLK Jitter	$t_{CHCH} = \tau$	±2.5				%
t_{CLCH}	PCLK Low Width		10000	9	6	5	ns
t_{CHCL}	PCLK High Width		10000	7	6	5	ns
t_{PVCH}	Pixel Word Setup Time			5	4	3	ns
t_{CHPX}	Pixel Word Hold Time			5	4	3	ns
t_{BVCH}	$\overline{\text{BLANK}}$ Setup Time			5	4	3	ns
t_{CHBX}	$\overline{\text{BLANK}}$ Hold Time			5	4	3	ns
t_{CHAV}	PCLK to DAC Output Valid	Note G	30	5	5	5	ns
Δt_{CHAV}	Differential Output Delay	Note H	2				ns
t_{CC}	Pixel Clock Transition Time		50				ns

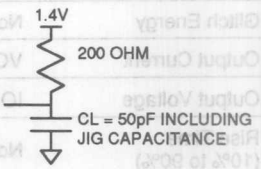
Video Timing Waveforms Diagram



Input Test Waveforms



Digital Input/Output Load



Notes: 1. t_R, t_F <3 ns (10% to 90%).
2. Input timing reference is at 1.5 V.

MPU Interface Timing Characteristics

Symbol	Parameter	Conditions	All Max	40 MHz Min	50 MHz Min	66 MHz Min	Units
t_{WLWH}	$\overline{WR}$ Pulse Width Low			50	50	50	ns
t_{RLRH}	$\overline{RD}$ Pulse Width Low			50	50	50	ns
t_{SVWL}	Register Select Setup Time	WRITE Operations		15	10	10	ns
t_{SVRL}	Register Select Setup Time	READ Operations		15	10	10	ns
t_{WLSX}	Register Select Hold Time	WRITE Operations		15	10	10	ns
t_{RLSX}	Register Select Hold Time	READ Operations		15	10	10	ns
t_{DVWH}	Write Data Setup Time			15	10	10	ns
t_{WHDX}	Write Data Hold Time			15	10	10	ns
t_{RLQX}	Output Turn-on Delay			5	5	5	ns
t_{RLQV}	Read Enable Access Time		40				ns
t_{RHQX}	Output Hold Time			5	5	5	ns
t_{RHQZ}	Output Turn-off Delay	Note I	20				ns
t_{WHWL1}	Successive Write Interval	τ=PCLK Period		4τ	4τ	4τ	ns
t_{WHRL1}	Write Followed by Read Interval	τ=PCLK Period		4τ	4τ	4τ	ns
t_{RHRL1}	Successive Read Interval	τ=PCLK Period		4τ	4τ	4τ	ns
t_{RHWL1}	Read Followed by Write Interval	τ=PCLK Period		4τ	4τ	4τ	ns
t_{WHWL2}	Write After Color Write	τ=PCLK Period		4τ	4τ	4τ	ns
t_{WHRL2}	Read After Color Write	τ=PCLK Period		4τ	4τ	4τ	ns
t_{RHRL2}	Read After Color Read	τ=PCLK Period		7τ	7τ	7τ	ns
t_{RHWL2}	Write After Color Read	τ=PCLK Period		7τ	7τ	7τ	ns
t_{WHRL3}	Read After Read Address Write	τ=PCLK Period		7τ	7τ	7τ	ns
t_{WREN}	Read/Write Enable Transition Time		50				ns

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Notes

Note A: Measured from best fit line through DAC transfer curve.

Note B: Measured from the mid point of the distribution of the three DAC transfer curves.

Note C: $FSE=\left[\frac{VO-2.1\times IREF\times R_{Load}}{2.1\times IREF\times R_{Load}}\right]\times 100\%$

Note D: Z_{Load} = 37.5 ohm + 30 pF, IREF = -8.88 mA

Note E: This parameter is sampled and not 100% tested.

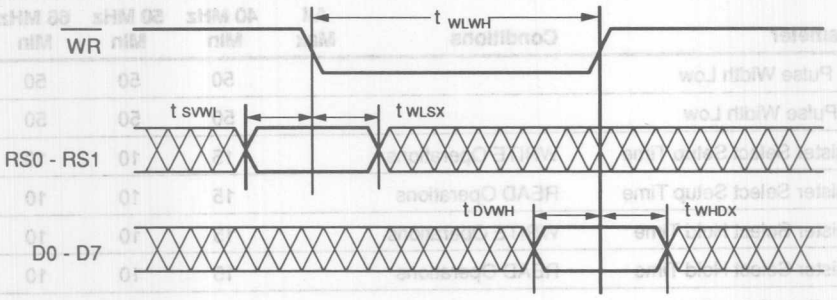
Note F: Measured from a 2% change in the DAC output voltage to within 2% of the final value.

Note G: Measured between the 50% point of the rising edge of PCLK and at the analog output halfway between successive output values.

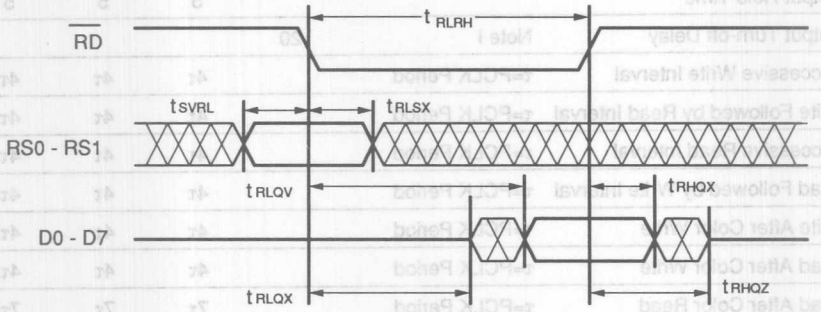
Note H: Measured between different analog outputs on the same device.

Note I: Measured at ±200 mV from steady state output values.

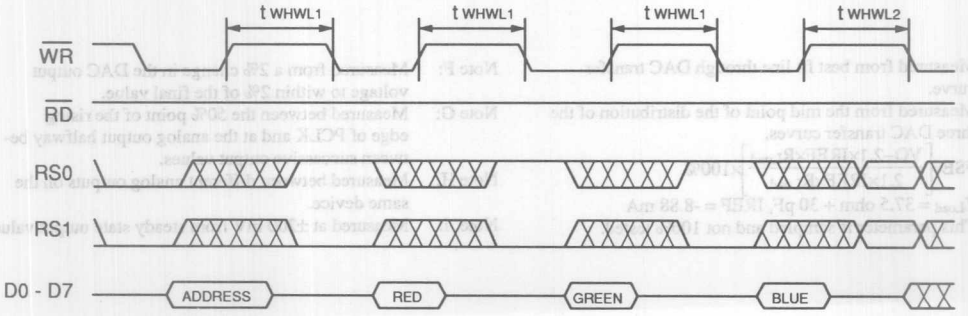
Write Operations Waveforms



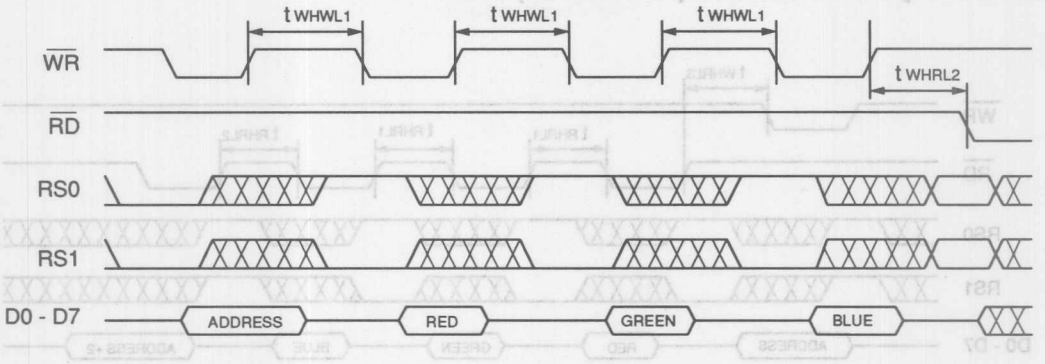
Read Operations Waveforms



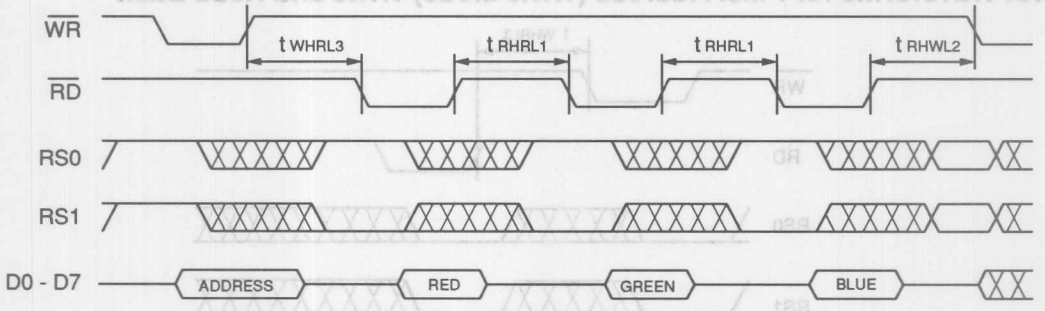
A.C. Waveforms for Color Value Write Followed by Any Write



A.C. Waveforms for Color Value Write Followed by Any Read

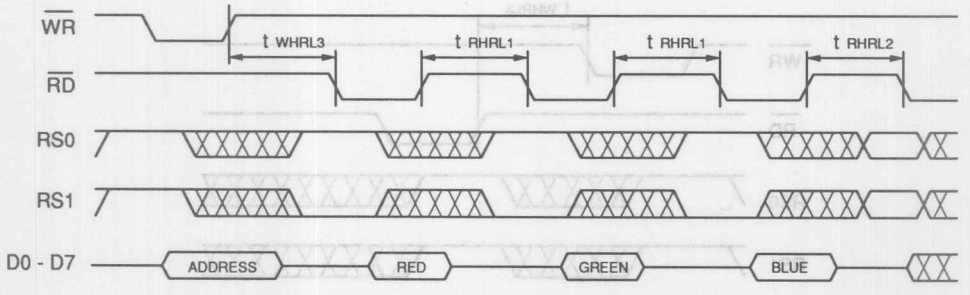


A.C. Waveforms for Color Value Read Followed by Any Write



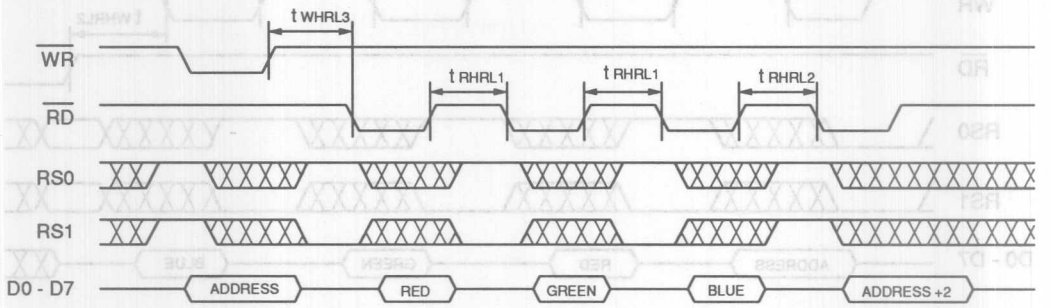
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A.C. Waveforms for Color Value Read Followed by Any Read

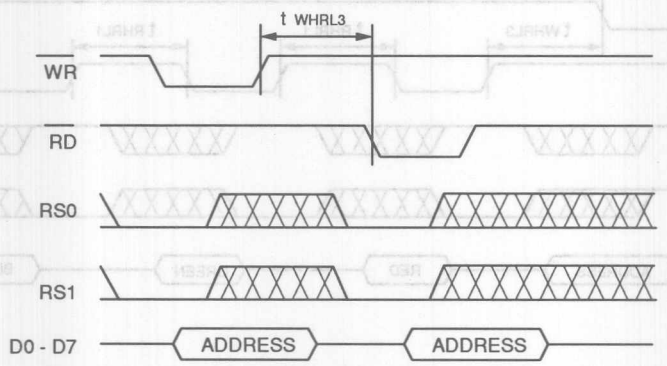


A.C. Waveforms for Color Value Read

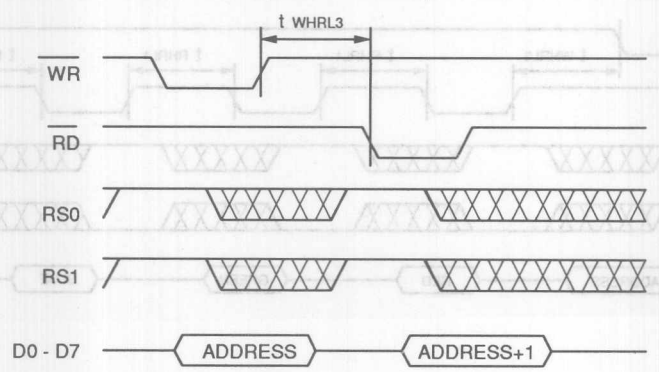
Followed by Pixel Address (Read Mode) Read



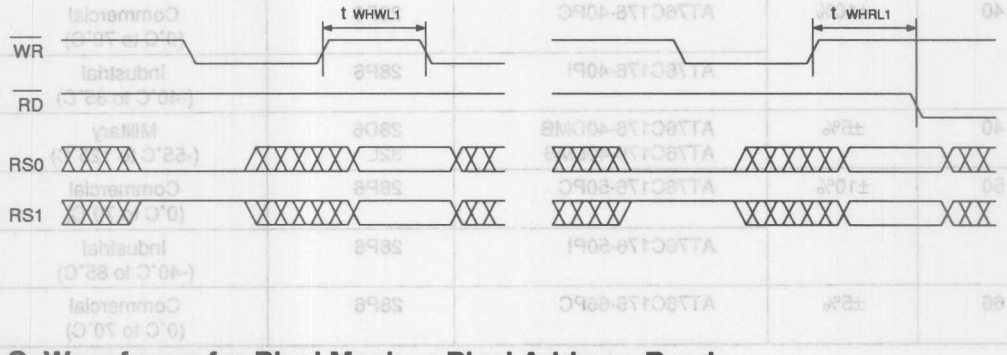
A.C. Waveforms for Pixel Address (Write Mode) Write and Read Back



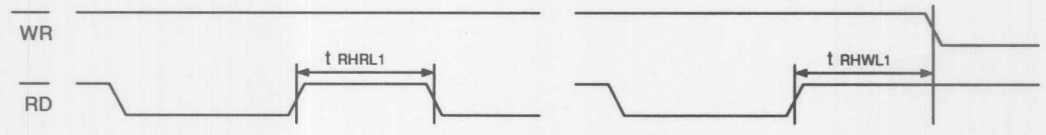
A.C. Waveforms for Pixel Address (Read Mode) Write and Read Back



A.C Waveforms for Pixel Mask Write Followed by Any Write or Read



A.C. Waveforms for Pixel Mask or Pixel Address Read Followed by Any Read or Write



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Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
40	±10%	AT76C176-40PC	28P6	Commercial (0°C to 70°C)
		AT76C176-40PI	28P6	Industrial (-40°C to 85°C)
40	±5%	AT76C176-40DMB AT76C176-40LMB	28D6 32L	Military (-55°C to 125°C)
50	±10%	AT76C176-50PC	28P6	Commercial (0°C to 70°C)
		AT76C176-50PI	28P6	Industrial (-40°C to 85°C)
66	±5%	AT76C176-66PC	28P6	Commercial (0°C to 70°C)

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)

Features

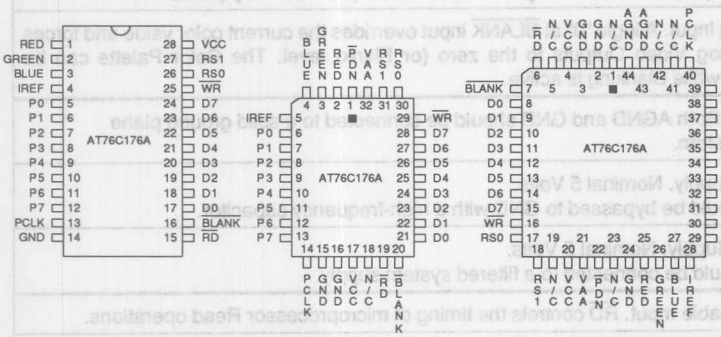
- Personal System/2*, 8514/A, and VGA* Compatible
- High Pixel Rates to 135 MHz
- Supports High Resolution 1280 x 1280 Pixels Color Graphics Displays
- Low Standby Current Less than 1 mA (Typical)
- Anti-Sparkle Circuitry
- Triple 6-Bit DACs Display 256K Possible Colors
- Pixel Word Mask and Composite Blank on All Three Channels
- 18-Bit Wide Color Palette Stores 256 Colors
- High Reliability CMOS Technology
  - 2000 V ESD Protection
  - 200 mA Latchup Immunity
- Available in Standard 28-Pin DIP, 32-Pin LCC, and 32- and 44-Pin Plastic LCC
- Full Military, Commercial and Industrial Temperature Ranges

Description

The AT76C176A is a second generation color palette DAC which provides direct drives for high resolution RGB color displays with resolutions up to 1280 x 1280 pixels. The AT76C176A integrates three high performance six-bit video DACs (Digital-to-Analog Converters), an advanced 256 x 18 Color Palette (Color Look-up Table) and a versatile microprocessor interface on a monolithic substrate.

The AT76C176A supports the RS170 video standard and graphics controllers compatible with the VGA and extended VGA standards. This device allows 256 colors to be displayed out of a total of 262,144 colors. The AT76C176A provides composite blank outputs on all three channels. Additional advanced features include on-chip anti-sparkle circuitry and pixel mask logic which allows displayed colors to be modified in a single write cycle rather than by altering the contents of the color palette. For lap-top computers and other battery powered applications, the AT76C176A provides a low power standby mode of operation.

Pin Configurations



Pin Name	Function
RED GREEN BLUE	Analog Video Outputs for R,G,B Guns
IREF	Reference Current Input
P0-P7	Pixel Address Inputs
PCLK	Pixel Clock Input
AGND	Analog Ground
GND	Ground
$\overline{RD}$	Read Enable Input

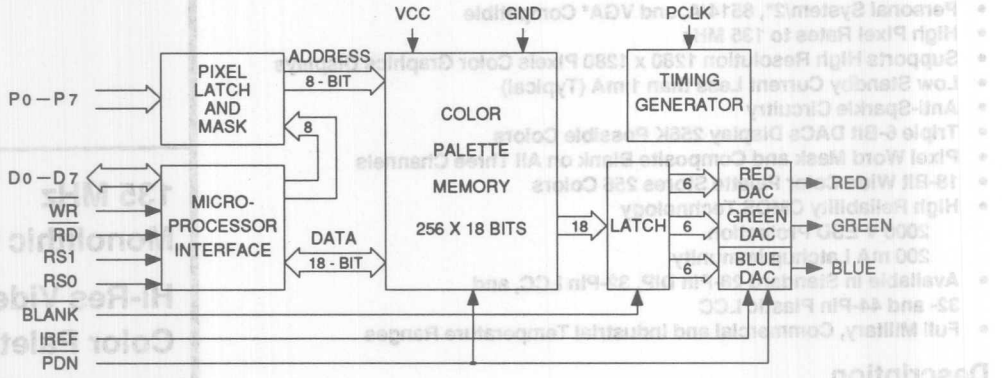
$\overline{BLANK}$	Video Blanking Input
D0-D7	Program Data I/O
$\overline{WR}$	Write Enable Input
RS0,RS1	Register Select Inputs
$\overline{PDN}$	Power-Down Input
VCC	+5 Volts Supply Input
VAA	+5 Volts Analog Supply Input
N/C	No Connect

* Personal System/2 and VGA are registered trademarks of IBM Corporation.

135 MHz Monolithic CMOS Hi-Res Video Color Palette

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Block Diagram



Pin Definitions

	Symbol	Functional Descriptions
Video Interface	RED GREEN BLUE	Analog Video Outputs. These are the outputs of the triple video DACs. The 18-bit wide color palette output and the $\overline{\text{BLANK}}$ input drive the DAC inputs.
	IREF	Reference Current Input. The Reference Current sets the full scale current sourced by each DAC.
	P0-P7	Pixel Address Inputs. The 8-bit Pixel Address is logically AND'ed with the Pixel Mask value before it is used to select a stored 18-bit color value from the palette.
	PCLK	Pixel (or Dot) Clock Input. The rising edge of PCLK samples the Pixel Address and $\overline{\text{BLANK}}$ inputs. PCLK is the system clock for the palette DAC pipeline.
	$\overline{\text{BLANK}}$	Blanking Input. A logic "0" at $\overline{\text{BLANK}}$ input overrides the current color value and forces the Analog Video Outputs to the zero (or Blank) level. The Color Palette can be updated while Blanking is active.
Power Supply	AGND GND	Ground. Both AGND and GND should be connected to a solid ground plane in the system.
	VCC	Digital Supply. Nominal 5 Volts. VCC should be bypassed to GND with a high-frequency capacitor.
	VAA	Analog Supply. Nominal 5 Volts. VAA should be connected to a filtered system supply.
Microprocessor Interface	$\overline{\text{RD}}$	Read Enable Input. $\overline{\text{RD}}$ controls the timing of microprocessor Read operations.
	$\overline{\text{WR}}$	Write Enable Input. $\overline{\text{WR}}$ controls the timing of microprocessor Write operations. $\overline{\text{RD}}$ and $\overline{\text{WR}}$ should not be active (low) at the same time.
	D0-D7	Program Data I/O Ports (Bidirectional). The rising edge of $\overline{\text{WR}}$ latches Program Data at D7-D0 into the selected internal register. The falling edge of $\overline{\text{RD}}$ enables D7-D0 as outputs and the rising edge of $\overline{\text{RD}}$ returns D7-D0 to a high impedance state.
	RS0, RS1	Register Select Inputs. Control the selection of internal registers. (See description on Internal Registers.) The falling edge of $\overline{\text{RD}}$ or $\overline{\text{WR}}$ latches in the value at RS1, RSO.
	$\overline{\text{PDN}}$	Power-Down Input. A logic "0" at $\overline{\text{PDN}}$ input powers down the video DAC and Color Palette circuits for low power standby mode operation. The Color Palette can still be read or updated if PCLK is active. $\overline{\text{PDN}}$ should be held at logic "1" for normal operation.

Internal Registers

RS1	RS0	Bits	Register Name	Functional Description
0	0	8	Pixel Address (Write Mode)	The Pixel Address Register is accessed via Register Address (0,0) or (1,1). Reading the Pixel Address value from (0,0) is the same as reading from (1,1). A pixel address value is normally written to Pixel Address Register at (0,0) before one or more color values are written to the Color Palette. A pixel address value is normally written to Pixel Address Register at (1,1) before one or more color values are read from the Color Palette.
1	1	8	Pixel Address (Read Mode)	
0	1	18	Color Value	The Color Value Register acts as a buffer between the 18-bit wide Color Palette and the 8-bit microprocessor interface. Each READ and WRITE at (0,1) consists of three byte transfers in the order of RED first, GREEN second and BLUE last. Only the LSBs D5-D0 of each byte are used, the two MSBs are set to "0" when a color value is read. The Pixel Address Register automatically increments after each 18-bit color value READ or WRITE operation. Each color value READ or WRITE operation overrides the pixel stream for one PCLK period.
1	0	8	Pixel Mask	The Pixel Mask value is bitwise AND'ed with the Pixel Address value at P7-P0. A "1" in a position of the Pixel Mask will not change the corresponding bit in the Pixel Address, while a "0" sets that bit to "0". Pixel Address supplied via the microprocessor interface is not affected by the Pixel Mask.

Device Operation

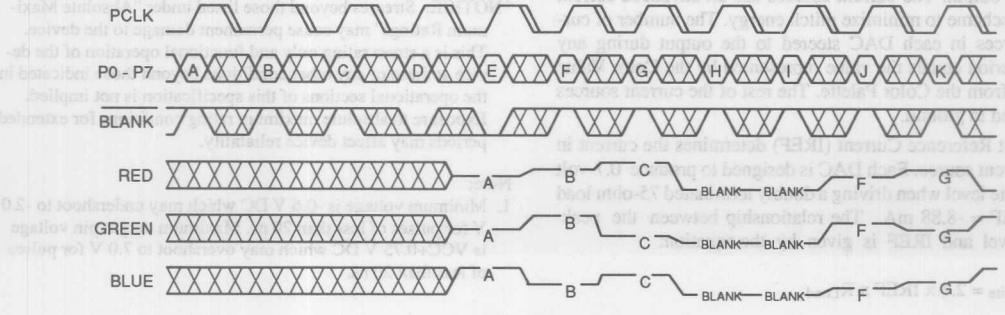
COLOR PALETTE: The AT76C176A provides an 18-bit wide by 256-word deep color palette static RAM array for storing the desired color intensity values. Each word is divided into three fields for the RED, GREEN and BLUE video DACs respectively. The eight-bit wide Pixel Address is decoded and used to select a particular location in the RAM array. The color value retrieved from that location is then used as inputs to the three video DACs which convert the digital color code into analog color intensity values.

The AT76C176A achieves low power, high speed operation by using an advanced pipelined palette DAC architecture. Delay from Pixel Address to color intensity value out is three PCLK periods.

MPU INTERFACE: The AT76C176A provides a standard microprocessor interface which allows the host display controller to access the Color Palette RAM and all internal registers of the AT76C176A. MPU READ and WRITE operations are internally synchronized with the video pipeline and therefore can take place asynchronously from the normal pixel mapping operation. An on-chip address counter allows the MPU to READ or WRITE the Color Palette in a Block Mode.

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Video Pipeline Timing Diagram



COLOR PALETTE READ AND WRITE: Four MPU operations are required to write (i.e. store a Color Value) to a specific location in the Color Palette RAM. The desired RAM address is first written into the internal Pixel Address register by executing a WRITE operation at register address (0,0). A new Color Value is next written into the internal Color Value register at register address (0,1) by three consecutive WRITE operations, with the RED color first, GREEN second and BLUE last. Only LSBs D5-D0 of each byte transferred are used. The new Color Value is then automatically written into the designated address in the Color Palette RAM.

Similarly, four MPU operations are required to read a Color Value from a specific location in the Color Palette RAM. The RAM address is written into the internal Pixel Address register by executing a WRITE operation at register address (1,1). The Color Value stored in that particular RAM location is automatically transferred to the internal Color Value Register. Three consecutive READ operations are then required to read the retrieved Color Value in three bytes, with the RED color first, GREEN second and BLUE last. Only the last six LSBs D5-D0 contain valid data, the two MSBs are set to "0".

BLOCK READ AND WRITE MODE: The on-chip Pixel Address Register automatically increments by one after each complete Color Value READ or WRITE operation. This useful feature allows an entire block of the Color Palette RAM to be accessed by simply writing the starting address into the Pixel Address register at the appropriate register address. Subsequent READ or WRITE operations require only three-byte transfers at D7-D0.

ANTI-SPARKLE CIRCUITRY: The outputs of the Color Palette RAM drive the inputs of the video DACs via an 18-bit anti-sparkle register. Whenever a Read or Write is performed on the Color Palette through the MPU interface, the anti-sparkle register substitutes the latest pixel Color Value with the previous pixel Color value. Since the Color Value may be corrupted when the Color Palette is accessed during active display, this feature minimizes and often eliminates any visible sparkles on the video display. The anti-sparkle circuitry makes unrestricted access to the Color Palette RAM viable.

TRIPLE VIDEO DAC: Each of the three video DACs on the AT76C176A consists of an array of current sources tied to a common output. The current sources use an advanced current steering scheme to minimize glitch energy. The number of current sources in each DAC steered to the output during any PCLK period equals the value represented by the Color Value selected from the Color Palette. The rest of the current sources are steered to ground.

The input Reference Current (IREF) determines the current in each current source. Each DAC is designed to produce 0.7-volt peak white level when driving a doubly terminated 75-ohm load with IREF = -8.88 mA. The relationship between the peak white level and IREF is given by the equation:

$$V_{Peak\ White} = 2.1 \times IREF \times R_{Load}$$

BLANKING: The AT76C176A supports composite blanking at all three RED, GREEN and BLUE video outputs. The $\overline{BLANK}$ input is latched on the rising edge of PCLK and affects the analog video outputs after three PCLK periods. An internal pipelined delay circuit is used to synchronize the $\overline{BLANK}$ input with the normal pixel pipeline. A logic "0" at $\overline{BLANK}$ input overrides the current color value and forces the analog video outputs to the zero (or Blank) level. The $\overline{BLANK}$ circuit has no effect on the MPU interface and the Color Palette remains accessible via READ and WRITE.

PIXEL MASK: The AT76C176A features an advanced on-chip Pixel Mask which is very useful for cursor control, flashing objects, and animation. The Pixel Mask value stored in internal register (1,0) is bitwise AND'ed with the input Pixel Address value at P7-P0 to form the actual RAM address for the Color Palette. A "1" in a position of the Pixel Mask will not change the corresponding bit in the Pixel Address, while a "0" sets that bit to "0". Pixel Addresses supplied via the MPU interface are not affected by the Pixel Mask.

POWER-DOWN MODE: In PLCC packages, the AT76C176A provides an on-chip power-down feature for use in lap-top computers and other battery-powered applications. During normal operation, pin $\overline{PDN}$ should be held as logic "1." A logic "0" at $\overline{PDN}$ powers down the video DAC and Color Palette circuits.

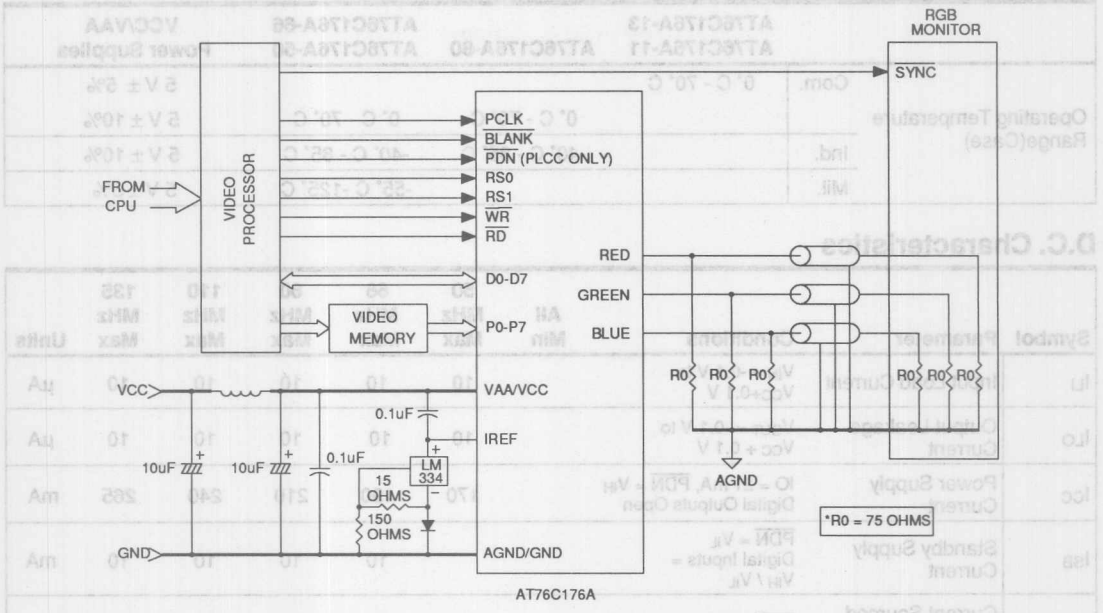
Absolute Maximum Ratings*

Temperature Under Bias	-55°C to 125°C
Storage Temperature	-65°C to 150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to 7.0 V(1)
Power Dissipation	1.5 W
Reference Current	-15 mA
Analog Output Current	45 mA
DC Digital Output Current	25 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
1. Minimum voltage is -0.6 V DC which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is VCC+0.75 V DC which may overshoot to 7.0 V for pulses of less than 20 ns.

Sample Connection for Typical Application



System Implementation Considerations

POWER SUPPLY DECOUPLING AND GROUNDING: To obtain the cleanest possible analog outputs from the AT76C176A, digital noise coupling into the analog signal paths needs to be minimized. The video data paths, power supply lines and ground planes on the circuit board should be laid out carefully to reduce noise coupling. As illustrated in the diagram above (Sample Connection for Typical Application), a separate VAA line decoupled to AGND with an electrolytic capacitor in parallel with a smaller ceramic chip capacitor should be used for the analog circuits on the AT76C176A. Similarly, a separate analog ground return, AGND, which is connected to the lowest impedance point in the system ground plane, should be used.

For best results, four-layer PC boards with separate ground and power supply planes are recommended. The AGND plane should be laid out as an island or tub underneath the AT76C176A. All video frequency signal traces should be kept as short as possible to minimize radiation and all decoupling capacitors should be placed as close to the AT76C176A as the layout rules permit.

Noise and transients on the power and ground lines can be coupled or aliased into the video circuits by the switching action of the AT76C176A. For applications at 66 MHz and above, it may be necessary to isolate both VAA and AGND from the system supplies with inductors of appropriate values.

CURRENT REFERENCE: The maximum full scale output of the video DACs is determined by the reference current supplied externally at pin IREF. An adjustable current source such as the LM334 is recommended to set the reference current at 8.88 mA for a full scale output of 0.7 volt when driving a 37.5-ohm load. The video DACs employ current sources which are referenced to the positive supply voltage. A high quality 0.1-µF chip capacitor may be required to decouple IREF to VAA or VCC.

VIDEO INTERFACE: The RED, GREEN and BLUE video outputs are designed to drive doubly terminated 75-ohm lines. To minimize ringing due to impedance mismatch, 75-ohm ± 1% thin film resistors should be placed close to the AT76C176A on the PC board.

To comply with FCC RF emission regulations, ferrite beads can be inserted at the video outputs to limit the amount of high frequency emission. The AT76C176A is designed to produce very little high frequency digital feedthrough.

SYSTEM TIMING: The pixel clock, PCLK, controls the timing of the Color Palette and the Video DACs. To obtain the highest quality display possible with the AT76C176A, Setup and Hold time requirements with respect to PCLK should be strictly adhered to. The duty cycle limits of PCLK should also be met over the entire display.

DIGITAL INTERFACE: When the high impedance digital inputs of the CMOS AT76C176A are driven by low impedance sources, considerable ringing can occur, which may degrade high video rate operation. Impedance matching resistors of the order of 50 ohms can be inserted in series at the inputs to the Pixel Address and Blanking inputs to reduce ringing. This also minimizes the amount of high frequency emission due to excessively high slew rates at the video data inputs.

D.C. and A.C. Operating Range

		AT76C176A-13 AT76C176A-11	AT76C176A-80	AT76C176A-66 AT76C176A-50	VCC/VAA Power Supplies
Operating Temperature Range(Case)	Com.	0° C - 70° C			5 V ± 5%
			0° C - 70° C	0° C - 70° C	5 V ± 10%
	Ind.		-40° C - 85° C	-40° C - 85° C	5 V ± 10%
	Mil.			-55° C -125° C	5 V ± 5%

D.C. Characteristics

Symbol	Parameter	Conditions	All Min	50 MHz Max	66 MHz Max	80 MHz Max	110 MHz Max	135 MHz Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1 V to V_{CC}+0.1 V		10	10	10	10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1 V to V_{CC} + 0.1 V		10	10	10	10	10	µA
I_{CC}	Power Supply Current	IO = 21 mA, $\overline{PDN}$ = V_{IH} Digital Outputs Open		170	190	210	240	265	mA
I_{SB}	Standby Supply Current	$\overline{PDN}$ = V_{IL} Digital Inputs = V_{IH} / V_{IL}			10	10	10	10	mA
I_{ILP}	Current Sourced by Pin PDN	$\overline{PDN}$ = V_{IL}			20	20	20	20	µA
I_{REF}	Reference Current		-7	-10	-10	-10	-10	-10	mA
V_{IL}	Input Low Voltage		-0.5	0.8	0.8	0.8	0.8	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}+0.5	V_{CC}+0.5	V_{CC}+0.5	V_{CC}+0.5	V_{CC}+0.5	V
V_{OL}	Output Low Voltage	IO = 5 mA		0.4	0.4	0.4	0.4	0.4	V
V_{OH}	Output High Voltage	IO = -5 mA	2.4						V
V_{REF}	Voltage at IREF Input		V_{CC}-3	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V

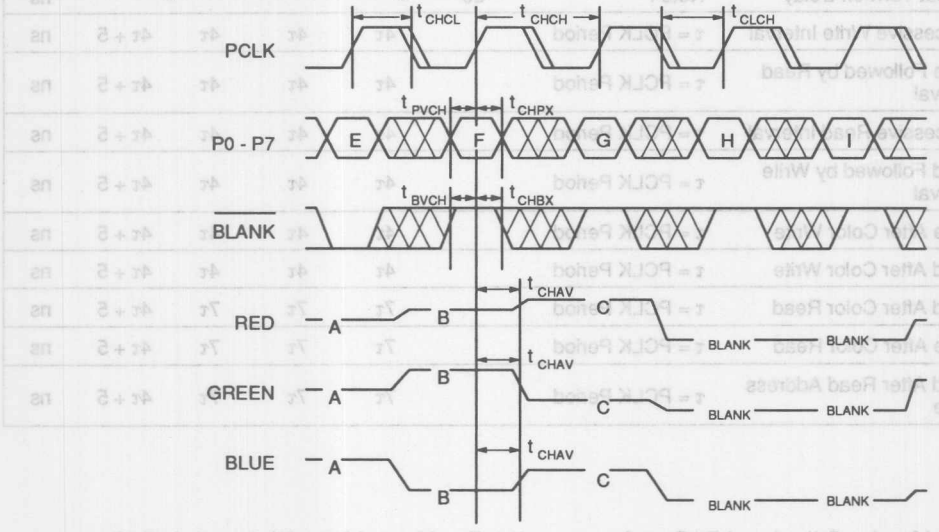
Video DAC Characteristics

Symbol	Parameter	Conditions	All Min	All Typ	50 MHz Max	66 MHz Max	80 MHz Max	110 MHz Max	135 MHz Max	Units
RES	Resolution		6							bits
ILE	Integral Linearity Error	Note A			±0.5	±0.5	±0.5	±0.5	±0.5	LSB
COR	DAC to DAC Correlation	Note B			±2	±2	±2	±2	±2	%
FSE	Full Scale Error	Note C			±5	±5	±5	±5	±5	%
DVT	Glitch Energy	Notes D, E		75						pVsec
IO	Output Current	VO < 1 V		18.6	21	21	21	21	21	mA
VO	Output Voltage	IO < 21 mA		0.7	1.5	1.5	1.5	1.5	1.5	V
t_{DR}	Rise Time (10% to 90%)	Notes D, E			8	6	6	5	4	ns

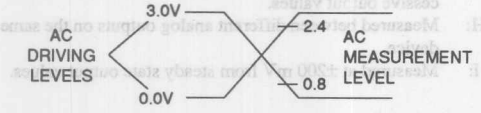
Video Timing Characteristics

Symbol	Parameter	Conditions	All Max	50 MHz Min	66 MHz Min	80 MHz Min	110 MHz Min	135 MHz Min	Units
t_{CHCH}	PCLK Period (τ)	Normal	10000	20	15	12.5	9	7.4	ns
Δt_{CHCH}	PCLK Jitter	$t_{CHCH} = \tau$	±2.5						%
t_{CLCH}	PCLK Low Width	Normal	10000	6	5	5	4	3.2	ns
t_{CHCL}	PCLK High Width	Normal	10000	6	5	5	4	3.2	ns
t_{PVCH}	Pixel Word Setup Time			4	3	3	3	2.5	ns
t_{CHPX}	Pixel Word Hold Time			4	3	3	2	2	ns
t_{BVCH}	$\overline{\text{BLANK}}$ Setup Time			4	3	3	3	2.5	ns
t_{CHBX}	$\overline{\text{BLANK}}$ Hold Time			4	3	3	2	2	ns
t_{CHAV}	PCLK to DAC Output Valid	Note G	30	5	5	5	5	5	ns
Δt_{CHAV}	Differential Output Delay	Note H	2						ns
t_{CC}	Pixel Clock Transition Time		50						ns

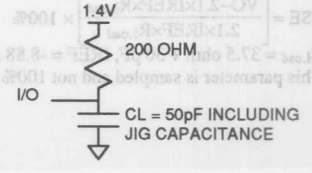
Video Timing Waveforms Diagram



Input Test Waveforms



Digital Input/Output Load



Notes: 1. t_R, t_F <3 ns (10% to 90%).
2. Input timing reference is at 1.5 V.

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MPU Interface Timing Characteristics

Symbol	Parameter	Conditions	All Max	66/50 MHz Min	80 MHz Min	110 MHz Min	135 MHz Min	Units
t_{WLWH}	$\overline{WR}$ Pulse Width Low			50	50	50	50	ns
t_{RLRH}	$\overline{RD}$ Pulse Width Low			50	50	50	50	ns
t_{SVWL}	Register Select Setup Time	WRITE Operations		10	10	10	10	ns
t_{SVRL}	Register Select Setup Time	READ Operations		10	10	10	10	ns
t_{WLSX}	Register Select Hold Time	WRITE Operations		10	10	10	10	ns
t_{RLSX}	Register Select Hold Time	READ Operations		10	10	10	10	ns
t_{DVWH}	Write Data Setup Time			10	10	10	10	ns
t_{WHDX}	Write Data Hold Time			10	10	10	10	ns
t_{RLQX}	Output Turn-on Delay			5	5	5	5	ns
t_{RLQV}	Read Enable Access Time		40					ns
t_{RHQX}	Output Hold Time			5	5	5	5	ns
t_{RHQZ}	Output Turn-off Delay	Note I	20					ns
t_{WHWL1}	Successive Write Interval	τ = PCLK Period		4τ	4τ	4τ	4τ + 5	ns
t_{WHRL1}	Write Followed by Read Interval	τ = PCLK Period		4τ	4τ	4τ	4τ + 5	ns
t_{RHRL1}	Successive Read Interval	τ = PCLK Period		4τ	4τ	4τ	4τ + 5	ns
t_{RHWL1}	Read Followed by Write Interval	τ = PCLK Period		4τ	4τ	4τ	4τ + 5	ns
t_{WHWL2}	Write After Color Write	τ = PCLK Period		4τ	4τ	4τ	4τ + 5	ns
t_{WHRL2}	Read After Color Write	τ = PCLK Period		4τ	4τ	4τ	4τ + 5	ns
t_{RHRL2}	Read After Color Read	τ = PCLK Period		7τ	7τ	7τ	4τ + 5	ns
t_{RHWL2}	Write After Color Read	τ = PCLK Period		7τ	7τ	7τ	4τ + 5	ns
t_{WHRL3}	Read After Read Address Write	τ = PCLK Period		7τ	7τ	7τ	4τ + 5	ns

Notes

Note A: Measured from best fit line through DAC transfer curve.

Note B: Measured from the mid point of the distribution of the three DAC transfer curves.

Note C: $FSE = \left[\frac{VO - 2.1 \times IREF \times R_{Load}}{2.1 \times IREF \times R_{Load}}\right] \times 100\%$

Note D: Z_{Load} = 37.5 ohm + 30 pF, IREF = -8.88 mA

Note E: This parameter is sampled and not 100% tested.

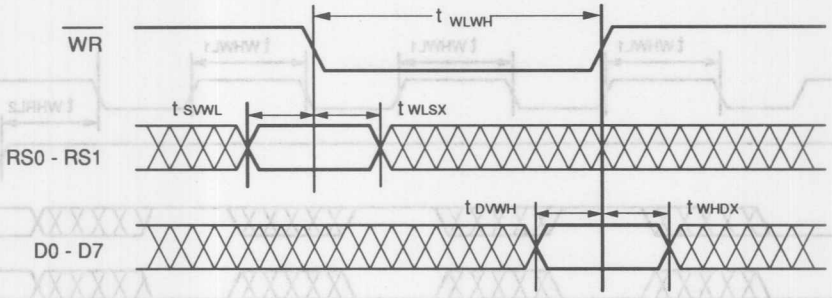
Note F: Measured from a 2% change in the DAC output voltage to within 2% of the final value.

Note G: Measured between the 50% point of the rising edge of PCLK and at the analog output halfway between successive output values.

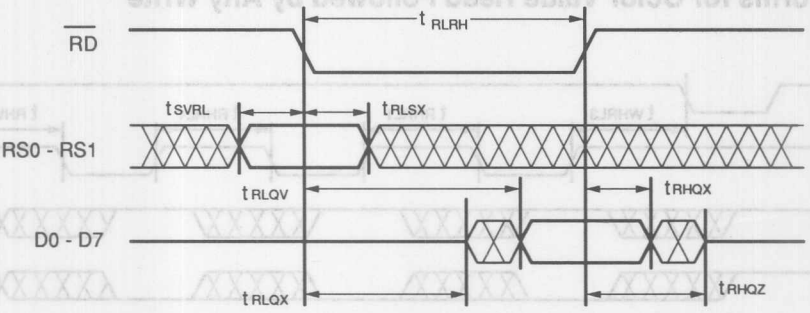
Note H: Measured between different analog outputs on the same device.

Note I: Measured at ±200 mV from steady state output values.

Write Operations Waveforms

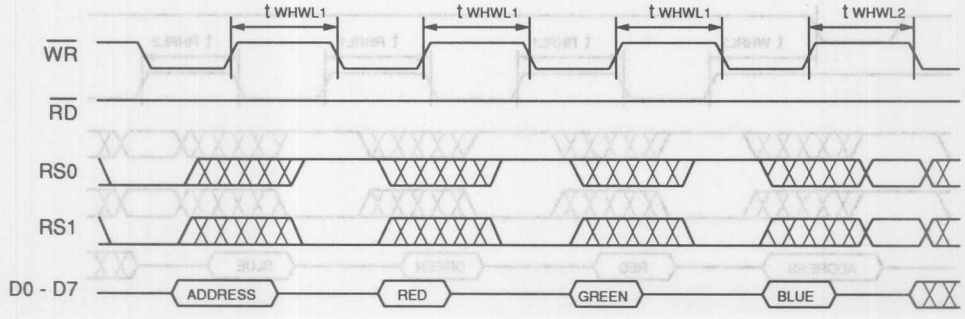


Read Operations Waveforms

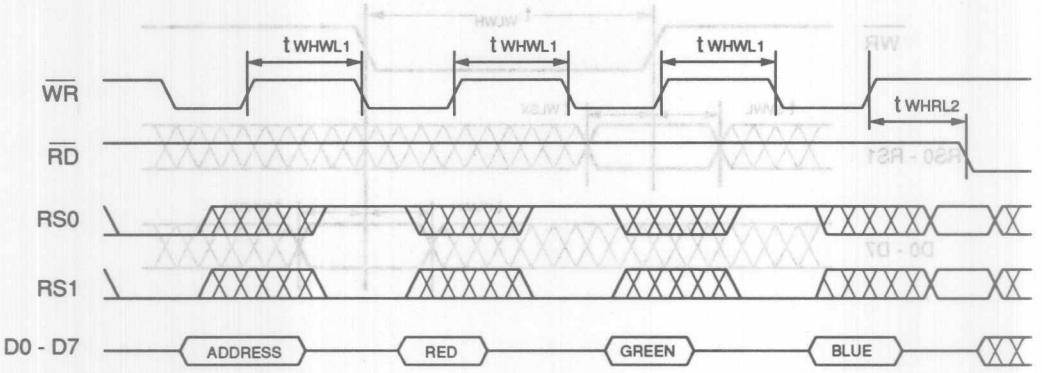


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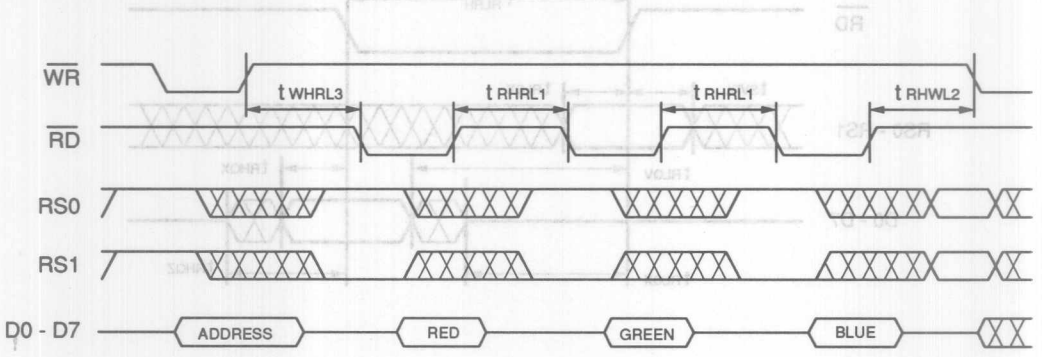
A.C. Waveforms for Color Value Write Followed by Any Write



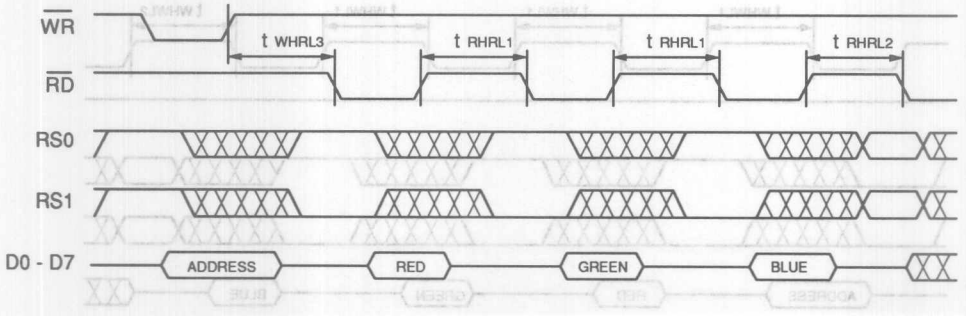
A.C. Waveforms for Color Value Write Followed by Any Read



A.C. Waveforms for Color Value Read Followed by Any Write

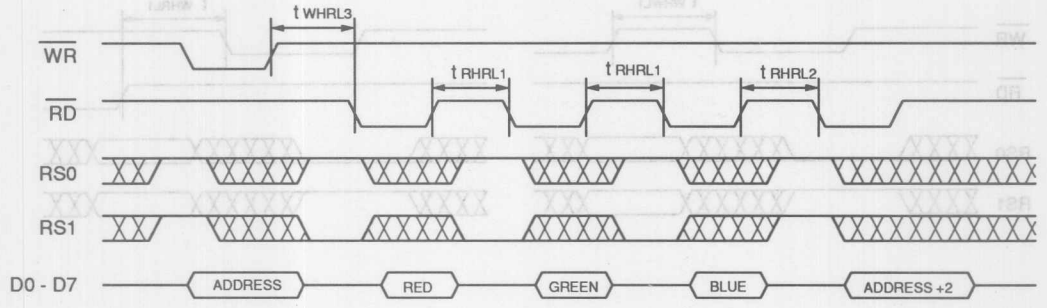


A.C. Waveforms for Color Value Read Followed by Any Read

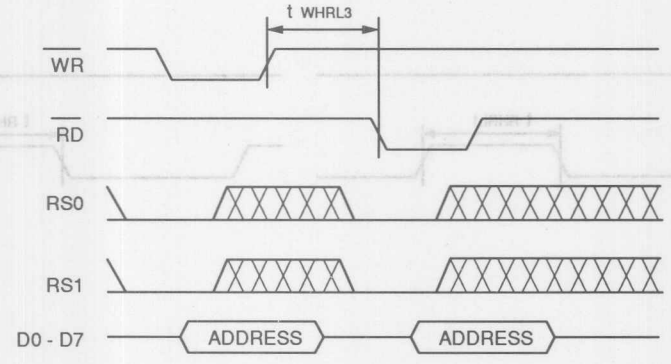


A.C. Waveforms for Color Value Read

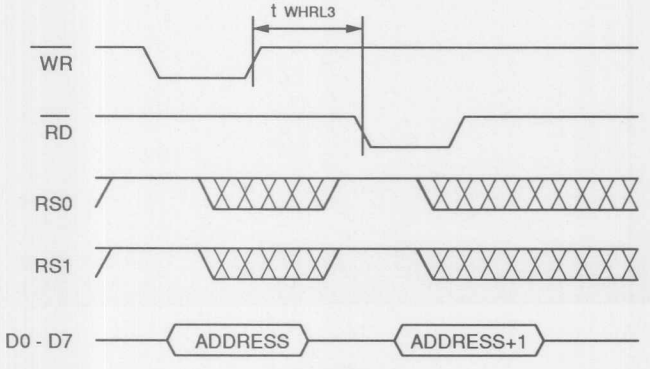
Followed by Pixel Address (Read Mode) Read



A.C. Waveforms for Pixel Address (Write Mode) Write and Read Back

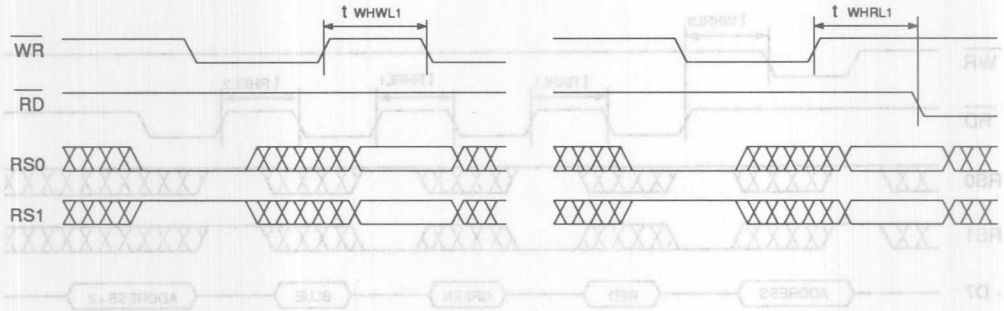


A.C. Waveforms for Pixel Address (Read Mode) Write and Read Back



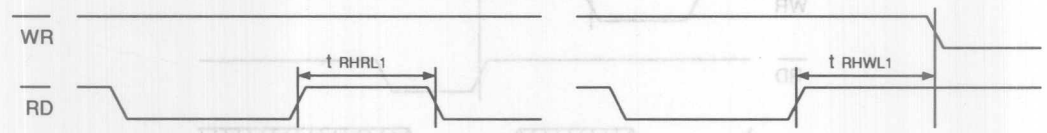
11

A.C Waveforms for Pixel Mask Write Followed by Any Write or Read



A.C. Waveforms for Pixel Mask or Pixel Address Read

Followed by Any Read or Write



Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
50	±10%	AT76C176A-50PC AT76C176A1-50JC AT76C176A2-50JC	28P6 32J 44J	Commercial (0°C to 70°C)
		AT76C176A-50PI AT76C176A1-50JI AT76C176A2-50JI	28P6 32J 44J	Industrial (-40°C to 85°C)
50	±5%	AT76C176A-50DMB AT76C176A-50LMB	28D6 32L	Military (-55°C to 125°C)
66	±10%	AT76C176A-66PC AT76C176A1-66JC AT76C176A2-66JC	28P6 32J 44J	Commercial (0°C to 70°C)
		AT76C176A-66PI AT76C176A1-66JI AT76C176A2-66JI	28P6 32J 44J	Industrial (-40°C to 85°C)
66	±5%	AT76C176A-66DMB AT76C176A-66LMB	28D6 32L	Military (-55°C to 125°C)
80	±10%	AT76C176A-80PC AT76C176A1-80JC AT76C176A2-80JC	28P6 32J 44J	Commercial (0°C to 70°C)
		AT76C176A-80PI AT76C176A1-80JI AT76C176A2-80JI	28P6 32J 44J	Industrial (-40°C to 85°C)
110	±5%	AT76C176A-11PC AT76C176A1-11JC AT76C176A2-11JC	28P6 32J 44J	Commercial (0°C to 70°C)

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
44J	44 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
50	±10%	AT76C1764-50PC AT76C1764A-50JC AT76C1764AZ-50JC	28P6 32J 44J	Commercial (0°C to 70°C)
		AT76C1764-50PI AT76C1764A-50JI AT76C1764AZ-50JI	28P6 32J 44J	Industrial (-40°C to 85°C)
50	±5%	AT76C1764-50DMB AT76C1764A-50LMB	28D6 32L	Military (-55°C to 125°C)
66	±10%	AT76C1764-66PC AT76C1764A-66JC AT76C1764AZ-66JC	28P6 32J 44J	Commercial (0°C to 70°C)
		AT76C1764-66PI AT76C1764A-66JI AT76C1764AZ-66JI	28P6 32J 44J	Industrial (-40°C to 85°C)
66	±5%	AT76C1764-66DMB AT76C1764A-66LMB	28D6 32L	Military (-55°C to 125°C)
80	±10%	AT76C1764-80PC AT76C1764A-80JC AT76C1764AZ-80JC	28P6 32J 44J	Commercial (0°C to 70°C)
		AT76C1764-80PI AT76C1764A-80JI AT76C1764AZ-80JI	28P6 32J 44J	Industrial (-40°C to 85°C)
110	±5%	AT76C1764A-11PC AT76C1764A-11JC AT76C1764AZ-11JC	28P6 32J 44J	Commercial (0°C to 70°C)

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
44J	44 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)

Interfacing the AT76C10/E to a Microcontroller

CMOS Programmable Amplifier Delay Equalizer

Application Note

Introduction

The AT76C10/E is a programmable gain amplifier integrated with a programmable telephone line group delay equalizer on a single chip. Its serial interface enables it to be packaged in an economical and space-saving 16-pin DIP. The AT76C10/E is especially suited for modems and data communications equipment where it can compensate for line gain variations and group delay distortions. In the E^2PROM version of the chip, the AT76C10E, a particular gain or delay configuration can be stored in the device's nonvolatile memory and recalled later by the user.

The programmable gain and group delay responses are controlled and configured by a serial seven-bit configuration code. The purpose of this application note is to illustrate how this serial configuration can be accomplished in a microcomputer environment, more specifically, utilizing a microcontroller (the Intel 8031AH) to interface to the AT76C10/E. Such an interface enables the gain and delay responses to be changed or updated in real-time (for the AT76C10) as well as saved into the E^2PROM (for the AT76C10E).

As shown in Figure 1, the Intel 8031AH, an eight-bit latch, a transmission line receiver, and external memory form a complete and versatile system to generate control and data bits for the AT76C10/E. An RS-232C cable can connect this system to the serial port of a microcomputer (e.g. IBM PC) or TTY terminal. The serial port transmits data to the microcontroller, which, under software control, outputs them as serial bits to the AT76C10/E for controlling the gain and delay outputs as desired by the user. As will be explained, an evaluation board implementing the system just described has been developed by Atmel Corporation following the guidelines in this application note.

The Hardware

The 8031AH has four eight-bit I/O ports: P0, P1, P2, and P3. Ports P0 and P2, however, are used for external memory addressing when external memory is present (as is the case here) and are thus unavailable as general-purpose I/O ports. This leaves all of the eight bits of port P1 and five bits of port P3 available for I/O. P1.0, P1.1, and P1.2, are used to produce respectively, via software instructions, the signals $\overline{CS}$, $\overline{WE}$, and DIN necessary to program the AT76C10/E.

The eight-bit latch acts as the low-order address latch/data buffer for the signals between the P0 I/O port of the microcontroller and the external memory. The line receiver enables the microcontroller to receive data signals from the microcomputer or TTY terminal via the RS-232C link.

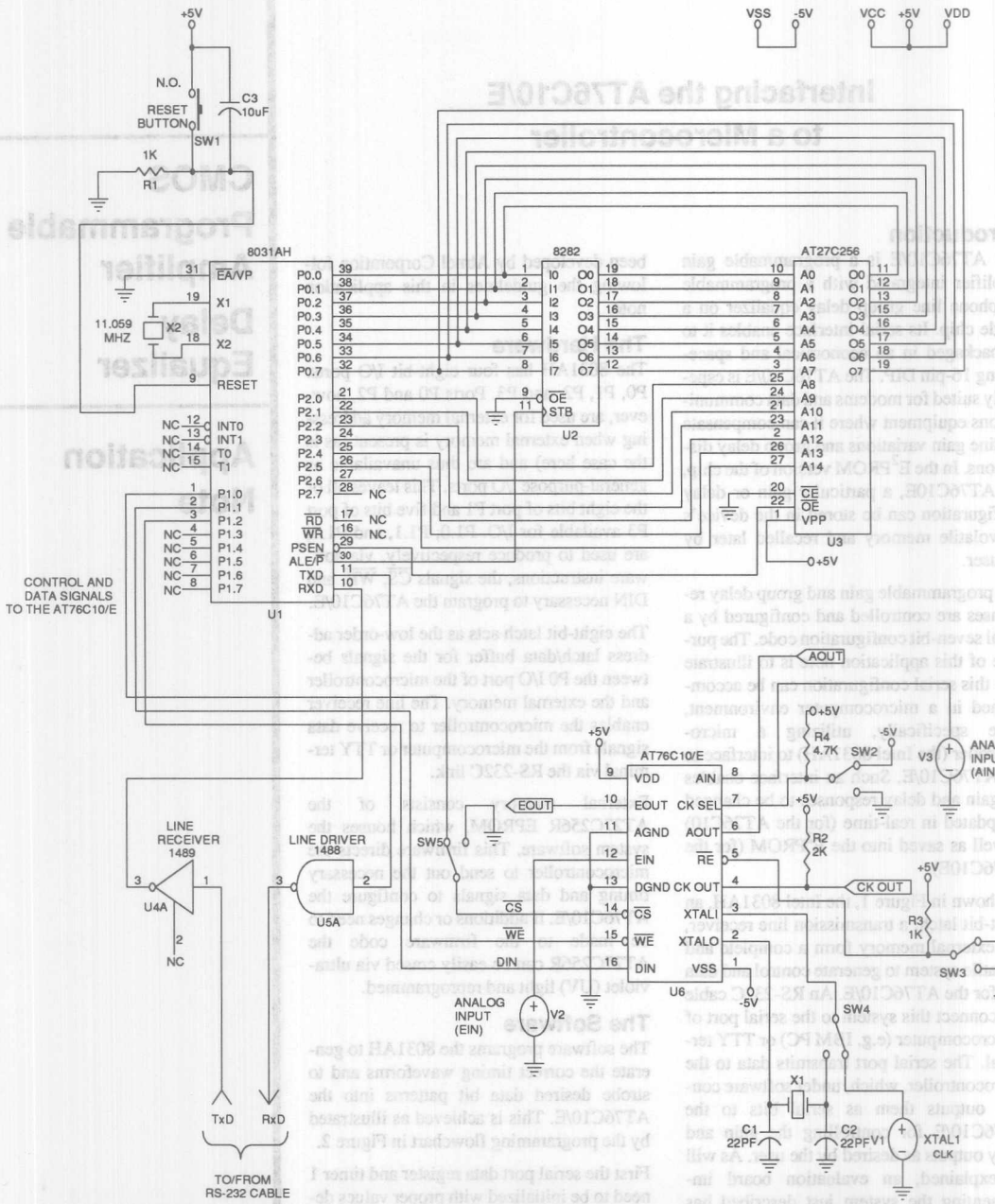
External memory consists of the AT27C256R EPROM, which houses the system software. This firmware directs the microcontroller to send out the necessary timing and data signals to configure the AT76C10/E. If additions or changes need to be made to the firmware code the AT27C256R can be easily erased via ultraviolet (UV) light and reprogrammed.

The Software

The software programs the 8031AH to generate the correct timing waveforms and to strobe desired data bit patterns into the AT76C10/E. This is achieved as illustrated by the programming flowchart in Figure 2.

First the serial port data register and timer 1 need to be initialized with proper values de-

Figure 1. Microcontroller Interface to the AT76C10/E



The Software (Continued)

pending on desired transmission parameters and baud rate. A 9600-baud data transmission rate has been used in this application. As soon as the accumulator receives a character from the keyboard the data is sent out bit-by-bit (LSB first) as data bits through the carry flag to the serial data input pin of the AT76C10/E. Appropriate delays and specific bit-manipulating instructions then control and synchronize the transitions of $\overline{CS}$ and $\overline{WE}$ with the data bits so that the writing waveforms conform to timing specifications defined in the device data sheet. Seven rising edges of $\overline{WE}$ strobe in a complete data word in a single write cycle.

The complete programming code is given in Figure 3. It directly implements the flowchart in Figure 2.

Using The AT76C10/E Evaluation Board

As previously mentioned, an evaluation board integrating the hardware and software subsystems covered in this application note is available from Atmel Corporation. This board includes a 5.25" disk (IBM-PC format) with gain/delay programming menus and is designed to enable the user to quickly and easily evaluate the functionality and performance of the AT76C10/E through a standard serial interface to an IBM PC or compatible computer. Through the board one can cycle through all the individual gain/delay steps in each of the two amplifiers and the group delay equalizer.

Figure 2. 8031 Programming Algorithm

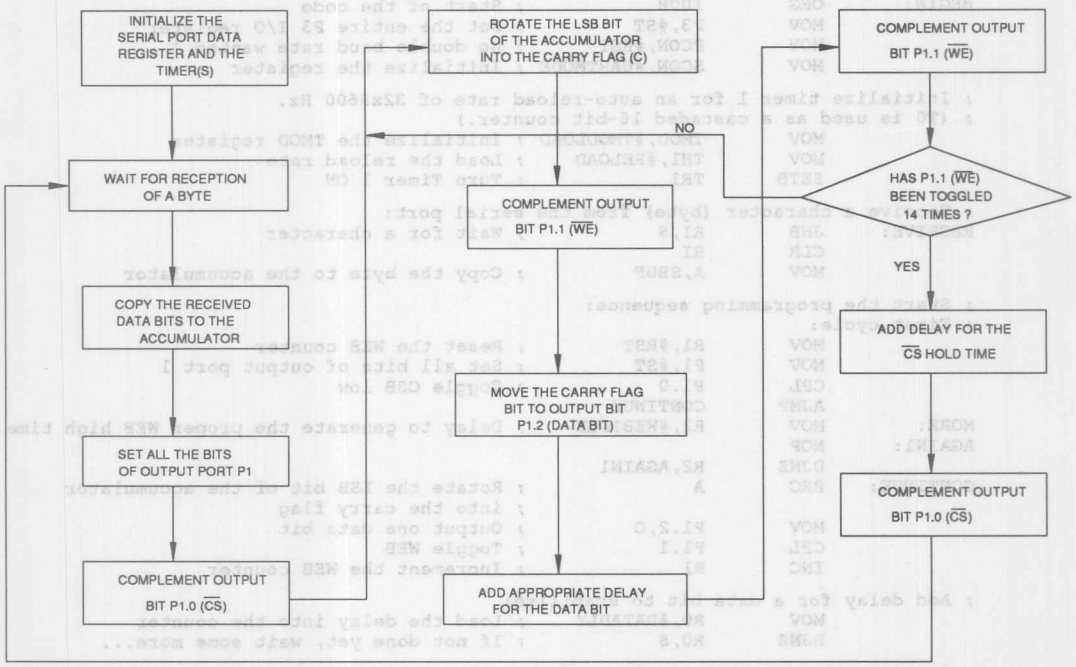


Figure 3. Program Code for AT76C10/E

```
;*************************************************************
;*                  8031 program for the AT76C10/E           *
;*                  Evaluation Board                         *
;*                                                           *
;*            Written by: Ta Wei (David) Lee                 *
;*          (C) 1988  ATMEL Corporation                      *
;*************************************************************
; 8031 control program for programming the AT76C10/E

; Constant Definitions:
ST          EQU     0FFH
RST         EQU     00H
DONE        EQU     14              ; 14 edges (falling and rising) for WEB
UARTMODE    EQU     01010000B       ; Set UART for: start, 8 data bits, stop
TMODLOAD    EQU     00100001B       ; Initialization word for the TMOD register
PCON        EQU     87H             ; Power Control Register
RELOAD      EQU     -3              ; Reload rate for 9600 baud
DATADLY     EQU     3H              ; Delay for a valid data bit
CSBHDLY     EQU     4H              ; Delay for CSB hold time
CSBIDLE     EQU     2               ; Delay before starting another CSB cycle
WEBIDLE     EQU     1               ; Delay before starting another WEB cycle

; Start of the program:
START:      ORG     00H
            LJMP    BEGIN

; Initialize the serial port data register for 8-bit UART mode:
BEGIN:      ORG     100H            ; Start of the code
            MOV     P3,#ST          ; Set the entire P3 I/O register
            MOV     PCON,#RST       ; No double baud rate wanted !
            MOV     SCON,#UARTMODE  ; Initialize the register

; Initialize timer 1 for an auto-reload rate of 32x9600 Hz.
; (T0 is used as a cascaded 16-bit counter.)
            MOV     TMOD,#TMODLOAD  ; Initialize the TMOD register
            MOV     TH1,#RELOAD     ; Load the reload rate
            SETB    TR1             ; Turn Timer 1 ON

; Receive a character (byte) from the serial port:
RECEIVE:    JNB     RI,$            ; Wait for a character
            CLR     RI
            MOV     A,SBUF          ; Copy the byte to the accumulator

; Start the programming sequence:
; First cycle:
            MOV     R1,#RST         ; Reset the WEB counter
            MOV     P1,#ST          ; Set all bits of output port 1
            CPL     P1.0            ; Toggle CSB low
            AJMP    CONTINUE
MORE:       MOV     R2,#WEBIDLE     ; Delay to generate the proper WEB high time
AGAIN1:     NOP
            DJNZ    R2,AGAIN1
CONTINUE:   RRC     A               ; Rotate the LSB bit of the accumulator
                                    ; into the carry flag
            MOV     P1.2,C          ; Output one data bit
            CPL     P1.1            ; Toggle WEB
            INC     R1              ; Increment the WEB counter

; Add delay for a data bit to stabilize:
            MOV     R0,#DATADLY     ; Load the delay into the counter
            DJNZ    R0,$            ; If not done yet, wait some more...

; Continue the data bit strobe cycle:
            CPL     P1.1            ; Toggle WEB
            INC     R1              ; Increment the WEB counter
            CJNE    R1,#DONE,MORE   ; Have 7 data bits been strobed in ?

; Add delay for the CSB hold time:
            MOV     R0,#CSBHDLY     ; Load the delay for TCH
            DJNZ    R0,$            ; Delay finished ?
```

A/D Conversion Using the AT76C120

How the AT76C120 Works

The AT76C120 simultaneously samples and holds both analog inputs, ADIN1 (Channel-1) and ADIN2 (Channel-2), once every CONV period. The AT76C120 then performs an A/D conversion of both samples and returns the two resulting 16-bit or 18-bit 2's complement codes at the serial data output pin DOUT during the following CONV clock period.

Selecting Which Channel's Data Comes Out First

Channel-1 output data will be returned first, during CONV "low" (and Channel-2 data will be returned second, during CONV "high") when a logic "1" is present at the input SEL1. Conversely, a logic "0" at the input SEL1 will cause Channel-2 data to be returned first, during CONV "low" (and CHANNEL-1 data to be returned second, during CONV "high").

Required Clocking for the AT76C120

The AT76C120 requires two clocks, SCLK and CONV, for proper operation:

- SCLK is the system clock and can have a maximum frequency of 6.144 MHz. It takes 64 SCLK cycles for the AT76C120 to perform one A/D conversion, and 64 more SCLK cycles for the digital data to be output (while a new sample is being converted).
- CONV is the convert clock, and its period corresponds to one A/D conversion. It should equal 64 SCLK cycles. Normally, CONV is derived from SCLK using a negative-edge triggered divide-by-64 counter, and both SCLK and CONV run continuously. In this mode, the AT76C120 will be sampling continuously at frequencies up to 96 kHz. Since CONV initiates conversions, however, it is possible to use CONV as a trigger for one-shot sampling.

Using the AT76C120 A/D Converter in One-Shot Mode

The AT76C120 can be used in a single-shot mode for acquiring data. To get one sample from each of the two channels, you need one conversion cycle to sample and convert the ADIN1 and ADIN2 inputs, and another conversion cycle to clock out both Channel 1 and Channel 2 digital codes. A total of two CONV periods and 128 SCLK cycles are required.

To use the AT76C120 in single-channel single-shot mode, you need one conversion cycle to sample and convert the ADIN1 or ADIN2 inputs, and another half cycle to clock out the Channel 1 or Channel 2 digital code. Only 1.5 CONV periods, and 96 SCLK periods are required.

One-shot sampling can be implemented by holding CONV low until a sample is desired. Note that while waiting to sample, SCLK can be either running or stopped. When a sample is desired, both SCLK and CONV are brought high, initiating a sample-and-hold of the analog inputs. SCLK should be clocked 32 times, at which point CONV is brought low. SCLK should then be clocked 32 more times, completing the first conversion cycle. CONV should then be brought high, and SCLK should be clocked 32 times, shifting out the first channel's digital code. For single-channel sampling, this would be the end and CONV should once again be brought low until a new sample is desired, and the process is repeated. For dual-channel sampling, CONV should be brought low, and SCLK should be clocked 32 more times, shifting out the second channel's digital code, and completing the second conversion cycle. CONV should be held low until a new sample is desired, at which time the process repeats.

Analog Interface

Due to the high sampling rate of the AT76C120, little if any anti-alias filtering is required for most industrial applications. For high performance Digital Audio applications, external Anti-Alias Lowpass or Bandpass Filters, shown as AAFs in the Sample Connection Diagram (Figure 1), should be used to eliminate signals outside the desired passband. Low noise op amps with low output impedance such as the OP27 should also be used to supply the analog inputs.

Digital Interface

The AT76C120 uses a single multiplexed serial data output pin, DOUT. CH-1 and CH-2 data bits are synchronized with SCLK, and are available during either the "high" or the "low" period of CONV. CONV, if equal to SCLK divided by 64, makes a transition from "high" to "low" or vice versa after the LSB is shifted out of DOUT. This allows the serial data to be latched easily into most popular D/A converters or digital signal processors by using CONV rising or falling edges. For applications with an 8-bit, 16-bit, or 32-bit host microprocessor, 16- or 18-bit wide parallel data may be desired, and serial-to-parallel conversion will be needed. In such cases, SCLK can be used to shift in the serial data from DOUT, and CONV can be used as a latch to output the parallel data.

More on Converting the Output Data from Serial to Parallel

It may be desirable to convert the AT76C120's serial data to parallel data. This may be achieved using 18 shift registers and 18 output latches, or several serial-to-parallel converters. Additionally, there may be a need to provide control signals to interface the parallel data with a microcontroller.

An easy way to integrate the entire serial-to-parallel conversion, complete with control signals for interface, is to use an Atmel ATV2500H Erasable Programmable Logic Device (EPLD). This device has the necessary I/O pins, logic terms, and registers to easily and conveniently interface the AT76C120 with most microcontrollers and DSP devices.

The ATV2500H is capable of latching in all 16/18 data bits that have been output serially from the AT76C120. All 16/18 bits can be presented in parallel on ATV2500H's output pins. Additionally, the ATV2500H can transfer this same data in eight-bit bytes, complete with handshaking, to a host device.

Power Supply Decoupling and Grounding

To obtain the highest performance possible with the AT76C120, critical signal paths, power supply lines, and ground planes on the circuit board should be laid out carefully to minimize noise coupling or aliasing into sensitive analog paths. As illustrated in the diagram showing a Sample Connection for Typical Applications (Figure 1), a separate AVCC line decoupled to AGND with a tantalum capacitor in parallel with a smaller ceramic chip capacitor should be used for the analog circuits on the AT76C120. Similarly, a separate analog ground return, AGND, which is connected to the most quiet point in the system ground plane, should be used.

For best results, four layer PC boards with separate ground and power supply planes are recommended. The AGND plane should be laid out as an island or tub underneath pins 1 to 6 and pins 19 to 24.

High frequency noise on the power and ground lines can be aliased into the passband by the sampling action of the AT76C120. If a switching power supply has to be used, both AVCC and AGND need to be isolated from the system supplies with inductors of appropriate values.

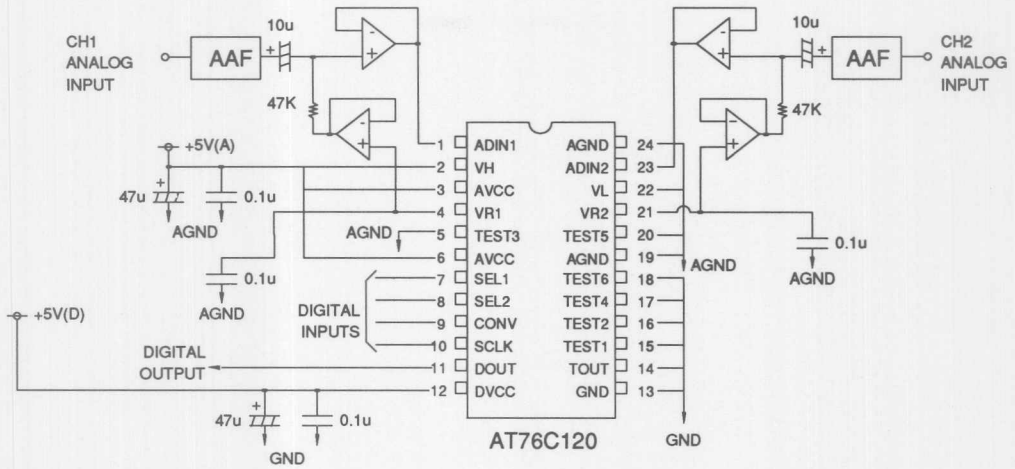
Evaluating the AT76C120 with the Atmel AT76C120 Demonstration Board

The AT76C120 dual-channel 16/18-bit A/D converter may be evaluated using the Atmel AT76C120 evaluation board (see Figure 2). This board can perform analog input signal conditioning, timing waveform generation, and serial-to-parallel data conversion. Evaluation requires a low-ripple, low-noise power supply, a low-distortion signal source, a clock source, and a digital signal processor.

The AT76C120 evaluation board requires a +15-volt and -15-volt analog power supply, and a +5-volt digital power supply. Voltage reference circuitry has already been included on the board. The user may build filters and buffers for the analog inputs in the analog patch area provided. The required clocking for the system may be generated using the SCLK BNC, or by inserting a clock oscillator in the socket provided. An Atmel ATV750 EPLD programmed as a divide-by-64 counter generates the convert clock CONV. An Atmel ATV2500 EPLD programmed as a serial-to-parallel converter places the 18-bit digital output codes from the AT76C120 at the pins of a 25-by-2 header. Because the ATV2500 is programmable, the digital interface may be modified by the user to meet specific interfacing needs, including the ability to program in control and handshake signals to facilitate data transfer to a host processor.

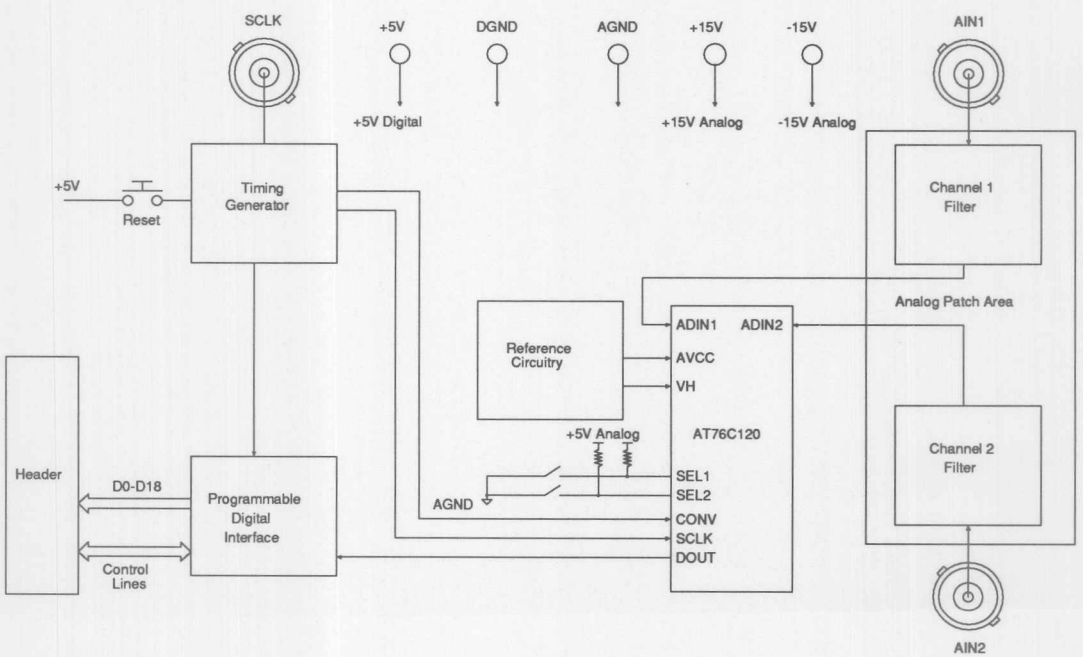
Dynamic evaluation of the AT76C120 is one application for the AT76C120 evaluation board. After building the appropriate filters in the analog patch areas, a spectrally pure sinusoid may be applied to the analog inputs of the AT76C120. Consecutive data samples may be collected as they appear at the header, and FFT may be performed to produce spectral information on the converter, such as signal-to-noise and signal-to-distortion ratios.

Figure 1. Sample Connection for Typical Application



Notes: 1. AVCC, AGND, +5V (A)- analog supply
2. DVCC, GND, +5V (D)- digital supply
3. Use high quality 0.1-µF ceramic chip capacitors

Figure 2. AT76C120 Evaluation Board



AT76C176A Color Palette DAC

110 MHz Monolithic CMOS Hi-Res Video Color Palette

Application Note

The Atmel family of six-bit video color palette (color look-up table) devices include the AT76C176A (28-pin), the AT76C176A1 (32-pin), and the AT76C176A2 (44-pin). They are designed for the IBM VGA 8514/A, XGA graphics standards and beyond. The VGA standard is already well supported by the software industry, but there are significant applications developing beyond standard VGA requiring higher resolutions. The Atmel devices can meet this emerging need. This application note will explore features of this family's members which can be fully utilized by graphics hardware designers and systems designers for implementing high-performance graphics solutions. It will also examine some design-related issues concerning such implementations.

SPEED: The AT76C176A/A1/A2 are available in these different speeds: 50 MHz, 66 MHz, 80 MHz, 110 MHz and 135 MHz. The speed refers to the maximum pixel clock frequency at which the device can be driven. Basically, the higher this frequency the greater the number of pixels that can be displayed on a CRT (cathode-ray tube) screen for bit-mapped graphics.

The equation used to calculate the color palette pixel clock rate required for a particular range of display resolution is as follows:

PCLK = 1.35 (HORIZONTAL RESOLUTION × VERTICAL RESOLUTION × VERTICAL SCAN RATE)

The horizontal resolution means the horizontal number of pixels and the vertical resolution means the vertical number of pixels. The vertical scan rate term refers to the vertical video scanning frequency of CRT monitors, which can vary between 43 Hz and 72 Hz but is typically 60 Hz, while the 35% factor refers to the portion of each frame time taken up by the horizontal and vertical retrace. For interlaced displays the vertical scanning rate becomes 43 Hz instead of 60 Hz. This means the screen image would be refreshed 43 times a second.

For example, if a non-interlaced resolution of 1024 x 768 refreshed at 60 Hz is desired, the required pixel clock rate would be:

$$PCLK = 1.35\ (1024 \times 768 \times 60) = 63.7\ MHz$$

To appreciate the magnitude of these frequencies, one must look at the graphical applications which these devices are capable of displaying. Standard VGA specifies resolution modes such as 320 x 200 pixels with 256 possible simultaneous colors and 640 x 480 pixels with 16 colors, whereas presently available Super-VGA (and VESA or Video Electronics Standards Association) specifications call for a standard resolution of 800 x 600 in 16 or 256 simultaneous colors. These colors are normally available from a total palette of 262,144 colors.

50 MHz: At this speed the color look-up table device can drive RGB monitors up to a maximum of 1024 x 768 pixels, 256 colors, in interlaced mode. At the time of this writing this is the typical maximum resolution displayable by some of the best selling Super-VGA and multisync-type monitors. At this device speed virtually all the requirements called for by the VGA and Super-VGA specifications can be met.

66 MHz: At this frequency the color palette can drive display monitors up to 1024 x 768 pixels, 256 colors, in non-interlaced mode. A non-interlaced monitor costs more than an interlaced monitor capable of the same resolution, but it can be more pleasing to the eye, since the screen "flicker" associated with interlaced monitors is eliminated. The "flashing" phenomenon present in interlaced monitors is due to the fact that only alternate scan lines are updated during every frame (vertical refresh), rather than every single scan line.

80 MHz: At this speed the top displayable resolution reaches 1024 x 960 pixels, 256 colors, in non-interlaced mode with a 60-Hz refresh rate, virtually approaching workstation-quality graphics. This speed is also suit-

able for driving 1024 x 768 non-interlaced monitors with a higher refresh rate of 72 Hz. At 72 Hz, screen flicker will not be detected even under fluorescent lighting conditions, which typically induce flicker perceptions. Mainstream personal computer software can be written to take advantage of these high resolutions with a resulting hardware / software cost-performance ratio several times less expensive than similar workstation solutions.

110 MHz: At this speed an eye-pleasing top resolution of 1280 x 1024 pixels (non-interlaced mode) can be achieved, with the device still capable of simultaneously displaying 256 different colors on-screen. This type of resolution, which even exceeds some workstation-level monitors, would be ideal for applications such as CAD drawings, computer modeling, scanned images, video animation, and imaging, with resulting photo-realistic images and shaded renderings. As a quick comparison, at 1280 x 1024 there are 1,310,720 pixels of information on-screen compared to 307,200 pixels at the normal 640 x 480 VGA resolution, which is a factor of four greater! With the rapidly emerging software markets of windows-based graphical user environments and multimedia applications for personal computers, the Atmel color palette devices providing such a high resolution would bring unprecedented workstation-grade graphics performance to personal computer users at an affordable cost.

135 MHz: Finally, this is the top speed available and is used for 1280 x 1024 pixels (non-interlaced mode) with a refresh rate of 72 Hz. The combination of such high on-screen resolution with a high speed refresh rate provides a superior level of performance under the harshest conditions.

POWER SAVINGS: In the PLCC and LCC versions of the AT76C176A family there is a power-down mode, an especially useful feature in laptop and notebook computers. When activated by software, this mode turns off the video DACs and the internal clock circuitry of the device, causing total device current consumption to be dramatically reduced from its normal operating value. The power-down mode will afford a battery-operated system a much longer per-charge life, since current consumption can drop to as low as 100 µA, compared to 150 mA or more in active mode.

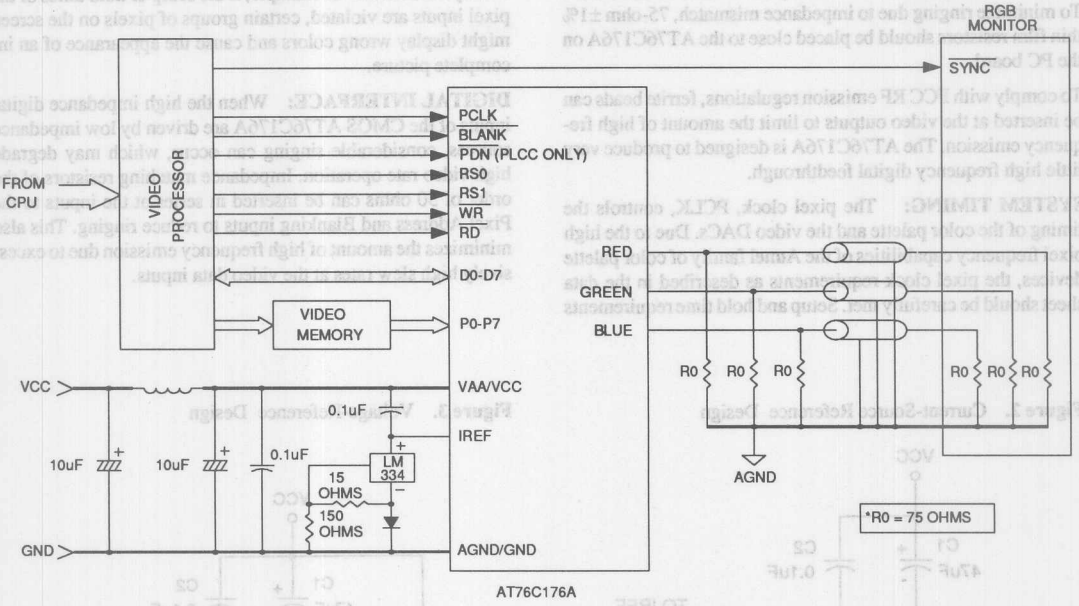
MILITARY APPLICATIONS: All the members of the AT76C176A family are processed up to full military specifications. This leads to consistent high reliability and quality. It also means that many previously expensive, proprietary military graphics subsystem designs can be easily upgraded to a cost-effective graphics solution supported by a wide array of standard off-the-shelf software written for the VGA standard. For example, military situational and awareness displays can be directly driven by Atmel color palette devices. The use of colors can dramatically add more meaningful information to the operators and users of visual equipment in the areas of avionics, logistics, radar and sonar systems, satellite communication, tactical warfare, and many others. Even if only a single primary color is used (e.g. GREEN) different shading levels could relay different objects very effectively.

RANGE OF COLORS: As discussed in the speed section, the Atmel color palette devices can simultaneously display a maximum of 256 distinct colors on-screen *throughout* their speed range. This means eight bits are allowed to define the color of each pixel. These 256 colors are available at any time from a total group of 262,144 colors. The specific set of 256 colors shown at any given instant can be easily changed through software. For most personal computer-based applications software, the availability of eight bits per pixel and 262,144 colors to choose from is more than adequate.

PACKAGING: The AT76C176A1 and the AT76C176A2 are the 32-pin and 44-pin PLCC versions of the AT76C176A, respectively. These packages are specially suited for the latest surface-mounted PCB manufacturing techniques and can significantly decrease the amount of real estate space required to implement an efficient graphics solution. Furthermore, these PLCC packages, with very short pins, can minimize the inductance inherently present in integrated circuit device pins, leading to sharper reproduction of colors with less distortion in analog displays. Other packaging such as LCC are also available.

The next section highlights design issues relevant to system and graphics subsystem designers. Also shown is a sample connection for the Atmel color palette in a typical design.

Figure 1. Sample Connection for Typical Application



System Implementation Considerations

POWER SUPPLY DECOUPLING AND GROUNDING: To obtain the cleanest possible analog outputs from the AT76C176A, digital noise coupling into the analog signal paths needs to be minimized. The video data paths, power supply lines and ground planes on the circuit board should be laid out carefully to reduce noise coupling. As illustrated in Figure 1 showing a sample connection for typical application, a separate VAA line decoupled to AGND with an electrolytic capacitor in parallel with a smaller ceramic chip capacitor should be used for the analog circuits on the AT76C176A. Similarly, a separate analog ground return, AGND, which is connected to the lowest impedance point in the system ground plane, should be used.

LAYOUT: For best results, four layer PC boards with separate ground and power supply planes are recommended. The AGND plane should be laid out as an island or tub underneath the AT76C176A. All video frequency signal traces should be kept as short as possible to minimize radiation and all decoupling capacitors should be placed as close to the AT76C176A as the layout rules permit.

Noise and transients on the power and ground lines can be coupled or aliased into the video circuits by the switching action of the AT76C176A. For applications at 66 MHz and above, it may be necessary to isolate both VAA and AGND from the system supplies with inductors of appropriate values.

CURRENT REFERENCE: The IREF pin in the Atmel devices determines the maximum full scale output of the video DACs and is designed to source current with reference to the positive supply rail. The required current to produce a 0.7-volt DAC full-scale output level into a doubly-terminated 75-ohm load, as specified in the data sheet, is -8.88 mA. In order to generate this current reference two approaches are suggested here: a current-source design and a voltage-reference design.

As shown in Figure 2, the first approach is based on the LM334Z adjustable current source device. In this design the LM334Z is operated in its zero temperature coefficient mode, resistor RSET determines the reference current drawn from the color palette, and resistor R1 and the silicon diode provide compensation against temperature variations. Decoupling capacitors C1 and C2 are recommended for avoiding changes in the current reference due to possible VCC or VAA variations within the operating frequency bandwidth. RSET should be a precision resistor, preferably with a 1% tolerance.

Figure 3 illustrates the voltage-reference approach. The use of a TL431C precision voltage regulator or an equivalent device is recommended. In this design the TL431C acts as a shunt regulator to provide a constant current sink. RSET again determines the amount of current drawn from the Atmel part and should be a precision resistor, while R1 limits the current flowing into the cathode terminal of the TL431C.

VIDEO INTERFACE: The RED, GREEN and BLUE video outputs are designed to drive doubly terminated 75-ohm lines. To minimize ringing due to impedance mismatch, 75-ohm ±1% thin film resistors should be placed close to the AT76C176A on the PC board.

To comply with FCC RF emission regulations, ferrite beads can be inserted at the video outputs to limit the amount of high frequency emission. The AT76C176A is designed to produce very little high frequency digital feedthrough.

SYSTEM TIMING: The pixel clock, PCLK, controls the timing of the color palette and the video DACs. Due to the high pixel frequency capabilities of the Atmel family of color palette devices, the pixel clock requirements as described in the data sheet should be carefully met. Setup and hold time requirements with respect to PCLK and duty cycle limits for PCLK should be strictly adhered to. For example, if the setup or hold times of the pixel inputs are violated, certain groups of pixels on the screen might display wrong colors and cause the appearance of an incomplete picture.

DIGITAL INTERFACE: When the high impedance digital inputs of the CMOS AT76C176A are driven by low impedance sources, considerable ringing can occur, which may degrade high video rate operation. Impedance matching resistors of the order of 50 ohms can be inserted in series at the inputs to the Pixel Address and Blanking inputs to reduce ringing. This also minimizes the amount of high frequency emission due to excessively high slew rates at the video data inputs.

Figure 2. Current-Source Reference Design

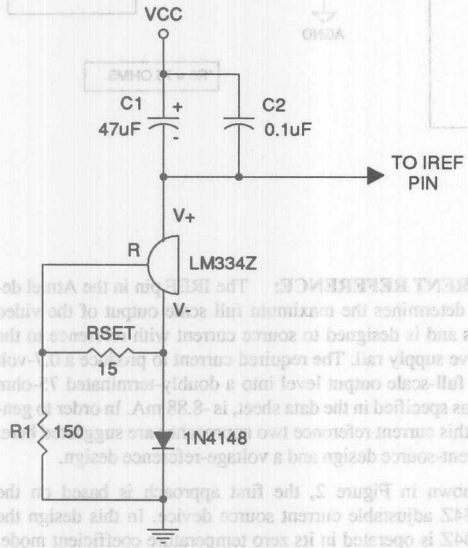
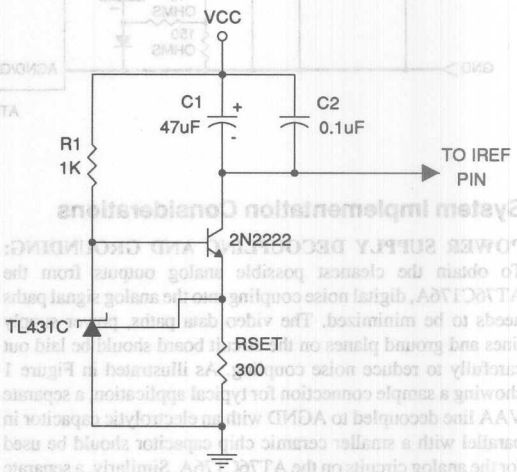


Figure 3. Voltage-Reference Design



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Contents

Section 12

CMOS Microcontroller

AT89C51 4K x 8 80C31 Microcontroller with 4K Bytes Flash 12-3

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Features

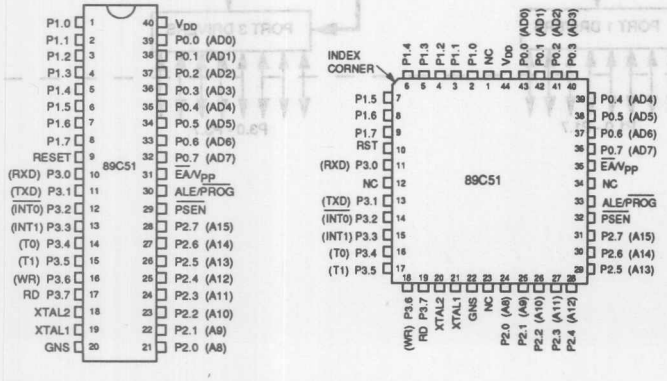
- Compatible with MCS-51[1] Products
- 4K Bytes of In-Circuit Re-Programmable Flash Memory
  - Endurance: 1000 Write/Erase Cycles
  - Data Retention: 10 Years
- Wide Operating Voltage Range: V_{CC} = 2.7V to 6V
- Fully Static Operation: 0 Hz to 16 MHz
- 3-Level Program Memory Lock
- 128 x 8-Bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-Bit Timer/Counters
- 5 Interrupt Sources
- Programmable Serial Channel
- Low Power Idle and Power Down Modes

Description

The AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4K Bytes of Flash Programmable and Erasable Read Only Memory (PEROM). The device is manufactured using Atmel's high density nonvolatile memory technology and is compatible with the industry standard 80C51 instruction set and pinout. The on-chip PEROM allows the program memory to be reprogrammed in-circuit or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with PEROM on a monolithic chip, the Atmel AT89C51 is a powerful microcomputer which provides a highly flexible and cost effective solution to many embedded control applications.

The AT89C51 provides the following standard features: 4K Bytes of PEROM, 128 bytes of RAM, 32 I/O lines, two 16-bit timer/counters, a five source two-level interrupt architecture, a full duplex serial port, on-chip oscillator and clock circuitry. The AT89C51 supplies all the necessary timing and high-voltage functions required for programming the PEROM array, and no external support circuits are required.

Pin Out



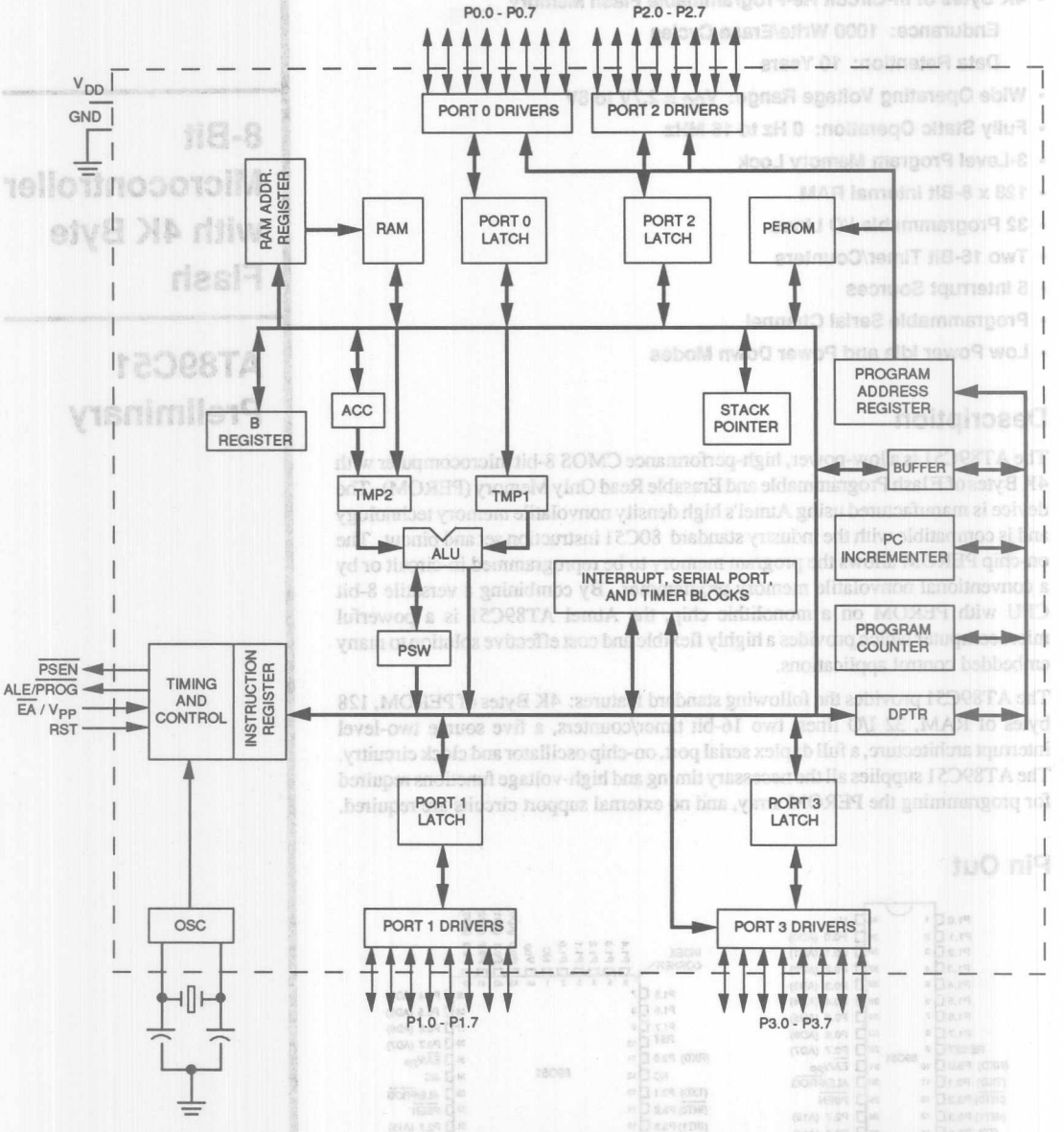
(1) MCS-51 is a registered trademark of Intel Corporation.

8-Bit Microcontroller with 4K Byte Flash

AT89C51 Preliminary

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AT89C51 Block Diagram



In addition, the AT89C51 supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The Power Down Mode saves the RAM contents but freezes the oscillator disabling all other chip functions until the next hardware reset.

Pin Description

V_{CC}: Supply voltage

V_{SS}: Ground

Port 0: Port 0 is an 8-bit open drain bidirectional I/O port. As an output port each pin can sink 8 TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1s.

Port 0 also receives the code bytes during PEROM programming, and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source 4 TTL inputs. When 1s are written to Port 1 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 1 also receives the low-order address bytes during PEROM programming and program verification.

Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source 4 TTL inputs. When 1s are written to Port 2 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1s. During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during PEROM programming and verification.

Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source 4 TTL inputs. When 1s are written to Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89C51 as listed below:

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	INT0 (external interrupt 0)
P3.3	INT1 (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	WR (external data memory write strobe)
P3.7	RD (external data memory read strobe)

Port 3 also receives some control signals for PEROM programming and programming verification.

RST: Reset Input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{PROG}$: Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during PEROM programming.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

$\overline{PSEN}$: Program Store Enable is the Read strobe to External Program Memory.

When the AT89C51 is executing code from external Program Memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to External Data Memory.

$\overline{EA}$/V_{PP}: External Access Enable. $\overline{EA}$ must be strapped to V_{SS} in order to enable the device to fetch code from External Program Memory locations starting at 0000H up to FFFFH. Note, however, that if either of the Lock Bits are programmed, $\overline{EA}$ will be internally latched on reset.

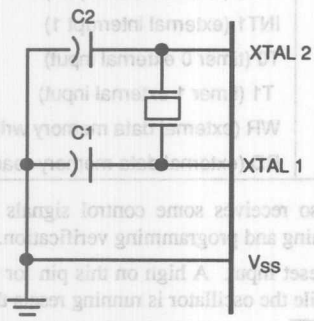
$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12 V programming enable voltage (V_{PP}) during PEROM programming, when 12 V programming is selected.

XTAL1: Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2: Output from the inverting oscillator amplifier.

Figure 1. Oscillator Connections



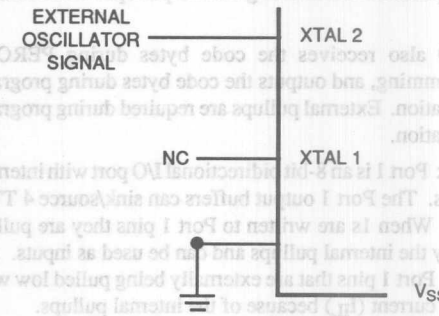
C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Oscillator Characteristics

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 1. Either a quartz crystal or ceramic resonator may be used.

To drive the device from an external clock source, XTAL1 should be grounded while XTAL2 is driven as shown in Figure 2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Figure 2. External Clock Drive Configuration



Idle Mode

In Idle Mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the Special Functions Registers remain unchanged during this mode as shown in the table below. The Idle Mode can be terminated by any enabled interrupt or by a hardware reset.

It should be noted that when Idle is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

Power Down Mode

In the Power Down mode the oscillator is stopped, and the instruction that invokes Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power Down mode is terminated.

The only exit from Power Down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Status of the External Pins During Idle and Power Down

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

Program Memory Lock Bits

On the chip are three Lock Bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the table below:

When Lock Bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value, and holds that value until reset is activated. It is necessary that the latched value of $\overline{EA}$ be in agreement with the current logic level at that pin in order for the device to function properly.

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Lock Bit Protection Modes

	Program Lock Bits			Protection Type
	LB1	LB2	LB3	
1	U	U	U	No program lock features enabled.
2	P	U	U	MOVC Instructions executed from external program memory are disabled from fetching code bytes from Internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the PEROM is disabled.
3	P	P	U	Same as mode 2, also verify is disabled.
4	P	P	P	Same as mode 3, also external execution is disabled.

Programming the PEROM

The AT89C51 is normally shipped with the on-chip PEROM code memory array in the erased state (i.e. contents=FFh) and ready to be programmed. The programming interface accepts either a High-Voltage (12V) or a Low-Voltage (V_{CC}) program enable signal. The Low Voltage programming mode provides a convenient way to program the AT89C51 inside the user's system. The High-Voltage programming mode is compatible with conventional third party PEROM or EPROM programmers. The AT89C51 is shipped with the High-Voltage programming mode selected.

The AT89C51 code memory array is programmed byte-by-byte in either programming modes. Before the on-chip PEROM Code Memory is re-programmed, the entire memory array can be erased electrically, even in the user's application system.Atmel can supply parts with factory programmed user code in the memory array.

Programming Algorithm: Before programming the AT89C51, the address, data and control signals should be set up according to the PEROM Programming Modes table and Figures 3 and 4. To program the AT89C51, the following sequence should be followed:

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12V if in the High-Voltage programming mode.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the PEROM array or the lock bits. The byte-write cycle is self-timed and takes no more than 0.5 ms.Repeat steps 1 through 5 changing the address and data for the entire array or until the end of the object file is reached.

Selecting V_{PP}: To program the V_{PP} select code, the ALE/$\overline{PROG}$ pin needs to be held low for 10 ms.

Data Polling: The AT89C51 features $\overline{Data}$ Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on PO.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{Data}$ Polling may begin any time after a write cycle has been initiated.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The lock bits cannot be verified directly. Verification of the lock bits is achieved by observing that their features are enabled.

Chip Erase: The entire PEROM array is erased electrically by using the proper combination of control signals and by holding ALE/$\overline{PROG}$ low for 10 ms. The code array is written with all "1"s in the Chip Erase operation and must be executed before the code memory can be re-programmed.

Reading the Signature Bytes: The Signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 need to be pulled to a logic low. The values returned are:

(030H) = 1EH indicates manufactured by Atmel

(031H) = 51H indicates 89C51

Programming Interface

Every code byte in the PEROM array can be written and the entire array can be erased by using the appropriate combination of control signals. The Write operation cycle is self-timed and once initiated, will automatically time itself to completion.

PEROM Programming Modes

MODE	RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/V_{PP}	P2.7	P2.6	P3.6	P3.7
Write Code Data	H	L	⎍	H/12V (1)	L	H	H	H
Read Code Data	H	L	⎍	H	L	L	H	H
Write V_{PP} Select Code (2)	H	L	⎍	12V	L	H	L	H
Write Lock Bit - 1	H	L	⎍	H/12V	H	H	H	H
Bit - 2	H	L	⎍	H/12V	H	H	L	L
Bit - 3	H	L	⎍	H/12V	H	L	H	L
Chip Erase	H	L	⎍	H/12V	H	L	L	L
Read Signal Byte	H	L	H	H	L	L	L	L

Notes:

(1) The V_{PP} Select Code determines whether $V_{PP} = 12V$ or $V_{PP} = V_{CC}$ is used to enable programming.

(2) Write data AAh to address 55h to select $V_{PP} = V_{CC}$.
Write data 55h to address AAh to select $V_{PP} = 12V$.

Figure 3. Programing the PEROM

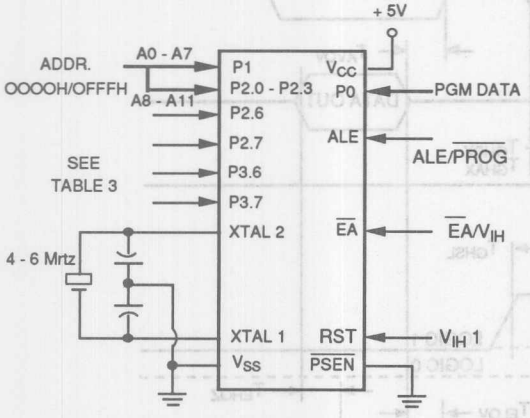
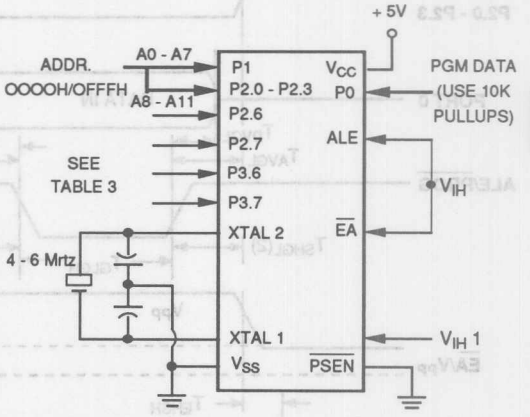


Figure 4. Verifying the PEROM



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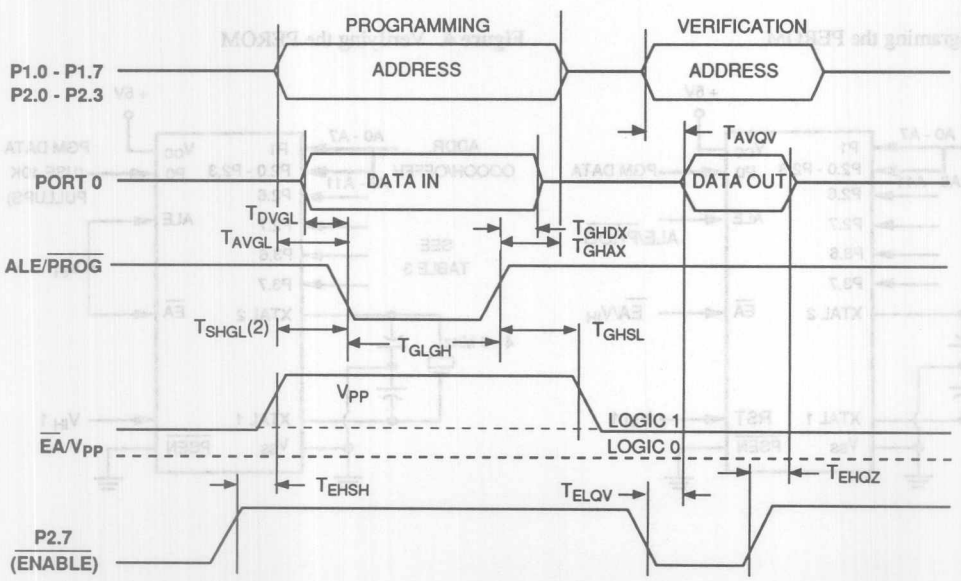
PEROM Programming and Verification Characteristics

T_{AI} = 21°C to 27°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0V

Symbol	Parameter	Min	Max	Units
V_{PP}[1]	Programming Supply Voltage	11.5	12.5	V
I_{PP}[1]	Programming Supply Current		1.0	mA
$1/T_{CLCL}$	Oscillator Frequency	4	6	MHz
T_{AVGL}	Address Setup to $\overline{PROG}$ Low	$48T_{CLCL}$		
T_{GHAX}	Address Hold After $\overline{PROG}$	$48T_{CLCL}$		
T_{DVGL}	Data Setup to $\overline{PROG}$ Low	$48T_{CLCL}$		
T_{GHDX}	Data Hold After $\overline{PROG}$	$48T_{CLCL}$		
T_{EHSH}	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48T_{CLCL}$		
T_{SHGL}[1]	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
T_{GHSL}	V_{PP} Hold After $\overline{PROG}$	10		µs
T_{GLGH}	$\overline{PROG}$ Width	90	110	µs
T_{AVQV}	Address to Data Valid		$48T_{CLCL}$	
T_{ELQV}	$\overline{ENABLE}$ Low to Data Valid		$48T_{CLCL}$	
T_{EHQZ}	Data Float After $\overline{ENABLE}$	0	$48T_{CLCL}$	

Note 1: Only used in 12 Volt programming mode.

PEROM Programming and Verification Waveforms



Note 2: For 12V programming only. For 5V programming, T_{SHEL} = 0.

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0 V to +7.0 V
Maximum Operating Voltage	6.6 V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_{AI} = -40°C to +85°C, V_{CC} = +2.7V to +6.0 V, T_{AC} = 0°C to +70°C, V_{CC} = +2.7V to +6.0 V (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{IL}	Input Low Voltage	(Except $\overline{EA}$)	–0.5		0.2 V_{CC} –0.1	V
V_{IL1}	Input Low Voltage ($\overline{EA}$)		–0.5		0.2 V_{CC} –0.3	V
V_{IH}	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9		V_{CC} + 0.5	V
V_{IH1}	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage(2)	I_{OL} = 1.6 mA			0.45	V
	(Ports 1,2,3)					
V_{OL1}	Output Low Voltage(2)	I_{OL} = 3.2 mA			0.45	V
	(Port 0, ALE,$\overline{PSEN}$)					
V_{OH}	Output High Voltage	I_{OH} = –60 µA V_{CC} = 5V ± 10%	2.4			V
	(Ports 1,2,3, ALE,$\overline{PSEN}$)	I_{OH} = –25 µA	0.75 V_{CC}			V
		I_{OH} = –10 µA	0.9 V_{CC}			V
V_{OH1}	Output High Voltage	I_{OH} = –800 µA V_{CC} = 5V ± 10%	2.4			V
	(Port 0 in External Bus	I_{OH} = –300 µA	0.75 V_{CC}			V
	Mode)	I_{OH} = –80 µA	0.9 V_{CC}			V
I_{IL}	Logical 0 Input Current	V_{IN} = 0.45V			–50	µA
	(Ports 1, 2, 3)					
I_{TL}	Logical 1 to 0 Transition	V_{IN} = 2V			–650	µA
	Current (Ports 1,2,3)					
I_{LI}	Input Leakage Current	0.45 < V_{IN} < V_{CC}			±10	µA
	(Port 0, $\overline{EA}$)					
RRST	Reset Pulldown Resistor		50		150	KΩ
C_{IO}	Pin Capacitance	Test Freq = 1 MHz, T_A = 25°C			10	pF
I_{CC}	Power Supply Current:					
	Active Mode, 12 MHz			11	20	mA
	Idle Mode, 12 MHz	(1)		1.7	5	mA
	Power Down Mode			5	50	mA

Notes: 1. Minimum V_{CC} for Power Down is 2V.

2. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:

Maximum I_{OL} per port pin: 10 mA

Maximum I_{OL} per 8-bit port-

Port 0: 26 mA

Ports1, 2, and 3: 15 mA

Maximum total I_{OL} for all output pins: 71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

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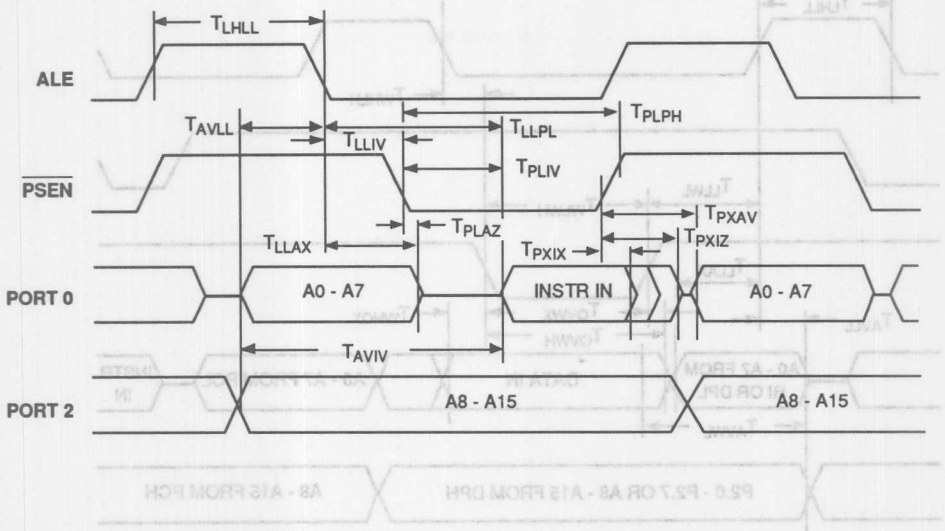
AC Characteristics

(Under Operating Conditions; Load Capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; Load Capacitance for all other outputs = 80 pF)

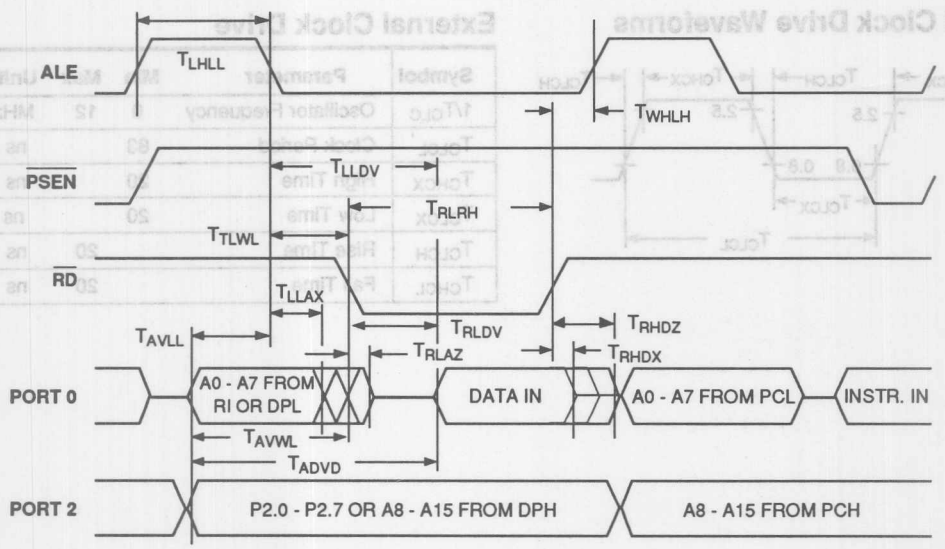
External Program Memory Characteristics

Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
$1/T_{CLCL}$	Oscillator Frequency			0	12.0	MHz
T_{LHLL}	ALE Pulse Width	127		$2T_{CLCL}-40$		ns
T_{AVLL}	Address Valid to ALE Low	43		$T_{CLCL}-40$		ns
T_{LLAX}	Address Hold After ALE Low	48		$T_{CLCL}-35$		ns
T_{LLIV}	ALE Low to Valid Instruction In		233		$4T_{CLCL}-100$	ns
T_{LLPL}	ALE Low to $\overline{PSEN}$ Low	58		$T_{CLCL}-25$		ns
T_{PLPH}	$\overline{PSEN}$ Pulse Width	215		$3T_{CLCL}-35$		ns
T_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		125		$3T_{CLCL}-20$	ns
T_{PXIX}	Input Instr Hold After $\overline{PSEN}$	0		0		ns
T_{PXIZ}	Input Instr Float After $\overline{PSEN}$		63		$T_{CLCL}-8$	ns
T_{PXAV}	$\overline{PSEN}$ to Address Valid	75		$T_{CLCL}-8$		ns
T_{AVIV}	Address to Valid Instruction In		302		$5T_{CLCL}-115$	ns
T_{PLAZ}	$\overline{PSEN}$ Low to Address Float		20		20	ns
T_{RLRH}	RD Pulse Width	400		$6T_{CLCL}-100$		ns
T_{WLWH}	WR Pulse Width	400		$6T_{CLCL}-100$		ns
T_{RLDV}	RD Low to Valid Data In		252		$5T_{CLCL}-165$	ns
T_{RHDX}	Data Hold After RD	0		0		ns
T_{RHDZ}	Data Float After RD		97		$2T_{CLCL}-70$	ns
T_{LLDV}	ALE Low to Valid Data In		517		$8T_{CLCL}-150$	ns
T_{AVDV}	Address to Valid Data In		585		$9T_{CLCL}-165$	ns
T_{LLWL}	ALE Low to RD or WR Low	200	300	$3T_{CLCL}-50$	$3T_{CLCL}-50$	ns
T_{AVWL}	Address to RD or WR Low	203		$4T_{CLCL}-130$		ns
T_{QVWX}	Data Valid to WR Transition	23		$T_{CLCL}-60$		ns
T_{QVWH}	Data Valid to WR High	433		$7T_{CLCL}-150$		ns
T_{WHQX}	Data Held After WR	33		$T_{CLCL}-50$		ns
T_{RLAZ}	RD Low to Address Float		0		0	ns
T_{WHLH}	RD or WR High to ALE High	43	123	$T_{CLCL}-40$	$T_{CLCL}+40$	ns

External Program Memory Read Cycle

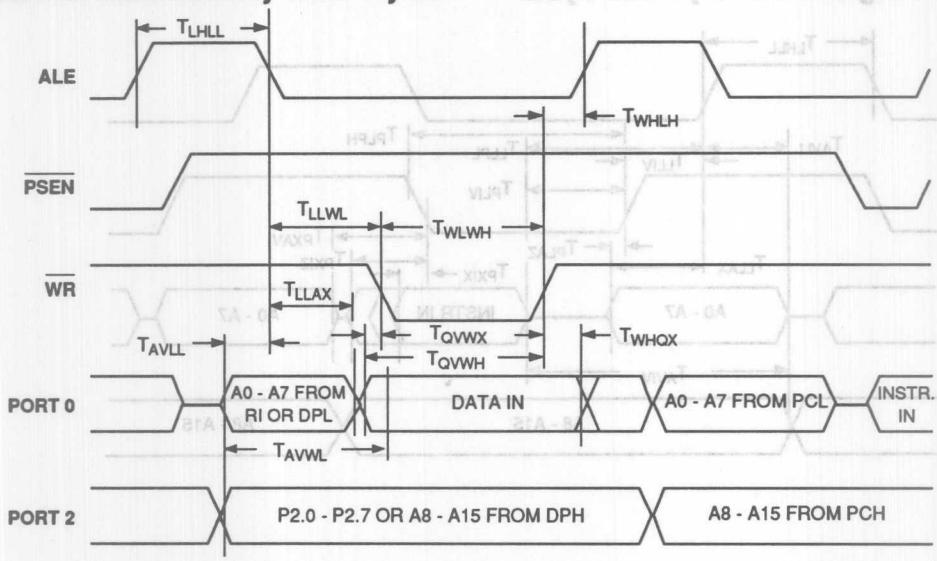


External Data Memory Read Cycle

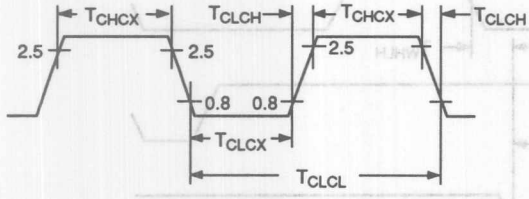


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External Data Memory Write Cycle



External Clock Drive Waveforms



External Clock Drive

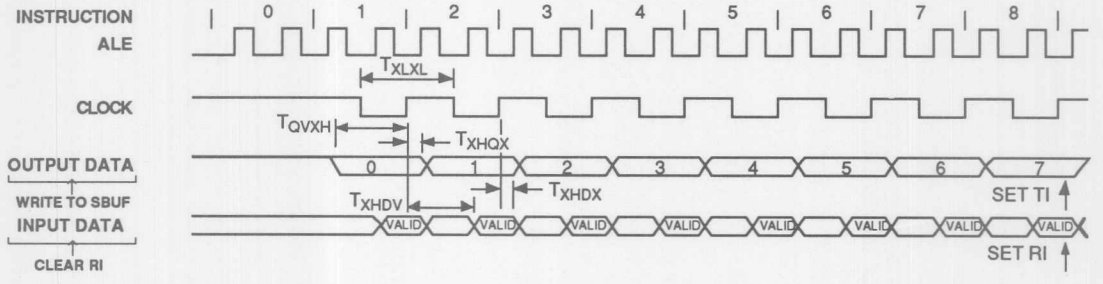
Symbol	Parameter	Min	Max	Units
$1/T_{CLC}$	Oscillator Frequency	0	12	MHz
T_{CLCL}	Clock Period	83		ns
T_{CHCX}	High Time	20		ns
T_{CLCX}	Low Time	20		ns
T_{CLCH}	Rise Time		20	ns
T_{CHCL}	Fall Time		20	ns

Serial Port Timing - Shift Register Mode Test Conditions

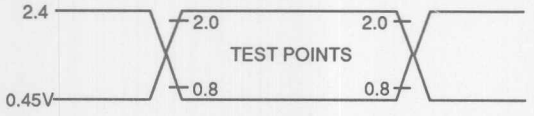
(T_{AI} = 0° = 70°C; V_{CC} - 5V ± 10%; V_{SS} = 0V; Load Capacitance = 80 pF)

Symbol	Parameter	12MHz Osc		Variable Osacillator		Units
		Min	Max	Min	Max	
T_{XLXL}	Serial Port Clock Cycle Time	1.0		$12T_{CLCL}$		µs
T_{QVXH}	Output Data Setup to Clock Rising Edge	700		$10T_{CLCL}$ - 133		ns
T_{XHQX}	Output Data Hold After Clock Rising Edge	50		$2T_{CLCL}$ - 117		ns
T_{XHDX}	Input Data Hold After	0		0		ns
T_{XHDV}	Clock Rising Edge to Input Data Valid		700		$10T_{CLCL}$ - 133	ns

Shift Register Mode Timing Waveforms



AC Testing Input/Output Waveforms



AC Inputs during testing are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

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Serial Port Timing - Shift Register Mode Test Conditions

(T_A = 0° - 70°C; V_{CC} - 5V ± 10%; V_{SS} = 0V; Load Capacitance = 80 pF)

Symbol	Parameter	12MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
T_{XLXL}	Serial Port Clock Cycle Time	1.0		12T_{CLCL}		µs
T_{QVXH}	Output Data Setup to Clock Rising Edge	700		10T_{CLCL} - 133		ns
T_{XHQX}	Output Data Hold After Clock Rising Edge	50		2T_{CLCL} - 117		ns
T_{XHDX}	Input Data Hold After	0		0		ns
T_{XHDV}	Clock Rising Edge to Input Data Valid		700		10T_{CLCL} - 133	ns

Shift Register Mode Timing Waveforms

AC Testing Input/Output Waveforms

AC inputs during testing are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

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Section 13

TAB Packaging Services

Wafer Bumping and Tape Automated Bonding Technology 13-3

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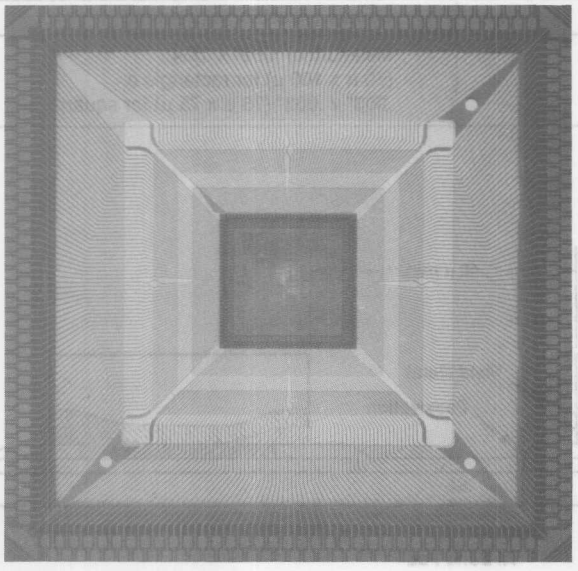
Features

- **Capability to .004" Pad Pitch with Gold Bumps**
- **Provides Known Good Die for Multichip Module Applications**
- **Smallest Footprint Available for a Fully Tested Device**
- **JEDEC Standard or Customer Specified TAB Tape**
- **Customer Specified Footprint for Flip TAB or Lead Formed Applications**
- **Superior Inductance, Resistance, and Capacitance Compared to Wire Bonding**

Description

Tape Automated Bonding (TAB) is a surface-mount packaging technology for integrated circuits which provides the highest lead density and smallest footprint available for fully-tested die. A pattern of leads is formed in a thin sheet of copper which allows chip contact on the inside of the pattern, and contact to external substrates at the lead terminations on the outside of the pattern.

The final configuration of the TAB'd die may conform to a JEDEC Standard UO-018 outline, or may be customized to the electrical and mechanical requirements of the customer, allowing unprecedented flexibility in finished product design.



Wafer Bumping and Tape Automated Bonding Technology

Wafer Bumping Services

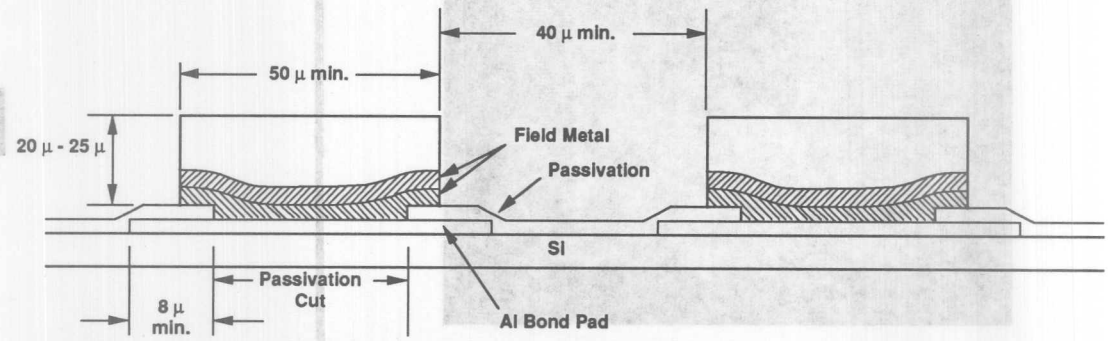
Gold bumps are plated to the bond pads of the die on an unprobed wafer (bumps must be applied in wafer form.) Wafers are readied for bumping according to Atmel's design rules for the size of the passivation opening over the bond pads. Titanium/Tungsten is sputtered on the wafer followed by layers of palladium and gold. Photolithography operations are performed to define the bump opening for plating. The bumps are then plated to the gold field metal on the bond pads. To complete the process, the photosensitive material and field metals are stripped, a final cleaning step is performed and the bumps are annealed.

Atmel's bump process is compatible with all types of wafer processes, including GaAs and SOS.

Gold Bump Capabilities	
Configuration	Straight Wall or Mushroom
Bump Height	20 - 25 µ
Bump Spacing	40 µ minimum for straight wall 100 µ minimum for mushroom
Field Metal	TiW/Pd/Au
Photolithography	Polyimide (straight wall) Aqueous Photoresist (mushroom)

Gold Bump Design Rules	
Passivation Opening Size	8 µ minimum from outside edge of bond pad
Passivation Opening Shape	Square or rectangle preferred
Size of Bump Opening on Bump Mask	Minimum of .002" x .004" (50 µ x 100 µ) for rectangle or .003" x .003" (75 µ x 75 µ) for square

Straight Wall Gold Bump



Bump Mask Requirements

Atmel Supplied Mask Requirements

GDS II tape of the mask layer for the bond pads
Die window size
Quantity of die per wafer
X and Y stepping distance (in mils or microns)
Pattern offshift distance (in mils or microns)
Information on test die

-If a test die is present on the wafer but will not be checked at probe, Atmel will procure a mask that will project a bump site of the subject device on the test die.

-If a test die is present and will be checked at wafer probe, required information includes a GDS II tape of the mask layer for the test die contacts, test die window size, and quantity of test die per wafer.

Customer Supplied Mask Requirements	
Orientation	Center of wafer pattern must be in the center of the mask pattern Mask title at top (device number, layer number, and revision) Wafer flat to top of mask with chrome side down
Mask Size	7" x 7" for 6" wafers, .120" thickness 6" x 6" for 5" wafers, .120" thickness 5" x 5" for 4" wafers, .090" thickness
Reticle Type	1X
Image Media	Anti-reflective (AR) for clear field See through chrome (STC) for dark field 0.8 to 1.0 optical density
Glass Type	Quartz
Defect Size	10 microns, no defects in die sites
CD or Registration	Not required, however alignment marks in the saw streets are recommended for critical alignment on fine pitch bumps (< .005")
Saw Streets	Saw streets should be clear of plating except for alignment marks
Location of Bump Openings	Over entire wafer surface (bond pads plus edge areas of bare silicon)

TAB Technology

After the integrated circuit is prepared for the TAB process by applying bumps to the bond pads, the wafer is probed with normal probe testing procedures. The wafer is then sawed, and the good die are inspected prior to presentation to the bonding process.

Inner Lead Bond (ILB) - To make the ILB connection, the TAB frame is attached to bumps formed on the chip in the wafer bumping process. ILB connections are affected via thermosonic single point bonding or thermocompression gang bonding. Single point bonding is typically employed for prototype, low volume production, and fine pitch/high pin count applications, and usually requires minimal tooling charges. The tape is presented to the bonding stage in singulated form in slide mount carriers. Gang bonding is typically employed in high volume applications. The tape is presented to the bonding stage in reel form, and a thermode must be tooled that is specific to the device that will be bonded.

Test and Burn-in - TAB'd die may be tested and burned in standard sockets. The die are tested by contacting the test pads found on the periphery of the tape. ILB'd die may be tested to finished device specifications.

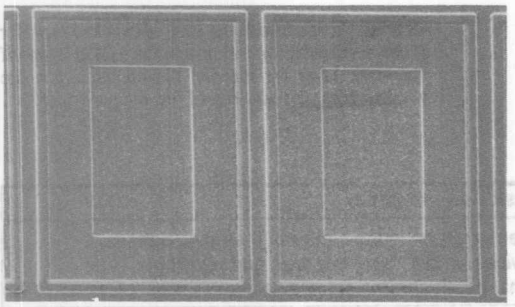
Encapsulation - ILB'd die may be encapsulated with a variety of clear or opaque coatings; non-coated die may be placed into ceramic packages for hermetic applications.

Outer Lead Bond (OLB) - OLB includes excise (and possibly lead forming) of the ILB'd die and attachment to a substrate. Single point thermosonic gold-to-gold or hot bar solder reflow capability is available.

Package Lead Bond (PLB) - Package lead bonding involves attachment of a TAB lead frame to a leadless chip carrier. This technique makes fine pitch outer lead spacing available for devices that may require hermetic packaging.

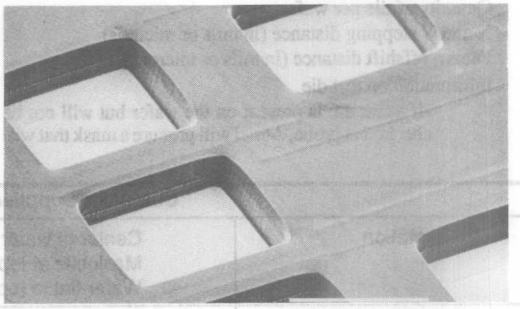
Atmel Gold Bump/TAB Process

Aluminum Bond Pads Covered with Field Metal



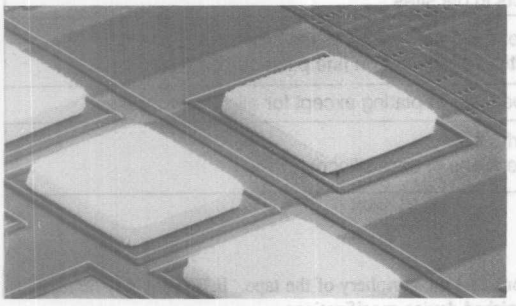
Small rectangle within bond pad is aluminum beneath the field metal
Area of passivation overlapping aluminum bond pad is greater than typical wire bond passivation

Bump Area Defined Prior to Plating



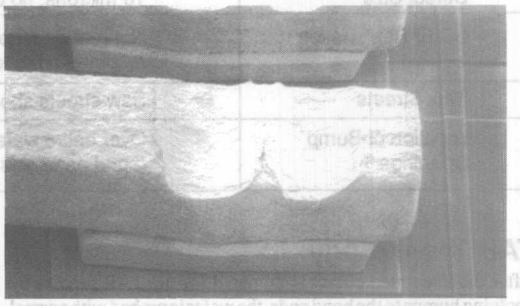
Exposed photosensitive polyimide creates opening for plating a gold bump to the exposed field metal

Gold Bumps Plated on Bond Pads



Polyimide has been removed
Bumps are approximately 25 µ high
Uniform size and profile

Lead Frame Attached to Bump



Tool imprint on lead surface is formed from a single point thermosonic bonder

Specifications

Inner Lead Bond		
Technologies	Thermosonic Single Point Bonding Thermocompression Gang Bonding	
Lead Frame Media	Cu/Polyimide (2 layer), Cu/Adhesive/Polyimide (3 layer) 35 mm/4 pitch to 70 mm/14 pitch Lead Pitch: .004" + (100 µ +) Lead Width Range: .001" to .004" (25 µ to 100 µ)	
Chip Configuration	Size Range (sq.): .073" to .600" (1.9 to 15.2 mm) Thickness Range: .015" to .030" (.37 to .75 mm) I/O Counts: 6 to 500+	
Product Handling	Chip Presentation	Automatic magazine feed Manual
	Lead Frame	Reel-to-reel Single-site chip carrier with magazine carrier
	ILB Component	Reel Single-site chip carrier with magazine carrier
Alignment Tolerance	+/-.0005" (12.5 µ)	

Frame Mount and Excise		
Equipment	35 mm, Super 35 mm	Automatic cut, frame, load into magazines
	48 mm-70 mm	Manually operated cut and frame
	Excise, Lead forming	Tooling product-specified per OLB, die attach requirements

Outer Lead Bond	
Technology	Single-point thermocompression Cu/Au, Au/Au - Pitch range: .005" (125 µ) Hot bar solder reflow - Pitch range .015" (375 µ)
Mounting Media	Ceramic leaded or leadless package Various ceramic/glass, laminate substrates

Encapsulation	
Hermetic/Non-hermetic	Au/Sn kovar resistance and furnace seal Epoxy lid/package Epoxy coat

Package Lead Bond	
Technology	Thermocompression gang bond or thermosonic single point bond Au/Au Pitch range: .005"+(125 µ+)
Mounting Media	Ceramic leaded or leadless package

Performance

System designers have reduced system clock cycle times from well over 100 ns in early system generations to less than 20 ns in commercial systems in development. The significance of the allowance in the system clock cycle for signal edge quality degradation has become correspondingly greater. Since an allowance of between one and three nanoseconds may be required, this allowance as a portion of the system clock has risen from about two percent for early generations to roughly ten percent for systems currently in development. Packaged silicon integrated circuits do not typically provide a controlled environment for fast rise- or fall-time signals through the packaging medium, though PCB designs usually accommodate signal plane isolation through ground or supply-plane shielding. The emphasis on shielding allows the PCB designer to control inductance as an influence on signal quality in the PCB medium. In spite of this control in the PCB medium, the circuit implementation may still have difficulty accepting uncontrolled nodes at the integrated circuit interfaces. The geometry of the TAB package typically results in lower inductance than packages requiring wirebonds. Resistances are also lower since there are no thick-film conductor layers in the signal path of a non-hermetic TAB package and the straight-wire TAB conductor is usually made of copper. In performance oriented systems, a TAB package can provide a superior interface when compared to wire-bonded packages.

Process Qualification/Long Term Reliability

Testing has been performed for evaluation, qualification, and long term reliability assessment of Atmel's gold Bump/TAB process, specifically the bump, bump to die, and lead frame to bump interfaces. To date, no reliability risk with respect to the bump/TAB process can be indentified as a result of this testing.

In the absence of a significant quantity of failures a reliability model cannot be constructed for any of the testing performed. Though the temperature extremes utilized for both Temperature Cycling and Thermal Shock testing provide an acceleration factor relative to nominal operating conditions, a quantitative factor cannot be calculated. However, the number of cycles achieved in the thermal shock at 0°C to 100°C group would equate to over 3.5 years of on/off cycles at 5 cycle per week (1 cycle daily, 5 days/week).

High temperature storage results show a bump reliability of less than 30 FITs for 60 percent confidence at standard operating conditions of 70°C, and an activation energy of 0.5 eV.

Atmel's bump/TAB process has been shown to be reliable, not only at the commercial level of operation but over the military range of temperatures as well.

Test Description

	Quantity Units	Hours/Cycles (through Mar 92)	Process Related Failures
High Temperature Storage			
75°C	14	2234	0
200°C	14	1718	0
Thermal Shock			
0°C to 100°C	22	900	0
-65°C to 150°C	21	900	0
Temperature Cycling			
-55°C to 85°C	22	850	0
-65°C to 150°C	22	800	0

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Quality and Reliability

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Quality and Reliability

Atmel's Policy on Quality 14-3

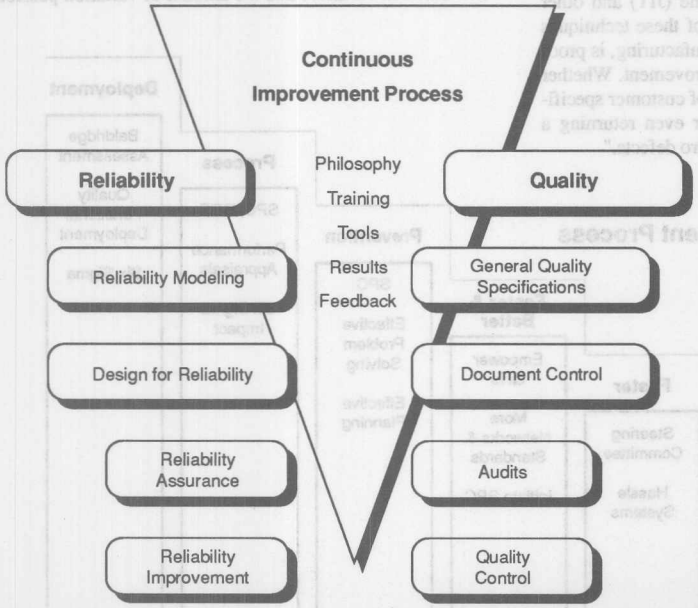
Atmel's Policy on Quality

Dedicated to Customer Satisfaction

It seems like such a simple request - *to get what you want, when you want it, and for a reasonable price*. However, in the complex world of integrated circuits, thousands of factors influence the design and manufacture of a part and can affect how the device will perform. At Atmel, every employee is committed to making sure the customer gets what he wants. From the executive level and throughout the organization, the Company's goal is one hundred percent customer satisfaction.

To achieve this goal, Atmel's employees have developed the philosophy, structure, training and tools necessary to sustain product quality and reliability. The result is two interrelated functions, one dedicated to quality and one dedicated to reliability. The "thread" that ties these functions to each other and to the rest of the Company is the Continuous Improvement Process.

Atmel's corporate philosophy of continuous improvement insures that you get not only high quality, reliable devices, but that every group within the Company is operating with your requirements in mind. Atmel's hallmark is excellence: quality and reliability from its circuits and service from its employees.



Continuous Improvement

Accepting the Malcolm Baldrige National Quality Award, one recipient said that "we are in a race without a finish line." That is a good synopsis of Atmel's philosophy of continuous improvement. The key responsibility of the executives, managers and employees of Atmel is to constantly and forever improve the quality of products and services delivered.

The Company's objectives include providing the leadership and training required to sustain a process of continuous quality improvement; implementing a total quality system that will allow Atmel to compete for and win the Malcolm Baldrige National Quality Award; implementing and utilizing SPC throughout the organization; and understanding and integrating the concepts of "six sigma" into the culture and processes.

In the past, the organization has gone through formal training in the Crosby 14-Step Quality Program; the Alamo Problem Solving, Planning and Decision Making Program; General Quality Specifications; Statistical Process Control (SPC); Statistical Design of Experiments (DOE); and in-house training for managerial and supervision skills.

Today, training continues with an emphasis on SPC, DOE, six sigma concepts and team building. The figure above represents the steps Atmel has already taken along the journey of continuous improvement. Each year, new organizational goals and functional strategies elevate the Company's level of quality even higher.

In addition to training, the journey of continuous improvement involves integrating SPC, DOE, just-in-time (JIT) and other techniques into everyday operations. Use of these techniques throughout the corporation, not just in manufacturing, is proof of Atmel's commitment to continuous improvement. Whether it is order entry, wafer fabrication, review of customer specifications, government compliance testing or even returning a customer's phone call, Atmel strives for "zero defects."

Statistical Process Control

Control of process parameters is the heart of Atmel's continuous improvement system. SPC involves the portrayal of process parametric values in a graphical form to display whether an operation is in control or out of control. Through experimentation and evaluation, upper and lower control limits are established for each parametric value of a given process step. The parametric values are charted on a continual basis and the result is an easy-to-interpret graph which allows for immediate corrections or adjustments by the person closest to the operation. This type of quality measurement can be applied to almost any operation within the Company.

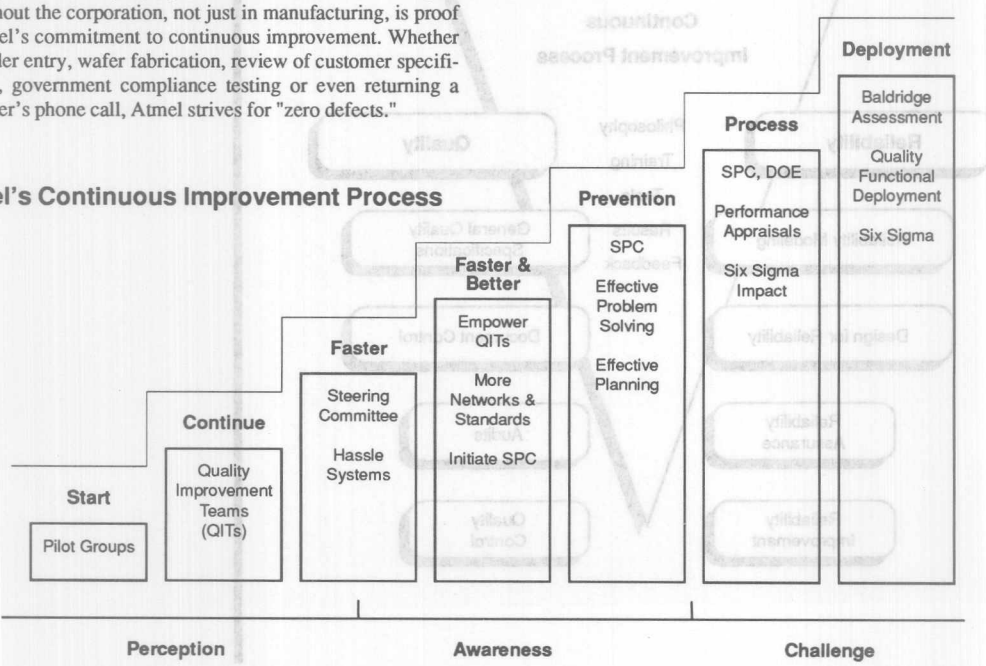
Currently over 500 SPC charts are monitored throughout wafer fabrication, test and packaging operations. Used at crucial points in the fabrication process, SPC insures compliance with pre-set control limits. Measurements taken at critical steps in the process are used in the development of engineering models and applied to current design. Process SPC data is monitored to insure the integrity of each wafer and the resulting statistics are used to constantly improve the process.

Statistical Design of Experiments (DOE)

The DOE technique has been successfully used for many years by the agriculture and chemical industries. Only recently has the technique been used in high-technology industries.

Using DOE, various problems can be solved simultaneously by determining variables that are statistically significant, interaction between variables and the amount of variation possible in

Atmel's Continuous Improvement Process



the process or product. DOE can greatly reduce the time required for process qualification and optimization. This is especially useful in wafer fabrication where quality depends on the interaction of hundreds of different process steps and materials.

When DOE is coupled with computer-aided design and process models, it can be used to predict relationships and outcomes by running experiments. Actual experiments are run on only those processes which show the most promise. This, in turn, reduces the time and cost of designing new products and processes or improving existing ones.

Just-in-time

The concept of receiving products exactly when they are needed for the system is what JIT is all about. In order for this technique to succeed, however, a significant commitment is made by both the supplier and the customer. JIT implies a partnership that gives the customer quality devices, reliable deliveries and lower costs compared with carrying inventory. Atmel performs design and fabrication tasks with such predictability that circuits may go directly to the customer's work floor, eliminating incoming inspection.

The Payoff

Quality and reliability at Atmel cannot be separated from the life cycle of the product. The Company recognizes that quality and reliability must be maintained at all levels of the organization and must be constantly improved. Through continuous improvement and a focus on customer requirements, Atmel has established dock-to-stock programs with several high-performance computer and military system companies.

The bottom line for Atmel customers is lower system life-cycle cost and faster time-to-market. Atmel's culture puts customer requirements and continuous improvement above all else, insuring that indeed you get what you want, when you want it, and at a reasonable price.

Atmel's Quality System

The foundation of Atmel's quality system is MIL-M-38510 and MIL-STD-883. These specifications are translated into company policies covering all areas of design, qualification, manufacturing and customer service. Atmel has chosen to operate to the high standards of the military in order to meet or exceed the needs of commercial and industrial customers. The Company's employees are trained, certified and audited on these policies, which are outlined in Atmel's Quality Manual.

Quality Control

Atmel's quality efforts focus on the customer and their system. For example, through strict attention to customers' component and system requirements Atmel has achieved preferred supplier status. To attain this level of customer confidence the Company demonstrates a commitment to quality control in all areas of the operation. This includes purchase control, in-process quality control, and statistical quality control.

Purchase Control

Every manufacturing process relies on its raw materials, and incoming inspection plays a vital role in the quality of those raw materials. At Atmel, incoming inspection is supplemented by supplier audits, historical review of supplier quality and insistence that suppliers use SPC.

In-process Quality Control

Once raw materials are controlled, the processes that transform them into a final product must also be controlled. This is done through inspection of product at critical, interim stages of manufacturing. Also included is the auditing of personnel and operations to insure that the proper procedures are being followed.

Statistical Quality Control

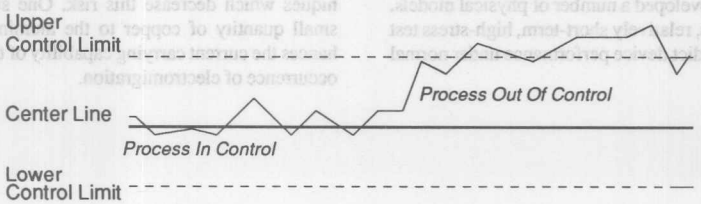
Immediate action is taken by the manufacturing organization when discrepancies are found during an inspection. At Atmel, a typical discrepancy results in permanent corrective action.

However, another vital function of quality control is the reporting of longer-term trends and statistics based upon individual control functions. Statistical quality control can be used to highlight increases in defects or errors in a department, for example. Atmel uses this information to take preventative action when a negative trend is detected.

Audits

Atmel maintains a self-audit group that continually monitors compliance to internal procedures and to customer specifications. The findings of this group are routinely reported to management to insure that adequate corrective actions are taken for any deficiencies.

Example of a Process Control Chart



Understanding Reliability

For integrated circuits, reliability is commonly defined as the probability that a device will operate properly for a given period of time, under specific environmental and electrical conditions. Although various methods exist for expressing reliability, it is most commonly presented in terms of probability of failure.

Reliability Modeling

Applying test data to general failure distribution curves, such as Weibull or lognormal curves, requires that the data fit the distribution and that the model is physically and mathematically reasonable with respect to the failure mechanism. Developing an accurate reliability model requires consideration of non-test-related failures as well as unidentified failure mechanisms. Atmel's reliability program is built on an understanding of the assumptions and restrictions inherent in practical reliability testing.

Design for Reliability

Many reliability concerns can be minimized with proper design techniques. For example ESD, which contributes to production yield loss and is a potential reliability problem, can be reduced or eliminated through the establishment of adequate design rules. Atmel's reliability assurance systems insure that data taken from actual product testing is fed back to design groups for verification of models and design rule updates.

Reliability Assurance Concepts

Accelerated Testing

During its life cycle, an integrated circuit passes through three distinct phases which are best defined by the failure rate of the device. In order to determine the actual interval associated with each phase, a significant number of cumulative failures (usually 50 percent) must be observed. Due to the dramatically small failure rates of integrated circuits, testing under normal operating conditions provides little or no useful data for forecasting reliability. An alternative is to increase stress levels above normal, thereby accelerating the development of failure mechanisms over time. Determining proper stress conditions that lead to realistic failures (those that could occur under normal conditions) without introducing unwanted mechanisms is a primary concern of the Reliability Engineer.

Atmel's Reliability group uses a variety of tests designed to accelerate specific failures and reduce the probability of spurious results. Variables such as temperature, voltage, currents, humidity and radiation can be controlled during testing to influence operational parameters of the device. Stress also can be selectively increased to affect specific circuit elements. To quantify the degree of failure acceleration due to increased stress, the industry has developed a number of physical models. By utilizing these models, relatively short-term, high-stress test results can be used to predict device performance under normal operating conditions.

Failure Rates

Because the failure rate of an integrated circuit varies during its life span, product reliability is best described as the failure rate of units operating after a specified number of hours. This is called Instantaneous Failure Rate, or IFR. Other measures include Average Failure Rate, the average of the IFR over a period of time, and Cumulative Failure Rate, the total number of failures occurring during operation. Because the integrated circuit failure rates are remarkably low, they are normally measured with respect to billions of device hours. This value, referred to as a FIT, is defined as failures per one billion hours of device operation.

Failure Mechanisms

Integrated circuit failure mechanisms can be classified as either process anomalies or wear-out mechanisms. Process anomalies result from less than ideal process conditions and include product defects such as contamination, step coverage deficiencies and electrostatic discharge (ESD) damage. Often termed "quality" problems, these mechanisms are normally detected through process screens such as visual inspection, thermal cycling and burn-in. Process anomalies that escape manufacturing screens often accelerate or encourage wear-out mechanisms. For example, ESD can weaken insulating oxides or thin metallization allowing dielectric breakdown or electromigration failures to occur earlier in the life cycle.

Wear-out mechanisms are directly related to the useful life of device materials, their physical properties, and interactions occurring at material interfaces. Because wear-out mechanisms result from intrinsic physical properties of the materials, reducing these failures requires attention at the design level, strict control of process variation, and use of high quality materials and composites.

Of the failure mechanisms studied by Reliability, electromigration, time-dependent dielectric breakdown and latch-up are the primary concerns.

ELECTROMIGRATION: One of the more studied problems in integrated circuit design and production is electromigration. Devices utilizing aluminum conductors are most susceptible to the phenomena. Electrons flowing in the conductor effectively collide with aluminum atoms, pushing them away and eventually forming an open circuit. Design, wafer process control, metal composition, temperature and current density determine how long a device will operate before electromigration results in a failure. Atmel's experimental electromigration models and associated research have resulted in design and production techniques which decrease this risk. One such technique adds a small quantity of copper to the aluminum. This greatly enhances the current carrying capability of the metal, reducing the occurrence of electromigration.

TIME-DEPENDENT DIELECTRIC BREAKDOWN: Reduced dielectric strength in MOS capacitors is caused by the accumulation of electric charge in a gate oxide, which limits the operational life of the device. Experiments performed on CMOS and Bipolar Enhanced MOS (BEMOS) devices indicate that Atmel's dielectrics and related processes provide excellent resistance to long-term degradation and failure, even at the high voltage levels typical in non-digital circuit applications.

LATCH-UP: Latch-up in a CMOS device allows extremely high current to flow, often resulting in open circuit traces or bond wires. The condition can occur in any PNPN structure. Proper design and Atmel's proprietary process have eliminated this problem before it occurs.

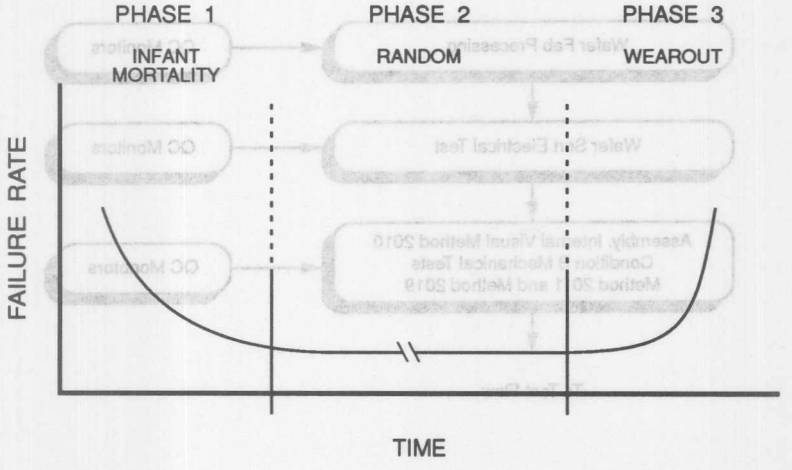
The Bathtub Curve

The traditional "bathtub" curve used to describe the failure rate of a product is actually a combination of two exponential failure rate models. The first model begins with a high failure rate and rapidly declines to a low, nearly constant level. This model describes the early-life reliability of an integrated circuit. Atmel's incoming material inspection, production test and process controls identify and remove potential phase one failures before they are shipped to a customer. Test and screening limits have been established through characterization and qualification of the processes used in fabrication. DOE and SPC are used to maintain process stability and repeatability throughout design, product development and production.

The second model that makes up the "bathtub curve" starts with a low, relatively constant failure rate and climbs exponentially after some period of time. This is the phase three wear-out stage where mechanisms such as electromigration and oxide breakdown predominate. Through rigorous analysis of phase three failures, Atmel has developed techniques to optimize material life. The result is a forestalled phase three period and consequently, an increased phase two period.

By combining these two models, a bathtub-shaped curve representing the lifetime of the product is formed. The nearly flat portion of the curve is the result of a mathematical summation of the "tails" of the two models and represents phase two. A low, stable failure rate is characteristic of this stage as failures observed during this period are random in nature. These random failures are usually the result of sudden exposure to overstress conditions or rare occurrences of wear-out type mechanisms. Devices shipped to the customer are in this stable portion of their lifetime.

Reliability Life (Bathtub) Curve



Manufacturing for Quality and Reliability

All Atmel products are manufactured to the standards of Military Standard 883D, Class B through wafer fabrication and assembly as shown in Figure 1. The products then follow different test flows that correspond to the different classes of products that Atmel offers.

(1) Commercial Grade. This product follows Test Flow (1), Figure 2 and is guaranteed over the temperature range of 0°C to +70°C.

(2) Industrial Grade. This product follows Test Flow (2), Figure 3 and is guaranteed over the temperature range of -40°C to +85°C.

(3) Quality Enhancement Flow. This product follows Test Flow (3), Figure 4 which specifies burn-in of industrial product in a standard flow.

(4) Military Grade. Three classes of military products are offered by Atmel (MIL-STD-883D, Class B standard product, Standard Military Drawing (SMD) product, and Source Control Drawing (SCD) product). The Military Section discusses test procedures for these products in detail.

The Payoff

The focus of Atmel's quality and reliability efforts is the customer and his system. The common goals of highest field reliability and lowest system life cycle cost are achieved through close working relationships using programs such as "ship to stock", "just in time", and "failure trend analysis". Under these programs incoming Atmel circuits go straight to the customers' workfloors— they do not go through an incoming inspection cycle. This, of course, lowers manufacturing costs and is a testimony of the trust that has been established. In addition, long term field failures are analyzed so that corrective action plans can be implemented. Atmel has developed programs such as these with many major customers.

Figure 1. MIL-STD-883D, Class B, Product Flow.
All Atmel products are manufactured to these standards.

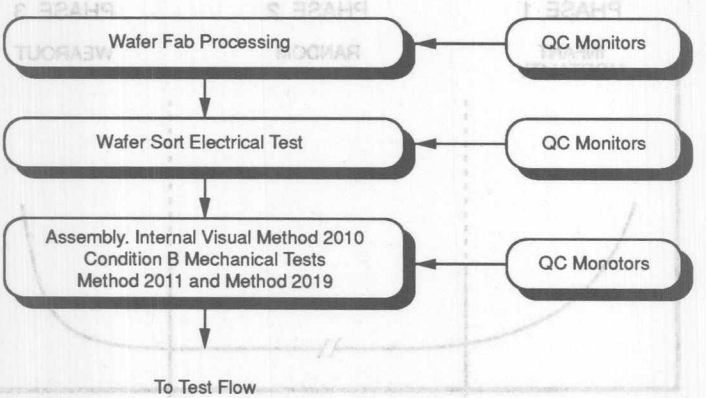


Figure 2. Test Flow (1), Commercial Grade Test Flow.

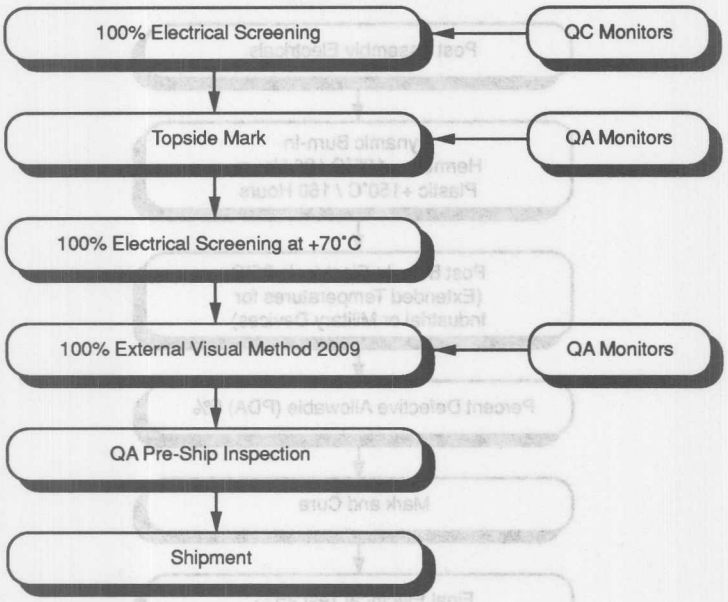


Figure 3. Test Flow (2), Industrial Grade Test Flow.

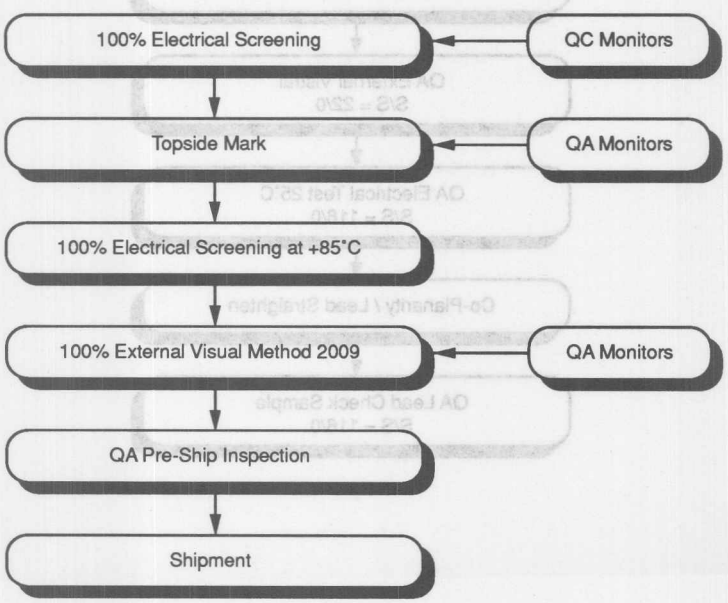
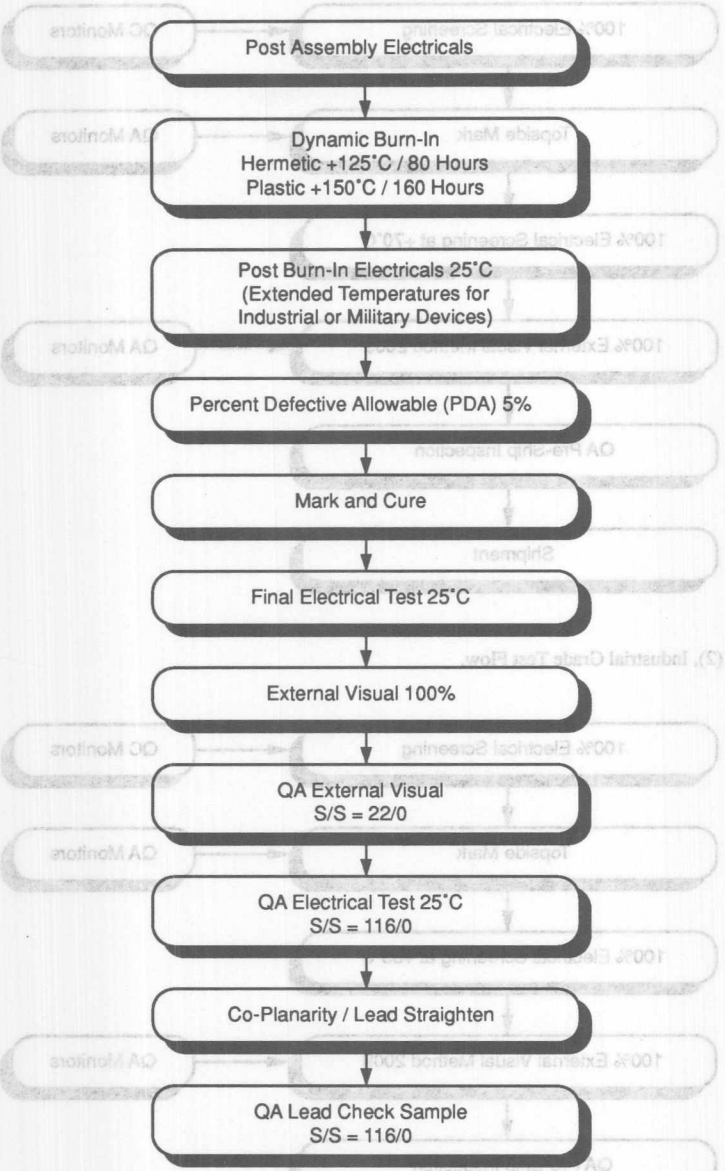


Figure 4. Test Flow (3), Quality Enhancement Flow (-9).



Product Information 1
E^2PROMs 2
PEROMs (Flash) 3
EPROMs 4
PROMs 5
SRAMs 6
EPLDs 7
Gate Arrays 8
Logic 9
Smart Card ICs 10
Mixed Signal 11
Microcontroller 12
Packaging Services 13
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1 Product Information
2 E²PROMs
3 PEROMs (Flash)
4 EPROMs
5 PROMs
6 SRAMs
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Contents

Section 15

Military

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Modified Class S Integrated Circuit Test Flow 15-47

Manufacturing and Test Overview of Military Products

All Atmel products are manufactured to the standards of Military Standard 883D, Class B through wafer fabrication and assembly, as shown in Figure 1. Military products then follow the test flow shown in Figure 2.

Quality Conformance Inspection Data

As shown in Table 1, Atmel performs Groups A, B, C, and D tests in compliance with Military Standard 883D, Class B. Groups A and B are performed on each inspection lot for MIL-STD-883D, Class B products. Groups C and D are periodic inspections as defined in MIL-M-38510. Preconditioning data, Group A, Group B, Group C, and Group D generic data are available for customer procurement.

Military Product Classes

Atmel offers three classes of military products:

(1) MIL-STD-883D, Class B products are fully compliant to MIL-STD-883C Paragraph 1.2.1, with no exceptions. A Certificate of Compliance (C of C) is enclosed with each shipment of MIL-STD-883D, Class B product.

(2) Standardized Military Drawing (SMD) products are fully compliant to MIL-STD-883D Paragraph 1.2.1 with optional additional tests as specified in the applicable Standardized Military Drawing as approved by DESC. Section 2, Table 1 lists currently approved Atmel SMD parts, organized by Atmel part type. Section 2, Table 2 lists currently approved Atmel SMD parts, organized by SMD number.

(3) Source Control Drawing (SCD) products are fully compliant to MIL-STD-883D Paragraph 1.2.1 with optional additional tests as specified by the specific customer specification. Atmel must review and accept a customer Source Control Drawing prior to order acceptance to assure compliance.

Figure 1. MIL-STD-883D, Class B, Product Flow.
All Atmel products are manufactured to these standards.

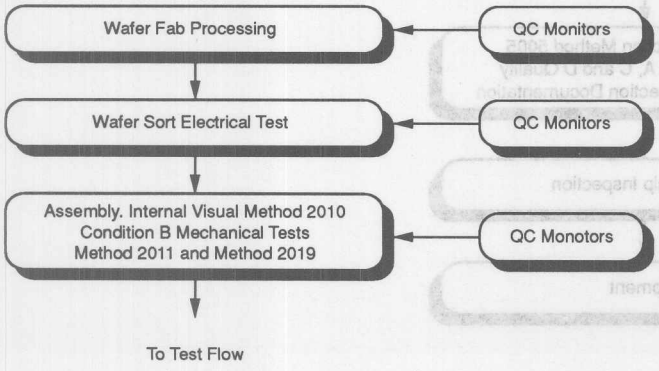


Figure 2. Test Flow (3), MIL-STD-883D, Class B, SMD and SCD Test Flow.

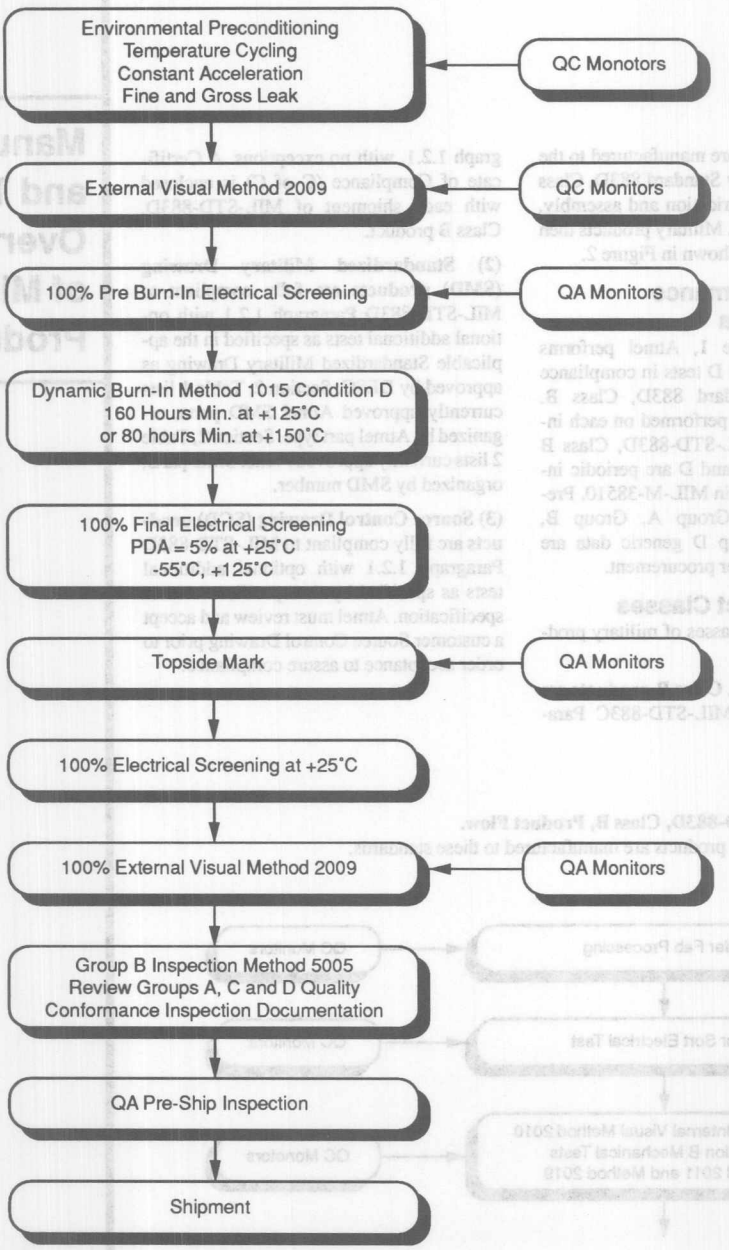


Table 1. Military Standard 883D, Class B Tests

Group A: Electrical Tests

Performed On Each Lot

Screen	MIL-STD-883D Method 5005 Table 1 Subgroups	LPTD
Static Tests at +25°C	1	2
Static Tests at +125°C	2	2
Static Tests at -55°C	3	2
Dynamic Tests at +25°C	4	2
Function Tests at +25°C	7	2
Function Tests at +125°C	8A	2
Function Tests at -55°C	8B	2
Switching Tests at +25°C	9	2
Switching Tests at +125°C	10	2
Switching Tests at -55°C	11	2

Group B: Assembly Integrity Tests

Performed On Each Lot

Screen	MIL-STD-883D Test Method	Conditions	Quantity (Accept No. or LTPD)
SUBGROUP 2			
Resistance to Solvents	2015	Top and Bottom Marks	4(0)
SUBGROUP 3			
Solderability	2003	+245°C +/-5°C	10
SUBGROUP 5			
Bond Strength	2011	Condition D	15

Group C: Die Related Tests

Performed Per MIL-STD-883D Paragraph 1.2.1

Screen	MIL-STD-883D Test Method	Conditions	LTPD
SUBGROUP 1			
Steady State Life Test	1005	Condition D	5
End Point Electricals	5005	As specified in the applicable device specification	

Table 1. Military Standard 883D, Class B Tests *(continued)*

Group D: Package Related Tests

Performed Per MIL-STD-883D Paragraph 1.2.1
By Package Type, Assembly Location, and Exterior Lead Finish

Screen	MIL-STD-883D Test Method	Conditions	Quantity (Accept No. or LTPD)
SUBGROUP 1			
Physical Dimensions	2016	MIL-M-38510, Appendix C	15
SUBGROUP 2			5
Lead Integrity	2004	Condition B2 (Condition D for LCC)	
Seal: Fine	1014	Conditon A or B	
Seal:Gross	1014	Condition C	
SUBGROUP 3			15
Thermal Shock	1011	Condition B, 15 Cycles	
Temperature Cycling	1010	Condition C, 100 Cycles	
Moisture Resistance	1004	10 Cycles	
End Point Electricals	5005	As specified in the applicable device specification (within 42 hrs)	
Seal: Fine	1014	Condition A or B	
Seal: Gross	1014	Condition C	
Visual Examination		Per Visual of Method 1004 and 1010	
SUBGROUP 4			15
Mechanical Shock	2002	Condition B	
Vibration Variable Freq.	2007	Condition A	
Constant Acceleration	2001	Condition E, 30 KG., Y1	
Seal: Fine	1014	Condition A or B	
Seal: Gross	1014	Condition C	
Visual Examination	1010		
End Point Electricals	5005	As specified in the applicable device specification	
SUBGROUP 5			15
Salt Atmosphere	1009	Condition A	
Seal: Fine	1014	Condition A or B	
Seal: Gross	1014	Condition C	
Visual Examination		Per Visual of Method 1009	
SUBGROUP 6			3 (0) or 5 (1)
Internal Water Vapor Content	1018	5,000 PPM Maximum Water Content at 100°C	
SUBGROUP 7			15
Adhesion of Lead Finish	2025	Glass Frit Seal Only (LTPD for Number of Leads)	
SUBGROUP 8			5 (0)
Lid Torque	2024	Glass Frit Seal Only	

Standard Military Drawing Product Offering

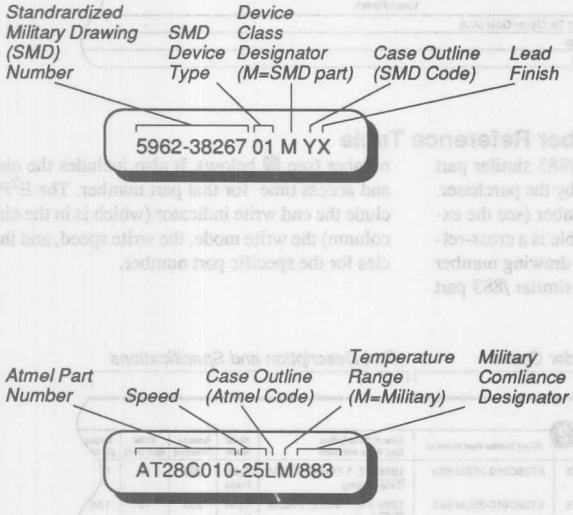
Introduction to the SMD Product Listing

Each Standardized Military Drawing (SMD) part number that Atmel supplies corresponds to an Atmel /883 part number. SMD products are compliant to MIL-STD-883, paragraph 1.2.1 and to the requirements of the applicable standardized military drawing. The tables in this section list the currently approved Atmel SMD parts by Atmel part number (Table 1) and by SMD part number (Table 2). They define and cross reference the Atmel /883 part number with the SMD part number for your ordering convenience.

Figure 1 (below) shows how an Atmel SMD order number defines a part, compared to the components of the Atmel similar part number.

Please note that some SMD part numbers contain the letter "M" between the device type and the case outline designator. The "M" is part of the one part-one number system, set up by DESC. It is a device class designator which indicates the part is an SMD part number as opposed to being a JAN part number.

Figure 1. Components of an SMD number (top) compared to the Atmel similar part number (bottom).



How to Use the Atmel Part Type Reference Table

The organization of Table 1 enables the purchaser to order a standardized military part by using the Atmel generic part type to locate the correct SMD drawing number. The SMD part number is the order number for SMD devices. The Atmel generic part type, which begins with the prefix "AT," heads Table 1. There are four sections in this table (see the sample table below):

SMD Options

The first section lists the SMD options available at Atmel. It includes the industry generic part type, the SMD drawing number, and the SMD device type. The SMD case outline options, the lead finish options, the circuit description, and the access time that correspond to that device type are also included. The tables for the E^2PROM in this section include the end write indicator in the circuit description column and the write mode for the specific device type.

Order Code Cross-Reference

The next section of the table cross-references each optionally complete SMD part number (see ❶ below) with the Atmel similar /883 part number (see ❷ below).

Case Outline Legend

The third section gives the SMD case outline options available for the device.

Lead Finish Legend

The last section lists the SMD lead finish options available for the device.

SMD Options with Part Description and Specifications

Order Code Cross-Reference

Case Outline Legend

Lead Finish Legend

AT28C010

Generic Number	Standard Military Drawing Number				Description				
28C010	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Spd(ms)	Endurance (Cycles)
	5962-38267	01	X, Y, Z	X, A, C	128K x 8, 1-Mbit E^2PROM Data Polling	Byte/ Page	250	10	10K
	5962-38267	03	X, Y, Z	X, A, C	128K x 8, 1-Mbit E^2PROM Data Polling	Byte/ Page	200	10	10

Atmel Cage No. 1FN41	Example: Atmel Order Number		Atmel Similar Part Number
	❶ 5962-38267 01M XX	❷	AT28C010-25BM/883
	5962-38267 01M YX		AT28C010-25LM/883
	5962-38267 01M ZX		AT28C010-25FM/883
	5962-38267 03M XX		AT28C010-20BM/883
	5962-38267 03M YX		AT28C010-20LM/883
	5962-38267 03M ZX		AT28C010-20FM/883

Case Outline	
X	32B, 32 Lead, 0.600" Wide, Ceramic Side Braze Dual Inline (Side Braze)
Y	44L, 44 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	32F, 32 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

How to Use the Atmel SMD Number Reference Table

Table 2 allows quick reference to the Atmel /883 similar part number when the SMD part number is known by the purchaser. The head for Table 2 is the SMD drawing number (see the example table below). The only section in this table is a cross-reference between the optionally complete SMD drawing number (see ❶ below) and the corresponding Atmel similar /883 part number (see ❷ below). It also includes the circuit description and access time for that part number. The E^2PROM tables include the end write indicator (which is in the circuit description column) the write mode, the write speed, and the endurance cycles for the specific part number.

Order Codes *Part Description and Specifications*

Order Code Cross-Reference

5962-38267

❶ Atmel Order Number	❷ Atmel Similar Part Number	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Spd. (ms)	Endur (Cycl
5962-38267 01M XX	AT28C010-25BM/883	128K x 8, 1-Mbit E^2PROM Data Polling	Byte/ Page	250	10	1
5962-38267 01M YX	AT28C010-25LM/883	128K x 8, 1-Mbit E^2PROM Data Polling	Byte/ Page	250	10	10K
5962-38267 01M ZX	AT28C010-25FM/883	128K x 8, 1-Mbit E^2PROM Data Polling	Byte/ Page	250	10	10K
5962-38267 03M XX	AT28C010-20BM/883	128K x 8, 1-Mbit E^2PROM Data Polling	Byte/ Page	200	10	1
5962-38267 03M YX	AT28C010-20LM/883	128K x 8, 1-Mbit E^2PROM Data Polling	Byte/ Page	200	10	10K
5962-38267 03M ZX	AT28C010-20FM/883	128K x 8, 1-Mbit E^2PROM Data Polling	Byte/ Page	200	10	10K

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number

AT22V10

Generic Number	Standardized Military Drawing Number				Description	
C22V10	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	TPD (ns)
	5962-87539	01	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	25
	5962-87539	02	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	30
	5962-87539	03	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	40
	5962-87539	04	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	20

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-87539 **01 KX**	AT22V10-25YM/883
	5962-87539 **01 LX**	AT22V10-25DM/883
	5962-87539 **01 3X**	AT22V10-25LM/883
	5962-87539 **02 KX**	AT22V10-30YM/883
	5962-87539 **02 LX**	AT22V10-30DM/883
	5962-87539 **02 3X**	AT22V10-30LM/883
	5962-87539 **03 KX**	AT22V10-40YM/883
	5962-87539 **03 LX**	AT22V10-40DM/883
	5962-87539 **03 3X**	AT22V10-40LM/883
	5962-87539 **04 KX**	AT22V10-20YM/883
	5962-87539 **04 LX**	AT22V10-20DM/883
	5962-87539 **04 3X**	AT22V10-20LM/883

Case Outline	
K	24CW, 24 Lead, Windowed, Ceramic Flat Package (Cerpack)
L	24DW3, 24 Lead 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
3	28LW, 28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

AT22V10L

Generic Number	Standardized Military Drawing Number				Description	
C22V10L	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	TPD (ns)
	5962-88724	01	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	25
	5962-88724	02	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	30
	5962-88724	03	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	40
	5962-88724	04	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	20

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-88724 **01 KX**	AT22V10L-25YM/883
	5962-88724 **01 LX**	AT22V10L-25DM/883
	5962-88724 **01 3X**	AT22V10L-25LM/883
	5962-88724 **02 KX**	AT22V10L-30YM/883
	5962-88724 **02 LX**	AT22V10L-30DM/883
	5962-88724 **02 3X**	AT22V10L-30LM/883
	5962-88724 **03 KX**	AT22V10L-40YM/883
	5962-88724 **03 LX**	AT22V10L-40DM/883
	5962-88724 **03 3X**	AT22V10L-40LM/883
	5962-88724 **04 KX**	AT22V10L-20YM/883
	5962-88724 **04 LX**	AT22V10L-20DM/883
	5962-88724 **04 3X**	AT22V10L-20LM/883

Case Outline	
K	24CW, 24 Lead, Windowed, Ceramic Flat Package (Cerpack)
L	24DW3, 24 Lead 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
3	28LW, 28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number *(continued)*

AT22V10 OTP

Generic Number	Standardized Military Drawing Number				Description	
C22V10 OTP	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	TPD (ns)
	5962-88670	01	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	25
	5962-88670	02	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	30
	5962-88670	03	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	40
	5962-88670	04	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	20
	5962-88670	05	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	15

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-88670 **01 KX**	AT22V10-25FM/883
	5962-88670 **01 LX**	AT22V10-25GM/883
	5962-88670 **01 3X**	AT22V10-25NM/883
	5962-88670 **02 KX**	AT22V10-30FM/883
	5962-88670 **02 LX**	AT22V10-30GM/883
	5962-88670 **02 3X**	AT22V10-30NM/883
	5962-88670 **03 KX**	AT22V10-40FM/883
	5962-88670 **03 LX**	AT22V10-40GM/883
	5962-88670 **03 3X**	AT22V10-40NM/883
	5962-88670 **04 KX**	AT22V10-20FM/883
	5962-88670 **04 LX**	AT22V10-20GM/883
	5962-88670 **04 3X**	AT22V10-20NM/883
	5962-88670 **05 KX**	AT22V10-15FM/883
	5962-88670 **05 LX**	AT22V10-15GM/883
	5962-88670 **05 3X**	AT22V10-15NM/883

Case Outline	
K	24C, 24 Lead, Non-Windowed, Ceramic Flat Package (Cerpack)
L	24D3, 24 Lead 0.300" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
3	28L, 28 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number *(continued)*

AT22V10L OTP

Generic Number	Standardizedized Military Drawing Number				Description	
C22V10L OTP	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	TPD (ns)
	5962-89755	01	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	25
	5962-89755	02	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	30
	5962-89755	03	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	40
	5962-89755	04	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	20

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-89755 **01 KX**	AT22V10L-25FM/883
	5962-89755 **01 LX**	AT22V10L-25GM/883
	5962-89755 **01 3X**	AT22V10L-25NM/883
	5962-89755 **02 KX**	AT22V10L-30FM/883
	5962-89755 **02 LX**	AT22V10L-30GM/883
	5962-89755 **02 3X**	AT22V10L-30NM/883
	5962-89755 **03 KX**	AT22V10L-40FM/883
	5962-89755 **03 LX**	AT22V10L-40GM/883
	5962-89755 **03 3X**	AT22V10L-40NM/883
	5962-89755 **04 KX**	AT22V10L-20FM/883
	5962-89755 **04 LX**	AT22V10L-20GM/883
	5962-89755 **04 3X**	AT22V10L-20NM/883

Case Outline	
K	24C, 24 Lead, Non-Windowed, Ceramic Flat Package (Cerpack)
L	24D3, 24 Lead 0.300" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
3	28L, 28 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number *(continued)*

ATV750

Generic Number	Standardized Military Drawing Number				Description	
V750	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	TPD (ns)
	5962-88726	01	L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	40
	5962-88726	02	L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	35
	5962-88726	03	L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	25
	5962-88726	04	L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	20

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-88726 **01 LX**	ATV750-40DM/883
	5962-88726 **01 3X**	ATV750-40LM/883
	5962-88726 **02 LX**	ATV750-35DM/883
	5962-88726 **02 3X**	ATV750-35LM/883
	5962-88726 **03 LX**	ATV750-25DM/883
	5962-88726 **03 3X**	ATV750-25LM/883
	5962-88726 **04 LX**	ATV750-20DM/883
	5962-88726 **04 3X**	ATV750-20LM/883

ATV750L

Generic Number	Standardized Military Drawing Number				Description	
V750L	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	TPD (ns)
	5962-88726	06	L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	30
	5962-88726	07	L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	25

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-88726 **06 LX**	ATV750L-30DM/883
	5962-88726 **06 3X**	ATV750L-30LM/883
	5962-88726 **07 LX**	ATV750L-25DM/883
	5962-88726 **07 3X**	ATV750L-25LM/883

Case Outline	
L	24DW3, 24 Lead 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
3	28LW, 28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number *(continued)*

ATV2500H

Generic Number	Standardized Military Drawing Number				Description	
V2500	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	TPD (ns)
	5962-91545	01	Q,X,Y	X, A, C	38-Input, 24-Output and-or-Logic Array	35
	5962-91545	02	Q,X,Y	X, A, C	38-Input, 24-Output and-or-Logic Array	25

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-91545 **01M QX**	ATV2500H-35DM/883
	5962-91545 **01M XX**	ATV2500H-35LM/883
	5962-91545 **01M YX**	ATV2500H-35KM/883
	5962-91545 **02M QX**	ATV2500H-25DM/883
	5962-91545 **02M XX**	ATV2500H-25LM/883
	5962-91545 **02M YX**	ATV2500H-25KM/883

ATV2500L

Generic Number	Standardized Military Drawing Number				Description	
V2500L	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	TPD (ns)
	5962-91545	03	Q,X,Y	X, A, C	38-Input, 24-Output and-or-Logic Array	30

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-91545 **03M QX**	ATV2500L-30DM/883
	5962-91545 **03M XX**	ATV2500L-30LM/883
	5962-91545 **03M YX**	ATV2500L-30KM/883

Case Outline	
Q	40DW6, 40 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
X	44LW, 44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
Y	44KW, 44 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number *(continued)*

AT27C256R

Generic Number	Standardized Military Drawing Number				Description	
27C256R	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	Access Time (ns)
	5962-86063	01	X, Y, Z	X, A, C	32K x 8 EPROM	200
	5962-86063	02	X, Y, Z	X, A, C	32K x 8 EPROM	250
	5962-86063	03	X, Y, Z	X, A, C	32K x 8 EPROM	300
	5962-86063	04	X, Y, Z	X, A, C	32K x 8 EPROM	170
	5962-86063	05	X, Y, Z	X, A, C	32K x 8 EPROM	170
	5962-86063	06	X, Y, Z	X, A, C	32K x 8 EPROM	120
	5962-86063	07	X, Y, Z	X, A, C	32K x 8 EPROM	90

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-86063 01 XX	AT27C256R-20DM/883
	5962-86063 01 YX	AT27C256R-20LM/883
	5962-86063 01 ZX	AT27C256R-20KM/883
	5962-86063 02 XX	AT27C256R-25DM/883
	5962-86063 02 YX	AT27C256R-25LM/883
	5962-86063 02 ZX	AT27C256R-25KM/883
	5962-86063 03 XX	AT27C256R-30DM/883
	5962-86063 03 YX	AT27C256R-30LM/883
	5962-86063 03 ZX	AT27C256R-30KM/883
	5962-86063 04 XX	AT27C256R-17DM/883
	5962-86063 04 YX	AT27C256R-17LM/883
	5962-86063 04 ZX	AT27C256R-17KM/883
	5962-86063 05 XX	AT27C256R-15DM/883
	5962-86063 05 YX	AT27C256R-15LM/883
	5962-86063 05 ZX	AT27C256R-15KM/883
	5962-86063 06 XX	AT27C256R-12DM/883
	5962-86063 06 YX	AT27C256R-12LM/883
	5962-86063 06 ZX	AT27C256R-12KM/883
	5962-86063 07 XX	AT27C256R-90DM/883
	5962-86063 07 YX	AT27C256R-90LM/883
	5962-86063 07 ZX	AT27C256R-90KM/883

Case Outline	
X	32DW6, 32 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number *(continued)*

AT27HC256R

Generic Number	Standardized Military Drawing Number				Description	
27HC256R	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	Access Time (ns)
	5962-86063	08	X, Y, Z	X, A, C	32K x 8 EPROM	70

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-86063 **08 XX**	AT27HC256R-70DM/883
	5962-86063 **08 YX**	AT27HC256R-70LM/883
	5962-86063 **08 ZX**	AT27HC256R-70KM/883

Case Outline	
X	28DW6, 28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	32KW, 32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number *(continued)*

AT27C512R

Generic Number	Standardized Military Drawing Number				Description	
27C512R	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	Access Time (ns)
	5962-87648	01	X, Y, Z	X, A, C	64K x 8 EPROM	150
	5962-87648	02	X, Y, Z	X, A, C	64K x 8 EPROM	200
	5962-87648	03	X, Y, Z	X, A, C	64K x 8 EPROM	250
	5962-87648	04	X, Y, Z	X, A, C	64K x 8 EPROM	120

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-87648 **01 XX**	AT27C512R-15DM/883
	5962-87648 **01 YX**	AT27C512R-15LM/883
	5962-87648 **01 ZX**	AT27C512R-15KM/883
	5962-87648 **02 XX**	AT27C512R-20DM/883
	5962-87648 **02 YX**	AT27C512R-20LM/883
	5962-87648 **02 ZX**	AT27C512R-20KM/883
	5962-87648 **03 XX**	AT27C512R-25DM/883
	5962-87648 **03 YX**	AT27C512R-25LM/883
	5962-87648 **03 ZX**	AT27C512R-25KM/883
	5962-87648 **04 XX**	AT27C512R-12DM/883
	5962-87648 **04 YX**	AT27C512R-12LM/883
	5962-87648 **04 ZX**	AT27C512R-12KM/883

Case Outline	
X	28DW6, 28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	32KW, 32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number *(continued)*

AT27C010

Generic Number	Standardized Military Drawing Number				Description	
27C010	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	Access Time (ns)
	5962-89614	01	X, Y	X, A, C	128K x 8, 1-Mbit EPROM	300
	5962-89614	02	X, Y	X, A, C	128K x 8, 1-Mbit EPROM	250
	5962-89614	03	X, Y	X, A, C	128K x 8, 1-Mbit EPROM	200
	5962-89614	04	X, Y	X, A, C	128K x 8, 1-Mbit EPROM	170
	5962-89614	05	X, Y	X, A, C	128K x 8, 1-Mbit EPROM	150
	5962-89614	06	X, Y	X, A, C	128K x 8, 1-Mbit EPROM	120

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-89614 **01M XX**	AT27C010-30DM/883
	5962-89614 **01M YX**	AT27C010-30LM/883
	5962-89614 **02M XX**	AT27C010-25DM/883
	5962-89614 **02M YX**	AT27C010-25LM/883
	5962-89614 **03M XX**	AT27C010-20DM/883
	5962-89614 **03M YX**	AT27C010-20LM/883
	5962-89614 **04M XX**	AT27C010-17DM/883
	5962-89614 **04M YX**	AT27C010-17LM/883
	5962-89614 **05M XX**	AT27C010-15DM/883
	5962-89614 **05M YX**	AT27C010-15LM/883
	5962-89614 **06M XX**	AT27C010-12DM/883
	5962-89614 **06M YX**	AT27C010-12LM/883

Case Outline	
X	32DW6, 32 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number *(continued)*

AT27C1024

Generic Number	Standardized Military Drawing Number				Description	
27C1024	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	Access Time (ns)
	5962-86805	01	Q, X	X, A, C	64K x 16, 1-Mbit EPROM	300
	5962-86805	02	Q, X	X, A, C	64K x 16, 1-Mbit EPROM	250
	5962-86805	03	Q, X	X, A, C	64K x 16, 1-Mbit EPROM	200
	5962-86805	04	Q, X	X, A, C	64K x 16, 1-Mbit EPROM	170
	5962-86805	05	Q, X	X, A, C	64K x 16, 1-Mbit EPROM	150
	5962-86805	06	Q, X	X, A, C	64K x 16, 1-Mbit EPROM	120

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-86805 **01 QX**	AT27C1024-30DM/883
	5962-86805 **01 XX**	AT27C1024-30LM/883
	5962-86805 **02 QX**	AT27C1024-25DM/883
	5962-86805 **02 XX**	AT27C1024-25LM/883
	5962-86805 **03 QX**	AT27C1024-20DM/883
	5962-86805 **03 XX**	AT27C1024-20LM/883
	5962-86805 **04 QX**	AT27C1024-17DM/883
	5962-86805 **04 XX**	AT27C1024-17LM/883
	5962-86805 **05 QX**	AT27C1024-15DM/883
	5962-86805 **05 XX**	AT27C1024-15LM/883
	5962-86805 **06 QX**	AT27C1024-12DM/883
	5962-86805 **06 XX**	AT27C1024-12LM/883

Case Outline	
Q	40DW6, 40 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
X	44LW, 44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number *(continued)*

AT27HC1024

Generic Number	Standardized Military Drawing Number				Description	
27HC1024	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	Access Time (ns)
	5962-86805	07	Q, X	X, A, C	64K x 16, 1-Mbit EPROM	90
	5962-86805	08	Q, X	X, A, C	64K x 16, 1-Mbit EPROM	70

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-86805 **07 QX**	AT27HC1024-90DM/883
	5962-86805 **07 XX**	AT27HC1024-90LM/883
	5962-86805 **08 QX**	AT27HC1024-70DM/883
	5962-86805 **08 XX**	AT27HC1024-70LM/883

Case Outline	
Q	40DW6, 40 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
X	44LW, 44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number *(continued)*

AT27HC641R

Generic Number	Standardized Military Drawing Number				Description	
27HC641R	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	Access Time (ns)
	5962-87515	01	J, K, 3	X, A, C	8K x 8 [UV] PROM	45
	5962-87515	02	J, K, 3	X, A, C	8K x 8 [UV] PROM	55
	5962-87515	03	J, K, 3	X, A, C	8K x 8 [UV] PROM	70
	5962-87515	04	J, K, 3	X, A, C	8K x 8 [UV] PROM	90

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-87515 **01 JX**	AT27HC641R-45DM/883
	5962-87515 **01 KX**	AT27HC641R-45CM/883
	5962-87515 **01 3X**	AT27HC641R-45LM/883
	5962-87515 **02 JX**	AT27HC641R-55DM/883
	5962-87515 **02 KX**	AT27HC641R-55CM/883
	5962-87515 **02 3X**	AT27HC641R-55LM/883
	5962-87515 **03 JX**	AT27HC641R-70DM/883
	5962-87515 **03 KX**	AT27HC641R-70CM/883
	5962-87515 **03 3X**	AT27HC641R-70LM/883
	5962-87515 **04 JX**	AT27HC641R-90DM/883
	5962-87515 **04 KX**	AT27HC641R-90CM/883
	5962-87515 **04 3X**	AT27HC641R-90LM/883

Case Outline	
J	24DW6, 24 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
K	24CW, 24 Lead, Windowed, Ceramic Flat Package (Cerpack)
3	28LW, 28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number *(continued)*

AT27HC642R

Generic Number	Standardized Military Drawing Number				Description	
27HC642R	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	Access Time (ns)
	5962-87515	01	L	X, A, C	8K x 8 [UV] PROM	45
	5962-87515	02	L	X, A, C	8K x 8 [UV] PROM	55
	5962-87515	03	L	X, A, C	8K x 8 [UV] PROM	70
	5962-87515	04	L	X, A, C	8K x 8 [UV] PROM	90

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-87515 **01 LX**	AT27HC642R-45DM/883
	5962-87515 **02 LX**	AT27HC642R-55DM/883
	5962-87515 **03 LX**	AT27HC642R-70DM/883
	5962-87515 **04 LX**	AT27HC642R-90DM/883

Case Outline	
L	24DW3, 24 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number *(continued)*

AT28C64

Generic Number	Standardized Military Drawing Number				Description				
28C64	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Speed(ms)	Endurance (Cycles)
	5962-87514	13	X, Y, Z	X, A, C	8K x 8 E^2PROM Rdy/$\overline{Busy}$	Byte	350	1	10K
	5962-87514	14	X, Y	X, A, C	8K x 8 E^2PROM Rdy/$\overline{Busy}$	Byte	300	1	10K
	5962-87514	15	X, Y, Z	X, A, C	8K x 8 E^2PROM Rdy/$\overline{Busy}$	Byte	250	1	10K
	5962-87514	16	X, Y	X, A, C	8K x 8 E^2PROM Rdy/$\overline{Busy}$	Byte	200	1	10K
	5962-87514	17	X, Y	X, A, C	8K x 8 E^2PROM Rdy/$\overline{Busy}$	Byte	150	1	10K

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-87514 13 XX	AT28C64-35DM/883
	5962-87514 13 YX	AT28C64-35LM/883
	5962-87514 13 ZX	AT28C64-35FM/883
	5962-87514 14 XX	AT28C64-30DM/883
	5962-87514 14 YX	AT28C64-30LM/883
	5962-87514 15 XX	AT28C64-25DM/883
	5962-87514 15 YX	AT28C64-25LM/883
	5962-87514 15 ZX	AT28C64-25FM/883
	5962-87514 16 XX	AT28C64-20DM/883
	5962-87514 16 YX	AT28C64-20LM/883
	5962-87514 17 XX	AT28C64-15DM/883
	5962-87514 17 YX	AT28C64-15LM/883

Case Outline	
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number *(continued)*

AT28C64X

Generic Number	Standardized Military Drawing Number				Description				
28C64X	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Speed(ms)	Endurance (Cycles)
	5962-87514	18	X, Y	X, A, C	8K x 8 E^2PROM Data Polling	Byte	350	1	10K
	5962-87514	19	X, Y	X, A, C	8K x 8 E^2PROM Data Polling	Byte	300	1	10K
	5962-87514	20	X, Y, Z	X, A, C	8K x 8 E^2PROM Data Polling	Byte	250	1	10K
	5962-87514	21	X, Y	X, A, C	8K x 8 E^2PROM Data Polling	Byte	200	1	10K
	5962-87514	22	X, Y	X, A, C	8K x 8 E^2PROM Data Polling	Byte	150	1	10K

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-87514 **18 XX**	AT28C64X-35DM/883
	5962-87514 **18 YX**	AT28C64X-35LM/883
	5962-87514 **19 XX**	AT28C64X-30DM/883
	5962-87514 **19 YX**	AT28C64X-30LM/883
	5962-87514 **20 XX**	AT28C64X-25DM/883
	5962-87514 **20 YX**	AT28C64X-25LM/883
	5962-87514 **20 ZX**	AT28C64X-25FM/883
	5962-87514 **21 XX**	AT28C64X-20DM/883
	5962-87514 **21 YX**	AT28C64X-20LM/883
	5962-87514 **22 XX**	AT28C64X-15DM/883
	5962-87514 **22 YX**	AT28C64X-15LM/883

Case Outline	
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number *(continued)*

AT28HC64L

Generic Number	Standardized Military Drawing Number				Description				
28HC64L	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Speed(ms)	Endurance (Cycles)
	5962-87514	10	X, Y	X, A, C	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	120	2	10K
	5962-87514	11	X, Y	X, A, C	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	90	2	10K
	5962-87514	12	X, Y	X, A, C	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	70	2	10K

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-87514 **10 XX**	AT28HC64L-12DM/883
	5962-87514 **10 YX**	AT28HC64L-12LM/883
	5962-87514 **11 XX**	AT28HC64L-90DM/883
	5962-87514 **11 YX**	AT28HC64L-90LM/883
	5962-87514 **12 XX**	AT28HC64L-70DM/883
	5962-87514 **12 YX**	AT28HC64L-70LM/883

Case Outline	
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number *(continued)*

AT28PC64

Generic Number	Standardized Military Drawing Number				Description				
28PC64	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Speed(ms)	Endurance (Cycles)
	5962-87514	06	X, Y	X, A, C	8K x 8 E^2PROM Data Polling	Byte/Page	350	2	10K
	5962-87514	07	X, Y	X, A, C	8K x 8 E^2PROM Data Polling	Byte/Page	300	2	10K
	5962-87514	08	X, Y	X, A, C	8K x 8 E^2PROM Data Polling	Byte/Page	250	2	10K
	5962-87514	09	X, Y	X, A, C	8K x 8 E^2PROM Data Polling	Byte/Page	200	2	10K

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-87514 **06 XX**	AT28PC64-35DM/883
	5962-87514 **06 YX**	AT28PC64-35LM/883
	5962-87514 **07 XX**	AT28PC64-30DM/883
	5962-87514 **07 YX**	AT28PC64-30LM/883
	5962-87514 **08 XX**	AT28PC64-25DM/883
	5962-87514 **08 YX**	AT28PC64-25LM/883
	5962-87514 **09 XX**	AT28PC64-20DM/883
	5962-87514 **09 YX**	AT28PC64-20LM/883

Case Outline	
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number *(continued)*

AT28C256

Generic Number	Standardized Military Drawing Number				Description				
28C256	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Speed(ms)	Endurance (Cycles)
	5962-88525	01	U, X, Y, Z	X, A, C	32K x 8 E^2PROM Data Polling	Byte/Page	350	10	10K
	5962-88525	02	U, X, Y, Z	X, A, C	32K x 8 E^2PROM Data Polling	Byte/Page	300	10	10K
	5962-88525	03	U, X, Y, Z	X, A, C	32K x 8 E^2PROM Data Polling	Byte/Page	250	10	10K
	5962-88525	04	U, X, Y, Z	X, A, C	32K x 8 E^2PROM Data Polling	Byte/Page	200	10	10K
	5962-88525	06	U, X, Y, Z	X, A, C	32K x 8 E^2PROM Data Polling	Byte/Page	150	10	10K

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-88525 **01 UX**	AT28C256-35UM/883
	5962-88525 **01 XX**	AT28C256-35DM/883
	5962-88525 **01 YX**	AT28C256-35LM/883
	5962-88525 **01 ZX**	AT28C256-35FM/883
	5962-88525 **02 UX**	AT28C256-30UM/883
	5962-88525 **02 XX**	AT28C256-30DM/883
	5962-88525 **02 YX**	AT28C256-30LM/883
	5962-88525 **02 ZX**	AT28C256-30FM/883
	5962-88525 **03 UX**	AT28C256-25UM/883
	5962-88525 **03 XX**	AT28C256-25DM/883
	5962-88525 **03 YX**	AT28C256-25LM/883
	5962-88525 **03 ZX**	AT28C256-25FM/883
	5962-88525 **04 UX**	AT28C256-20UM/883
	5962-88525 **04 XX**	AT28C256-20DM/883
	5962-88525 **04 YX**	AT28C256-20LM/883
	5962-88525 **04 ZX**	AT28C256-20FM/883
	5962-88525 **06 UX**	AT28C256-15UM/883
	5962-88525 **06 XX**	AT28C256-15DM/883
	5962-88525 **06 YX**	AT28C256-15LM/883
	5962-88525 **06 ZX**	AT28C256-15FM/883

Case Outline	
U	28U, 28 Pin, Ceramic Pin Grid Array (PGA)
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number *(continued)*

AT28C256E

Generic Number	Standardized Military Drawing Number				Description				
	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Speed(ms)	Endurance (Cycles)
28C256E	5962-88525	05	U, X, Y, Z	X, A, C	32K x 8 E^2PROM Data Polling	Byte/Page	250	10	100K

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-88525 **05 UX**	AT28C256E-25UM/883
	5962-88525 **05 XX**	AT28C256E-25DM/883
	5962-88525 **05 YX**	AT28C256E-25LM/883
	5962-88525 **05 ZX**	AT28C256E-25FM/883

Case Outline	
U	28U, 28 Pin, Ceramic Pin Grid Array (PGA)
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number *(continued)*

AT28C256F

Generic Number	Standardized Military Drawing Number				Description				
28C256F	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Speed(ms)	Endurance (Cycles)
	5962-88525	07	U, X, Y, Z	X, A, C	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	3	10K

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-88525 **07 UX**	AT28C256F-15UM/883
	5962-88525 **07 XX**	AT28C256F-15DM/883
	5962-88525 **07 YX**	AT28C256F-15LM/883
	5962-88525 **07 ZX**	AT28C256F-15FM/883

Case Outline	
U	28U, 28 Pin, Ceramic Pin Grid Array (PGA)
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

AT28HC256

Generic Number	Standardized Military Drawing Number				Description				
28HC256	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Speed(ms)	Endurance (Cycles)
	5962-88634	03	U, X, Y, Z	X, A, C	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	90	10	10K

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-88634 **03 UX**	AT28HC256-90UM/883
	5962-88634 **03 XX**	AT28HC256-90DM/883
	5962-88634 **03 YX**	AT28HC256-90LM/883
	5962-88634 **03 ZX**	AT28HC256-90FM/883

Case Outline	
U	28U, 28 Pin, Ceramic Pin Grid Array (PGA)
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number *(continued)*

AT28HC256F

Generic Number	Standardized Military Drawing Number				Description				
28HC256F	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Speed(ms)	Endurance (Cycles)
	5962-88634	04	U, X, Y, Z	X, A, C	32K x 8 E^2PROM Data Polling	Byte/Page	90	3	10K

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-88634 **04 UX**	AT28HC256F-90UM/883
	5962-88634 **04 XX**	AT28HC256F-90DM/883
	5962-88634 **04 YX**	AT28HC256F-90LM/883
	5962-88634 **04 ZX**	AT28HC256F-90FM/883

Case Outline	
U	28U, 28 Pin, Ceramic Pin Grid Array (PGA)
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number *(continued)*

AT28HC256L

Generic Number	Standardized Military Drawing Number				Description				
28HC256L	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Speed(ms)	Endurance (Cycles)
	5962-88634	01	U, X, Y, Z	X, A, C	32K x 8 E^2PROM Data Polling	Byte/Page	120	10	10K

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-88634 **01 UX**	AT28HC256L-12UM/883
	5962-88634 **01 XX**	AT28HC256L-12DM/883
	5962-88634 **01 YX**	AT28HC256L-12LM/883
	5962-88634 **01 ZX**	AT28HC256L-12FM/883

Case Outline	
U	28U, 28 Pin, Ceramic Pin Grid Array (PGA)
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number *(continued)*

AT28HC256LF

Generic Number	Standardized Military Drawing Number				Description				
28HC256LF	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Speed(ms)	Endurance (Cycles)
	5962-88634	02	U, X, Y, Z	X, A, C	32K x 8 E^2PROM Data Polling	Byte/Page	120	3	10K

Atmel Cage No.	Example: Atmel Order Number	Atmel Similar Part Number
1FN41	5962-88634 02 UX	AT28HC256LF-12UM/883
	5962-88634 02 XX	AT28HC256LF-12DM/883
	5962-88634 02 YX	AT28HC256LF-12LM/883
	5962-88634 02 ZX	AT28HC256LF-12FM/883

Case Outline	
U	28U, 28 Pin, Ceramic Pin Grid Array (PGA)
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number *(continued)*

AT28C010

Generic Number	Standardized Military Drawing Number				Description				
28C010	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Spd(ms)	Endurance (Cycles)
	5962-38267	01	X, Y, Z	X, A, C	128K x 8, 1-Mbit E^{2}PROM Data Polling	Byte/ Page	250	10	10K
	5962-38267	03	X, Y, Z	X, A, C	128K x 8, 1-Mbit E^{2}PROM Data Polling	Byte/ Page	200	10	10K
	5962-38267	05	X, Y, Z	X, A, C	128K x 8, 1-Mbit E^{2}PROM Data Polling	Byte/ Page	150	10	10K
	5962-38267	07	X, Y, Z	X, A, C	128K x 8, 1-Mbit E^{2}PROM Data Polling	Byte/ Page	120	10	10K

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-38267 **01M XX**	AT28C010-25BM/883
	5962-38267 **01M YX**	AT28C010-25LM/883
	5962-38267 **01M ZX**	AT28C010-25FM/883
	5962-38267 **03M XX**	AT28C010-20BM/883
	5962-38267 **03M YX**	AT28C010-20LM/883
	5962-38267 **03M ZX**	AT28C010-20FM/883
	5962-38267 **05M XX**	AT28C010-15BM/883
	5962-38267 **05M YX**	AT28C010-15LM/883
	5962-38267 **05M ZX**	AT28C010-15FM/883
	5962-38267 **07M XX**	AT28C010-12BM/883
	5962-38267 **07M YX**	AT28C010-12LM/883
	5962-38267 **07M ZX**	AT28C010-12FM/883

Case Outline	
X	32B, 32 Lead, 0.600" Wide, Ceramic Side Braze Dual Inline (Side Braze)
Y	44L, 44 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	32F, 32 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 2. Atmel SMD Part Types, Listed by SMD Number

5962-38267						
Atmel Order Number	**Atmel Similar Part Number**	**Circuit Description End Write Indicator**	**Write Mode**	**Access Time(ns)**	**Write Spd. (ms)**	**Endur. (Cycles)**
5962-38267 01M XX	AT28C010-25BM/883	128K x 8, 1-Mbit E^2PROM $\overline{\text{Data}}$ Polling	Byte/ Page	250	10	10K
5962-38267 01M YX	AT28C010-25LM/883	128K x 8, 1-Mbit E^2PROM $\overline{\text{Data}}$ Polling	Byte/ Page	250	10	10K
5962-38267 01M ZX	AT28C010-25FM/883	128K x 8, 1-Mbit E^2PROM $\overline{\text{Data}}$ Polling	Byte/ Page	250	10	10K
5962-38267 03M XX	AT28C010-20BM/883	128K x 8, 1-Mbit E^2PROM $\overline{\text{Data}}$ Polling	Byte/ Page	200	10	10K
5962-38267 03M YX	AT28C010-20LM/883	128K x 8, 1-Mbit E^2PROM $\overline{\text{Data}}$ Polling	Byte/ Page	200	10	10K
5962-38267 03M ZX	AT28C010-20FM/883	128K x 8, 1-Mbit E^2PROM $\overline{\text{Data}}$ Polling	Byte/ Page	200	10	10K
5962-38267 05M XX	AT28C010-15BM/883	128K x 8, 1-Mbit E^2PROM $\overline{\text{Data}}$ Polling	Byte/ Page	150	10	10K
5962-38267 05M YX	AT28C010-15LM/883	128K x 8, 1-Mbit E^2PROM $\overline{\text{Data}}$ Polling	Byte/ Page	150	10	10K
5962-38267 05M ZX	AT28C010-15FM/883	128K x 8, 1-Mbit E^2PROM $\overline{\text{Data}}$ Polling	Byte/ Page	150	10	10K
5962-38267 07M XX	AT28C010-12BM/883	128K x 8, 1-Mbit E^2PROM $\overline{\text{Data}}$ Polling	Byte/ Page	120	10	10K
5962-38267 07M YX	AT28C010-12LM/883	128K x 8, 1-Mbit E^2PROM $\overline{\text{Data}}$ Polling	Byte/ Page	120	10	10K
5962-38267 07M ZX	AT28C010-12FM/883	128K x 8, 1-Mbit E^2PROM $\overline{\text{Data}}$ Polling	Byte/ Page	120	10	10K

Table 2. Atmel SMD Part Types, Listed by SMD Number *(continued)*

5962-86063		
Atmel Order Number	**Atmel Similar Part Number**	**Circuit Description**	**Access Time (ns)**
5962-86063 01 XX	AT27C256R-20DM/883	32K x 8 EPROM	200
5962-86063 01 YX	AT27C256R-20LM/883	32K x 8 EPROM	200
5962-86063 01 ZX	AT27C256R-20KM/883	32K x 8 EPROM	200
5962-86063 02 XX	AT27C256R-25DM/883	32K x 8 EPROM	250
5962-86063 02 YX	AT27C256R-25LM/883	32K x 8 EPROM	250
5962-86063 02 ZX	AT27C256R-25KM/883	32K x 8 EPROM	250
5962-86063 03 XX	AT27C256R-30DM/883	32K x 8 EPROM	300
5962-86063 03 YX	AT27C256R-30LM/883	32K x 8 EPROM	300
5962-86063 03 ZX	AT27C256R-30KM/883	32K x 8 EPROM	300
5962-86063 04 XX	AT27C256R-17DM/883	32K x 8 EPROM	170
5962-86063 04 YX	AT27C256R-17LM/883	32K x 8 EPROM	170
5962-86063 04 ZX	AT27C256R-17KM/883	32K x 8 EPROM	170
5962-86063 05 XX	AT27C256R-15DM/883	32K x 8 EPROM	150
5962-86063 05 YX	AT27C256R-15LM/883	32K x 8 EPROM	150
5962-86063 05 ZX	AT27C256R-15KM/883	32K x 8 EPROM	150
5962-86063 06 XX	AT27C256R-12DM/883	32K x 8 EPROM	120
5962-86063 06 YX	AT27C256R-12LM/883	32K x 8 EPROM	120
5962-86063 06 ZX	AT27C256R-12KM/883	32K x 8 EPROM	120
5962-86063 07 XX	AT27C256R-90DM/883	32K x 8 EPROM	90
5962-86063 07 YX	AT27C256R-90LM/883	32K x 8 EPROM	90
5962-86063 07 ZX	AT27C256R-90KM/883	32K x 8 EPROM	90
5962-86063 08 XX	AT27HC256R-70DM/883	32K x 8 EPROM	70
5962-86063 08 YX	AT27HC256R-70LM/883	32K x 8 EPROM	70
5962-86063 08 ZX	AT27HC256R-70KM/883	32K x 8 EPROM	70

Table 2. Atmel SMD Part Types, Listed by SMD Number *(continued)*

5962-86805

Atmel Order Number	Atmel Similar Part Number	Circuit Description	Access Time (ns)
5962-86805 01 QX	AT27C1024-30DM/883	64K x 16, 1-Mbit EPROM	300
5962-86805 01 XX	AT27C1024-30LM/883	64K x 16, 1-Mbit EPROM	300
5962-86805 02 QX	AT27C1024-25DM/883	64K x 16, 1-Mbit EPROM	250
5962-86805 02 XX	AT27C1024-25LM/883	64K x 16, 1-Mbit EPROM	250
5962-86805 03 QX	AT27C1024-20DM/883	64K x 16, 1-Mbit EPROM	200
5962-86805 03 XX	AT27C1024-20LM/883	64K x 16, 1-Mbit EPROM	200
5962-86805 04 QX	AT27C1024-17DM/883	64K x 16, 1-Mbit EPROM	170
5962-86805 04 XX	AT27C1024-17LM/883	64K x 16, 1-Mbit EPROM	170
5962-86805 05 QX	AT27C1024-15DM/883	64K x 16, 1-Mbit EPROM	150
5962-86805 05 XX	AT27C1024-15LM/883	64K x 16, 1-Mbit EPROM	150
5962-86805 06 QX	AT27C1024-12DM/883	64K x 16, 1-Mbit EPROM	120
5962-86805 06 XX	AT27C1024-12LM/883	64K x 16, 1-Mbit EPROM	120
5962-86805 07 QX	AT27HC1024-90DM/883	64K x 16, 1-Mbit EPROM	90
5962-86805 07 XX	AT27HC1024-90LM/883	64K x 16, 1-Mbit EPROM	90
5962-86805 08 QX	AT27HC1024-70DM/883	64K x 16, 1-Mbit EPROM	70
5962-86805 08 XX	AT27HC1024-70LM/883	64K x 16, 1-Mbit EPROM	70

5962-87514

Atmel Order Number	Atmel Similar Part Number	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Spd. (ms)	Endur. (Cycles)
5962-87514 06 XX	AT28PC64-35DM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	350	2	10K
5962-87514 06 YX	AT28PC64-35LM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	350	2	10K
5962-87514 07 XX	AT28PC64-30DM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	300	2	10K
5962-87514 07 YX	AT28PC64-30LM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	300	2	10K
5962-87514 08 XX	AT28PC64-25DM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	2	10K
5962-87514 08 YX	AT28PC64-25LM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	2	10K
5962-87514 09 XX	AT28PC64-20DM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	200	2	10K

Table 2. Atmel SMD Part Types, Listed by SMD Number *(continued)*

5962-87514 (continued)

Atmel Order Number	Atmel Similar Part Number	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Spd. (ms)	Endur. (Cycles)
5962-87514 09 YX	AT28PC64-20LM/883	8K x 8 E^2PROM Data Polling	Byte/Page	200	2	10K
5962-87514 10 XX	AT28HC64L-12DM/883	8K x 8 E^2PROM Data Polling	Byte/Page	120	2	10K
5962-87514 10 YX	AT28HC64L-12LM/883	8K x 8 E^2PROM Data Polling	Byte/Page	120	2	10K
5962-87514 11 XX	AT28HC64L-90DM/883	8K x 8 E^2PROM Data Polling	Byte/Page	90	2	10K
5962-87514 11 YX	AT28HC64L-90LM/883	8K x 8 E^2PROM Data Polling	Byte/Page	90	2	10K
5962-87514 12 XX	AT28HC64L-70DM/883	8K x 8 E^2PROM Data Polling	Byte/Page	70	2	10K
5962-87514 12 YX	AT28HC64L-70LM/883	8K x 8 E^2PROM Data Polling	Byte/Page	70	2	10K
5962-87514 13 XX	AT28C64-35DM/883	8K x 8 E^2PROM Rdy/Busy	Byte	350	1	10K
5962-87514 13 YX	AT28C64-35LM/883	8K x 8 E^2PROM Rdy/Busy	Byte	350	1	10K
5962-87514 13 ZX	AT28C64-35FM/883	8K x 8 E^2PROM Rdy/Busy	Byte	350	1	10K
5962-87514 14 XX	AT28C64-30DM/883	8K x 8 E^2PROM Rdy/Busy	Byte	300	1	10K
5962-87514 14 YX	AT28C64-30LM/883	8K x 8 E^2PROM Rdy/Busy	Byte	300	1	10K
5962-87514 15 XX	AT28C64-25DM/883	8K x 8 E^2PROM Rdy/Busy	Byte	250	1	10K
5962-87514 15 YX	AT28C64-25LM/883	8K x 8 E^2PROM Rdy/Busy	Byte	250	1	10K
5962-87514 15 ZX	AT28C64-25FM/883	8K x 8 E^2PROM Rdy/Busy	Byte	250	1	10K
5962-87514 16 XX	AT28C64-20DM/883	8K x 8 E^2PROM Rdy/Busy	Byte	200	1	10K
5962-87514 16 YX	AT28C64-20LM/883	8K x 8 E^2PROM Rdy/Busy	Byte	200	1	10K
5962-87514 17 XX	AT28C64-15DM/883	8K x 8 E^2PROM Rdy/Busy	Byte	150	1	10K
5962-87514 17 YX	AT28C64-15LM/883	8K x 8 E^2PROM Rdy/Busy	Byte	150	1	10K
5962-87514 18 XX	AT28C64X-35DM/883	8K x 8 E^2PROM Data Polling	Byte	350	1	10K

Table 2. Atmel SMD Part Types, Listed by SMD Number *(continued)*

5962-87514 (continued)

Atmel Order Number	Atmel Similar Part Number	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Spd. (ms)	Endur. (Cycles)
5962-87514 18 YX	AT28C64X-35LM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	350	1	10K
5962-87514 19 XX	AT28C64X-30DM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	300	1	10K
5962-87514 19 YX	AT28C64X-30LM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	300	1	10K
5962-87514 20 XX	AT28C64X-25DM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	250	1	10K
5962-87514 20 YX	AT28C64X-25LM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	250	1	10K
5962-87514 20 ZX	AT28C64X-25FM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	250	1	10K
5962-87514 21 XX	AT28C64X-20DM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	200	1	10K
5962-87514 21 YX	AT28C64X-20LM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	200	1	10K
5962-87514 22 XX	AT28C64X-15DM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	150	1	10K
5962-87514 22 YX	AT28C64X-15LM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	150	1	10K

Table 2. Atmel SMD Part Types, Listed by SMD Number *(continued)*

5962-87515			
Atmel Order Number	**Atmel Similar Part Number**	**Circuit Description**	**Access Time (ns)**
5962-87515 01 JX	AT27HC641R-45DM/883	8K x 8 [UV] PROM	45
5962-87515 01 KX	AT27HC641R-45CM/883	8K x 8 [UV] PROM	45
5962-87515 01 LX	AT27HC642R-45DM/883	8K x 8 [UV] PROM	45
5962-87515 01 3X	AT27HC641R-45LM/883	8K x 8 [UV] PROM	45
5962-87515 02 JX	AT27HC641R-55DM/883	8K x 8 [UV] PROM	55
5962-87515 02 KX	AT27HC641R-55CM/883	8K x 8 [UV] PROM	55
5962-87515 02 LX	AT27HC642R-55DM/883	8K x 8 [UV] PROM	55
5962-87515 02 3X	AT27HC641R-55LM/883	8K x 8 [UV] PROM	55
5962-87515 03 JX	AT27HC641R-70DM/883	8K x 8 [UV] PROM	70
5962-87515 03 KX	AT27HC641R-70CM/883	8K x 8 [UV] PROM	70
5962-87515 03 LX	AT27HC642R-70DM/883	8K x 8 [UV] PROM	70
5962-87515 03 3X	AT27HC641R-70LM/883	8K x 8 [UV] PROM	70
5962-87515 04 JX	AT27HC641R-90DM/883	8K x 8 [UV] PROM	90
5962-87515 04 KX	AT27HC641R-90CM/883	8K x 8 [UV] PROM	90
5962-87515 04 LX	AT27HC642R-90DM/883	8K x 8 [UV] PROM	90
5962-87515 04 3X	AT27HC641R-90LM/883	8K x 8 [UV] PROM	90

Table 2. Atmel SMD Part Types, Listed by SMD Number *(continued)*

5962-87539

Atmel Order Number	Atmel Similar Part Number	Circuit Description	Access Time (ns)
5962-87539 01 KX	AT22V10-25YM/883	22-Input, 10-Output and-or-Logic Array	25
5962-87539 01 LX	AT22V10-25DM/883	22-Input, 10-Output and-or-Logic Array	25
5962-87539 01 3X	AT22V10-25LM/883	22-Input, 10-Output and-or-Logic Array	25
5962-87539 02 KX	AT22V10-30YM/883	22-Input, 10-Output and-or-Logic Array	30
5962-87539 02 LX	AT22V10-30DM/883	22-Input, 10-Output and-or-Logic Array	30
5962-87539 02 3X	AT22V10-30LM/883	22-Input, 10-Output and-or-Logic Array	30
5962-87539 03 KX	AT22V10-40YM/883	22-Input, 10-Output and-or-Logic Array	40
5962-87539 03 LX	AT22V10-40DM/883	22-Input, 10-Output and-or-Logic Array	40
5962-87539 03 3X	AT22V10-40LM/883	22-Input, 10-Output and-or-Logic Array	40
5962-87539 04 KX	AT22V10-20YM/883	22-Input, 10-Output and-or-Logic Array	20
5962-87539 04 LX	AT22V10-20DM/883	22-Input, 10-Output and-or-Logic Array	20
5962-87539 04 3X	AT22V10-20LM/883	22-Input, 10-Output and-or-Logic Array	20

5962-87648

Atmel Order Number	Atmel Similar Part Number	Circuit Description	Access Time (ns)
5962-87648 01 XX	AT27C512R-15DM/883	64K x 8 EPROM	150
5962-87648 01 YX	AT27C512R-15LM/883	64K x 8 EPROM	150
5962-87648 01 ZX	AT27C512R-15KM/883	64K x 8 EPROM	150
5962-87648 02 XX	AT27C512R-20DM/883	64K x 8 EPROM	200
5962-87648 02 YX	AT27C512R-20LM/883	64K x 8 EPROM	200
5962-87648 02 ZX	AT27C512R-20KM/883	64K x 8 EPROM	200
5962-87648 03 XX	AT27C512R-25DM/883	64K x 8 EPROM	250
5962-87648 03 YX	AT27C512R-25LM/883	64K x 8 EPROM	250
5962-87648 03 ZX	AT27C512R-25KM/883	64K x 8 EPROM	250
5962-87648 04 XX	AT27C512R-12DM/883	64K x 8 EPROM	120
5962-87648 04 YX	AT27C512R-12LM/883	64K x 8 EPROM	120
5962-87648 04 ZX	AT27C512R-12KM/883	64K x 8 EPROM	120

Table 2. Atmel SMD Part Types, Listed by SMD Number *(continued)*

5962-88525

Atmel Order Number	Atmel Similar Part Number	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Spd. (ms)	Endur. (Cycles)
5962-88525 01 UX	AT28C256-35UM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	350	10	10K
5962-88525 01 XX	AT28C256-35DM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	350	10	10K
5962-88525 01 YX	AT28C256-35LM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte Page	350	10	10K
5962-88525 01 ZX	AT28C256-35FM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	350	10	10K
5962-88525 02 UX	AT28C256-30UM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	300	10	10K
5962-88525 02 XX	AT28C256-30DM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	300	10	10K
5962-88525 02 YX	AT28C256-30LM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	300	10	10K
5962-88525 02 ZX	AT28C256-30FM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	300	10	10K
5962-88525 03 UX	AT28C256-25UM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	10	10K
5962-88525 03 XX	AT28C256-25DM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	10	10K
5962-88525 03 YX	AT28C256-25LM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	10	10K
5962-88525 03 ZX	AT28C256-25FM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	10	10K
5962-88525 04 UX	AT28C256-20UM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	200	10	10K
5962-88525 04 XX	AT28C256-20DM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	200	10	10K
5962-88525 04 YX	AT28C256-20LM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	200	10	10K
5962-88525 04 ZX	AT28C256-20FM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	200	10	10K
5962-88525 05 UX	AT28C256E-25UM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	10	100K
5962-88525 05 XX	AT28C256E-25DM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	10	100K
5962-88525 05 YX	AT28C256E-25LM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	10	100K
5962-88525 05 ZX	AT28C256E-25FM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	10	100K

Table 2. Atmel SMD Part Types, Listed by SMD Number *(continued)*

5962-88525 (continued)

Atmel Order Number	Atmel Similar Part Number	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Spd. (ms)	Endur. (Cycles)
5962-88525 06 UX	AT28C256-15UM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	10	10K
5962-88525 06 XX	AT28C256-15DM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	10	10K
5962-88525 06 YX	AT28C256-15LM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	10	10K
5962-88525 06 ZX	AT28C256-15FM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	10	10K
5962-88525 07 UX	AT28C256F-15UM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	3	10K
5962-88525 07 XX	AT28C256F-15DM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	3	10K
5962-88525 07 YX	AT28C256F-15LM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	3	10K
5962-88525 07 ZX	AT28C256F-15FM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	3	10K

Table 2. Atmel SMD Part Types, Listed by SMD Number *(continued)*

5962-88634						
Atmel Order Number	**Atmel Similar Part Number**	**Circuit Description End Write Indicator**	**Write Mode**	**Access Time(ns)**	**Write Spd. (ms)**	**Endur. (Cycles)**
5962-88634 01 UX	AT28HC256L-12UM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	120	10	10K
5962-88634 01 XX	AT28HC256L-12DM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	120	10	10K
5962-88634 01 YX	AT28HC256L-12LM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	120	10	10K
5962-88634 01 ZX	AT28HC256L-12FM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	120	10	10K
5962-88634 02 UX	AT28HC256LF-12UM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	120	3	10K
5962-88634 02 XX	AT28HC256LF-12DM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	120	3	10K
5962-88634 02 YX	AT28HC256LF-12LM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	120	3	10K
5962-88634 02 ZX	AT28HC256LF-12FM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	120	3	10K
5962-88634 03 UX	AT28HC256-90UM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	90	10	10K
5962-88634 03 XX	AT28HC256-90DM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	90	10	10K
5962-88634 03 YX	AT28HC256-90LM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	90	10	10K
5962-88634 03 ZX	AT28HC256-90FM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	90	10	10K
5962-88634 04 UX	AT28HC256F-90UM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	90	3	10K
5962-88634 04 XX	AT28HC256F-90DM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	90	3	10K
5962-88634 04 YX	AT28HC256F-90LM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	90	3	10K
5962-88634 04 ZX	AT28HC256F-90FM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	90	3	10K

5962-88670

Atmel Order Number	Atmel Similar Part Number	Circuit Description	Access Time (ns)
5962-88670 01 KX	AT22V10-25FM/883	22-Input, 10-Output and-or-Logic Array	25
5962-88670 01 LX	AT22V10-25GM/883	22-Input, 10-Output and-or-Logic Array	25
5962-88670 01 3X	AT22V10-25NM/883	22-Input, 10-Output and-or-Logic Array	25
5962-88670 02 KX	AT22V10-30FM/883	22-Input, 10-Output and-or-Logic Array	30
5962-88670 02 LX	AT22V10-30GM/883	22-Input, 10-Output and-or-Logic Array	30
5962-88670 02 3X	AT22V10-30NM/883	22-Input, 10-Output and-or-Logic Array	30
5962-88670 03 KX	AT22V10-40FM/883	22-Input, 10-Output and-or-Logic Array	40
5962-88670 03 LX	AT22V10-40GM/883	22-Input, 10-Output and-or-Logic Array	40
5962-88670 03 3X	AT22V10-40NM/883	22-Input, 10-Output and-or-Logic Array	40
5962-88670 04 KX	AT22V10-20FM/883	22-Input, 10-Output and-or-Logic Array	20
5962-88670 04 LX	AT22V10-20GM/883	22-Input, 10-Output and-or-Logic Array	20
5962-88670 04 3X	AT22V10-20NM/883	22-Input, 10-Output and-or-Logic Array	20
5962-88670 05 KX	AT22V10-15FM/883	22-Input, 10-Output and-or-Logic Array	15
5962-88670 05 LX	AT22V10-15GM/883	22-Input, 10-Output and-or-Logic Array	15
5962-88670 05 3X	AT22V10-15NM/883	22-Input, 10-Output and-or-Logic Array	15

5962-88724

Atmel Order Number	Atmel Similar Part Number	Circuit Description	Access Time (ns)
5962-88724 01 KX	AT22V10L-25YM/883	22-Input, 10-Output and-or-Logic Array	25
5962-88724 01 LX	AT22V10L-25DM/883	22-Input, 10-Output and-or-Logic Array	25
5962-88724 01 3X	AT22V10L-25LM/883	22-Input, 10-Output and-or-Logic Array	25
5962-88724 02 KX	AT22V10L-30YM/883	22-Input, 10-Output and-or-Logic Array	30
5962-88724 02 LX	AT22V10L-30DM/883	22-Input, 10-Output and-or-Logic Array	30
5962-88724 02 3X	AT22V10L-30LM/883	22-Input, 10-Output and-or-Logic Array	30
5962-88724 03 KX	AT22V10L-40YM/883	22-Input, 10-Output and-or-Logic Array	40
5962-88724 03 LX	AT22V10L-40DM/883	22-Input, 10-Output and-or-Logic Array	40
5962-88724 03 3X	AT22V10L-40LM/883	22-Input, 10-Output and-or-Logic Array	40
5962-88724 04 KX	AT22V10L-20YM/883	22-Input, 10-Output and-or-Logic Array	20
5962-88724 04 LX	AT22V10L-20DM/883	22-Input, 10-Output and-or-Logic Array	20
5962-88724 04 3X	AT22V10L-20LM/883	22-Input, 10-Output and-or-Logic Array	20

Table 2. Atmel SMD Part Types, Listed by SMD Number *(continued)*

5962-88726

Atmel Order Number	Atmel Similar Part Number	Circuit Description	Access Time (ns)
5962-88726 01 LX	ATV750-40DM/883	22-Input, 10-Output and-or-Logic Array	40
5962-88726 01 3X	ATV750-40LM/883	22-Input, 10-Output and-or-Logic Array	40
5962-88726 02 LX	ATV750-35DM/883	22-Input, 10-Output and-or-Logic Array	35
5962-88726 02 3X	ATV750-35LM/883	22-Input, 10-Output and-or-Logic Array	35
5962-88726 03 LX	ATV750-25DM/883	22-Input, 10-Output and-or-Logic Array	25
5962-88726 03 3X	ATV750-25LM/883	22-Input, 10-Output and-or-Logic Array	25
5962-88726 04 LX	ATV750-20DM/883	22-Input, 10-Output and-or-Logic Array	20
5962-88726 04 3X	ATV750-20LM/883	22-Input, 10-Output and-or-Logic Array	20
5962-88726 06 LX	ATV750L-30DM/883	22-Input, 10-Output and-or-Logic Array	30
5962-88726 06 3X	ATV750L-30LM/883	22-Input, 10-Output and-or-Logic Array	30
5962-88726 07 LX	ATV750L-25DM/883	22-Input, 10-Output and-or-Logic Array	25
5962-88726 07 3X	ATV750L-25LM/883	22-Input, 10-Output and-or-Logic Array	25

5962-89614

Atmel Order Number	Atmel Similar Part Number	Circuit Description	Access Time (ns)
5962-89614 01M XX	AT27C010-30DM/883	128K x 8, 1-Mbit EPROM	300
5962-89614 01M YX	AT27C010-30LM/883	128K x 8, 1-Mbit EPROM	300
5962-89614 02M XX	AT27C010-25DM/883	128K x 8, 1-Mbit EPROM	250
5962-89614 02M YX	AT27C010-25LM/883	128K x 8, 1-Mbit EPROM	250
5962-89614 03M XX	AT27C010-20DM/883	128K x 8, 1-Mbit EPROM	200
5962-89614 03M YX	AT27C010-20LM/883	128K x 8, 1-Mbit EPROM	200
5962-89614 04M XX	AT27C010-17DM/883	128K x 8, 1-Mbit EPROM	170
5962-89614 04M YX	AT27C010-17LM/883	128K x 8, 1-Mbit EPROM	170
5962-89614 05M XX	AT27C010-15DM/883	128K x 8, 1-Mbit EPROM	150
5962-89614 05M YX	AT27C010-15LM/883	128K x 8, 1-Mbit EPROM	150
5962-89614 06M XX	AT27C010-12DM/883	128K x 8, 1-Mbit EPROM	120
5962-89614 06M YX	AT27C010-12LM/883	128K x 8, 1-Mbit EPROM	120

Table 2. Atmel SMD Part Types, Listed by SMD Number *(continued)*

5962-89755

Atmel Order Number	Atmel Similar Part Number	Circuit Description	Access Time (ns)
5962-89755 01 KX	AT22V10L-25FM/883	22-Input, 10-Output and-or-Logic Array	25
5962-89755 01 LX	AT22V10L-25GM/883	22-Input, 10-Output and-or-Logic Array	25
5962-89755 01 3X	AT22V10L-25NM/883	22-Input, 10-Output and-or-Logic Array	25
5962-89755 02 KX	AT22V10L-30FM/883	22-Input, 10-Output and-or-Logic Array	30
5962-89755 02 LX	AT22V10L-30GM/883	22-Input, 10-Output and-or-Logic Array	30
5962-89755 02 3X	AT22V10L-30NM/883	22-Input, 10-Output and-or-Logic Array	30
5962-89755 03 KX	AT22V10L-40FM/883	22-Input, 10-Output and-or-Logic Array	40
5962-89755 03 LX	AT22V10L-40GM/883	22-Input, 10-Output and-or-Logic Array	40
5962-89755 03 3X	AT22V10L-40NM/883	22-Input, 10-Output and-or-Logic Array	40
5962-89755 04 KX	AT22V10L-20FM/883	22-Input, 10-Output and-or-Logic Array	20
5962-89755 04 LX	AT22V10L-20GM/883	22-Input, 10-Output and-or-Logic Array	20
5962-89755 04 3X	AT22V10L-20NM/883	22-Input, 10-Output and-or-Logic Array	20

5962-91545

Atmel Order Number	Atmel Similar Part Number	Circuit Description	Access Time (ns)
5962-91545 01M QX	ATV2500H-35DM/883	38-Input, 24-Output and-or-Logic Array	35
5962-91545 01M XX	ATV2500H-35LM/883	38-Input, 24-Output and-or-Logic Array	35
5962-91545 01M YX	ATV2500H-35KM/883	38-Input, 24-Output and-or-Logic Array	35
5962-91545 02M QX	ATV2500H-25DM/883	38-Input, 24-Output and-or-Logic Array	25
5962-91545 02M XX	ATV2500H-25LM/883	38-Input, 24-Output and-or-Logic Array	25
5962-91545 02M YX	ATV2500H-25KM/883	38-Input, 24-Output and-or-Logic Array	25
5962-91545 03M QX	ATV2500L-30DM/883	38-Input, 24-Output and-or-Logic Array	30
5962-91545 03M XX	ATV2500L-30LM/883	38-Input, 24-Output and-or-Logic Array	30
5962-91545 03M YX	ATV2500L-30KM/883	38-Input, 24-Output and-or-Logic Array	30

Atmel Modified Class S Integrated Circuit Test Flow

Introduction

Atmel has expanded upon and modified standard "Class S" testing procedures to accommodate up-to-date small-geometry integrated circuit processing methods which are not covered in the standard Class S Flow. This document describes Atmel's current Modified Class S Flow.

Modified Class S Flow

Screen Requirements	Atmel Procedure Number	MIL-STD-883D (as applicable)
Wafer Lot Acceptance		MIL-STD-883D, M5007[4]
Assembly		
Wafer Mount	1980-004	
Wafer Saw	1980-003	
Wafer Clean	1980-005	
Die Sort, Manual	1980-029	
2nd Optical, Military		Method 2010, Cond A, Class S Criteria
Package Clean	1980-037	
Die Attach	Package Related	Mark Wafer No. on Pkg
Shear Test	1980-038	Method 2019
Inspect [1]	1980-050	Method 2010, Cond A [5]
Wire Bond	1980-013	
Wire Bond Pull Test	1980-039	Method 2011, Cond D
Non Dest. Bond Pull	1980-039	Method 2023
3rd Optical, Military	1980-050	Method 2010 Cond A, Class S Criteria
QA Internal Visual	240-037	Method 2010, Cond A
Preseal Clean	1980-040	Nitrogen Blow Off
Preseal Bake, Vacuum	1980-053	
Seal	Package Related	
Mark	1980-032	
Production Screens		
Temperature Cycling	100%	Method 1010 Cond C
Constant Acceleration	100%	Method 2001 Cond E
Visual Inspect [6]		
Pind [1]	100%	Method 2020 Cond A
Serialization	100%	
Pre-burn-in	100%	
Test @ 25°C		

Continued on Next Page

Modified Class S Flow, *Continued*

Screen Requirements	Atmel Procedure Number	MIL-STD-883D (as applicable)
Burn-in (3)	100%	Method 1015, 240 hours
Interim Elect. @ 25°C (7)	100%	
HRTB Burn-in (Option) (7)		M1015, Cond A or C, 72 hours
Post burn-in Elect 25°C	100%	Read and Record Subgroup 1
Percent Defective 3%, 5%	100%	Method 5004 p 3.5.1
Final Electrical Test	100%	Method 5004 p 3.5.2
Fine, Gross Seal (1)	100% 9	Method 1014
Radiographic (1)	100%	Method 2012
Quality Conformance Inspection Sample Selection	Sample	Method 5005 p 3.5

Quality Conformance Inspections, Group A Electrical Tests

Perform for Every Lot

Inspection		-883 Method	100% Test	Sample/ Accept
Subgroup 1	Static Tests @ 25°C	5005	yes	116/0
Subgroup 2	Static Tests @ 125°C	5005	yes	116/0
Subgroup 3	Static Tests @ -55°C	5005	yes	116/0
Subgroup 4	Dynamic @ 25°C	5005	yes	116/0
Subgroup 5	Dynamic @ 125°C	5005	yes	116/0
Subgroup 6	Dynamic @ -55°C	5005	yes	116/0
Subgroup 7	Functional @ 25°C	5005	yes	116/0
Subgroup 8a	+125°C Functional Tests	5005	yes	116/0
Subgroup 8b	-55°C Functional Tests	5005	yes	116/0
Subgroup 9	Switching @ 25°C	5005	yes	116/0

Notes:

1. This screening procedure shall be performed within the sequence options allowed by MIL-STD-883, Method 5004, but not necessarily in the sequence shown.
2. Parametric Read and Record requirements shall exist for this procedure only when delta parametric limits are required in the PDA procedure determination by customer specification.
3. Condition F of MIL-STD-883 Method 1015 shall not apply. Paragraph 3.4.2 of MIL-STD-883 Method 5004 shall not apply.
4. Products made by Atmel do not comply to several requirements of MIL-STD-883 Method 5007. These include wafer, metal and glassivation thickness, where thickness limits are different by design, and SEM inspection where lot and sample size requirements of method 5007 are not compatible with modern equipment capacity. An alternative Atmel Wafer Lot Acceptance method exists and shall be used in place of method 5007. It is available upon request (when non-disclosure agreements exist).
5. Atmel shall take limited exception to compliance with MIL-STD-883 method 2010 for all contracts and all product. Atmel will physically perform the inspection to the best of its ability but will not guarantee absence of die visual defects in total or to any specified LTPD limit. The extreme complexity and small feature size of Atmel integrated circuit die make it physically impossible to inspect 100% of die features for the defect excluded by Method 2010.
6. This procedure will be performed at the option of Atmel. No lot acceptance criteria shall be imposed for this procedure.
7. Interim electrical screen and HTRB burn-in shall be performed only when required by customer specification. When they are performed, Read and Record requirements shall exist only when delta parametric limits are required as part of PDA determination by customer specification.
8. PIND shall be waived for non-JAN and non-883 compliant product unless specifically required by customer specification.
9. Shall be performed after all lead forming, clipping or straightening operations and only in sequence allowed by MIL-STD-883, Method 5004.
10. Shall be performed in sequence allowed by MIL-STD-883 method 5004. If any lead forming, clipping, or straightening operations occur after this procedure, a sample seal test shall be performed on the lot (Fine and Gross with LTPD = 2, C = 0).

Quality Conformance Inspections, Group B Tests

S = Sample Size / Accept Number

MIL-STD-883	883 Method	5005 Class S
Subgroup 1		
a. Physical Dimensions (1)	2016	yes, S = 2(0)
b. Internal Water Vapor Content	1018	yes (1,4,7), S = 3(0) or 5(1)
Subgroup 2 6		
a. Resistance to Solvents, S = 4(0)	2015	yes
b. Internal Vis and Mech, S = 2(0)	2013 and 2014	yes
c. Bond Strength, LTPD = 10 (2)	2011	yes
d. Die Shear Test	2019	yes
Subgroup 3		
a. Solderability (3,6), LTPD = 10	2003	yes
Subgroup 4 S = 2(0)		
a. Lead Integrity, S = 2(0)	2004 or 2028	yes
b. Seal Test Fine and Gross	1014	yes
c. Lid Torque, S = 2(0)	2024	yes (4)
Subgroup 5		
a. Steady State Life	1005	yes
b. Electrical Parameters	*	yes (8)
Subgroup 6		
a. Temp Cycle, 100 cycles	1010, Cond C	yes
b. Constant Acceleration	2001, Cond E	yes
c. Seal Test Fine and Gross	1014	yes
d. Electrical Parameters		yes (8), R and R
e. Die Shear Strength	2019	
Subgroup 7		
a. ESD	3015	yes (5), S = 3(0) / 15(0)
b. Electrical Parameters	group A, sub 1	yes (5)

*Per Device Spec.

Notes:

1. Not required for Method 5005 devices if Group D testing is performed.
2. LTPD = Number of bond pulls selected from a minimum of four devices.
3. Required number of leads must be contained in a minimum of three devices. Must be post Burn-In devices.
4. Applies only to packages with a glass-frit seal.
5. Unless otherwise specified test shall be performed for initial Qualification and product redesign as a minimum.
6. Electrical rejects may be used.
7. Required only when package contains a dessicant.
8. End point electricals as specified in applicable detail drawing.

Quality Conformance Inspections, Group D Tests

Perform Every Six Months for Method 5004, 5005 Devices

MIL-STD-883 Inspection	883 Method	5005 Class S
Subgroup 1 (1)		
a. Physical Dim, LTPD = 15	2016	yes
Subgroup 2		
a. Lead Integrity	2004 or 2028	yes
b. Seal Test Fine and Gross	1014	yes
Subgroup 3		LTPD = 15
a. Thermal Shock	1011	yes
b. Temperature Cycle	1010	yes
c. Moisture Rest.	1004	yes
d. Seal Test Fine and Gross	1014	yes
e. Visual Examination	1004, 1010	yes
f. Electrical Parameters	*	yes (2)
Subgroup 4		LTPD = 15
a. Mechanical Shock	2002	yes
b. Vibration Var. Frequency	2007	yes
c. Constant Acceleration	2001	yes
d. Seal Test Fine and Gross	1014	yes
e. Visual Examination	1010, 1011	yes
f. Electrical Parameters	*	yes (2)
Subgroup 5 (1)		S = 15(0)
a. Salt Atmosphere	1009	yes
b. Seal Test Fine and Gross (4)	1014	yes
c. Visual Examination	1009	yes
Subgroup 6 (1)		S = 3(0) or 5(1)
Internal Water Vapor Content	1018	yes
Subgroup 7 (1)		S = 15(0)
Adhesion of Lead Finish	2025	yes
Subgroup 8 (3)		S = 5(0)
Lid Torque	2024	yes

*Per Device Spec.

Notes:
1. Electrical rejects may be used.
2. Per applicable detail drawing.
3. Applies to package with glass frit-seal only.
4. Only for packages with leads exiting through a glass seal.

Quality Conformance Inspections, Group E Tests

Group E testing will be performed per device / customer specification.

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PROMs 5

SRAMs 6

EPLDs 7

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Product Information 1

E²PROMs 2

PEROMs (Flash) 3

EPROMs 4

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Section 16

Die Products

E^2PROM Die products 16-3

E^2PROM Die Products

Features

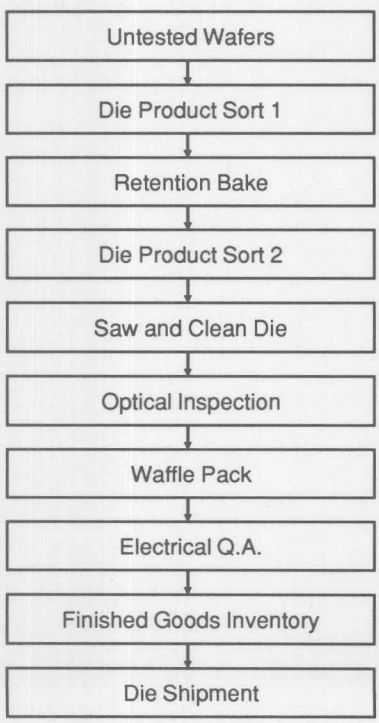
- **High Performance CMOS Technology**
- **Low Power Dissipation - Active and Standby**
- **Hardware Data Protection Features**
- **DATA Polling for End of Write Detection**
- **High Reliability**
  - **Endurance: 10^4 Cycles**
  - **Data Retention: 10 years**
- **Single 5 V ± 10% Supply**
- **CMOS Compatible Inputs and Outputs**
- **0°C to +70°C Operating Range**
- **Typical Die Thickness of 22 Mils**

Description

To facilitate custom packaging, some Atmel E^2PROMS are available in die form. All Atmel E^2PROM die products are 100% electrically tested in wafer form and visually inspected after saw and clean. Atmel's E^2PROM die products are processed with an advanced CMOS floating gate technology. As with all Atmel products, they are designed and tested to ensure high quality and manufacturability. The devices may include such features as internal error correction for extended endurance and improved data retention characteristics.

Test Flow

Atmel's die product sort testing incorporates comprehensive functional and parametric tests into wafer level tests. The typical Atmel E^2PROM die test flow is outlined below.



Testing

Die product sort test 1 includes checks for basic D.C. parameters such as I_{CC} and input leakage as well as for A.C. switching parameters. Data pattern testing is included to guarantee the functionality of each bit and to guard against pattern sensitivity. Several oxide stress tests are included to reduce the likelihood of infant mortality failures.

The data retention bake is included to ensure the integrity of the core cell oxides. A pattern is written to each die at the end of die sort test 1. The wafers are then subjected to a high temperature bake. After the bake, the pattern written in die sort test 1 is verified by die sort test 2.

A final quality assurance test is performed on each assembly lot. A sample of the dice ready to ship is selected and electrically examined.

Die Product Offering

Die products are guaranteed across the commercial temperature operating range. The following E^2PROM die products are currently available from Atmel[1]:

AT28C16	AT28LV64
AT28C17	AT28C256
AT28C64	AT28HC256L
AT28PC64	AT28HC291L
AT28HC64L	AT28C010

Handling and Die Information

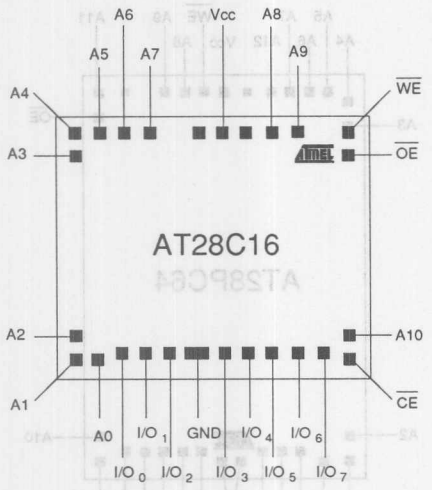
Handling instructions for E^2PROM die and other information needed for using E^2PROM die are available from Atmel.

Note: 1. The Atmel logo on the following die maps is not to scale and is only shown as a reference to properly orient the die.

AT28C16 Die Map

Die Size: 137 X 117 mils

Connect Substrate to Ground



Die Pad Coordinates *

Signal Name	X (µ)	Y (µ)
A_0	-1270	1130
A_1	-1270	1420
A_2	-920	1420
A_3	950	1370
A_4	1230	1370
A_5	1230	1140
A_6	1230	900
A_7	1230	660
A_8	1230	-680
A_9	1230	-920
A_{10}	-1000	-1630
I/O_0	-1190	870

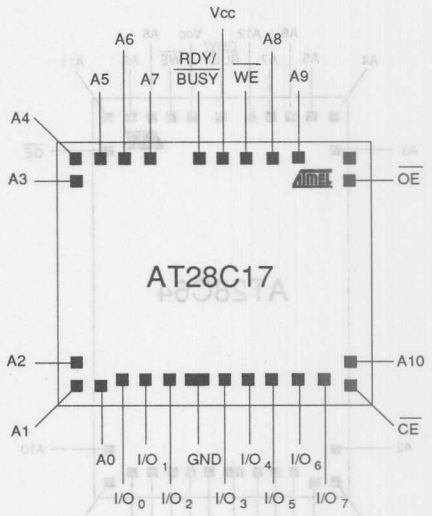
Signal Name	X (µ)	Y (µ)
I/O_1	-1190	610
I/O_2	-1190	360
I/O_3	-1190	-230
I/O_4	-1190	-480
I/O_5	-1190	-740
I/O_6	-1190	-990
I/O_7	-1190	-1250
GND	-1190	60
V_{cc}	1230	-210
$\overline{WE}$	1230	-1630
$\overline{OE}$	1000	-1630
$\overline{CE}$	-1230	-1630

* Coordinates are calculated from die center point

AT28C17 Die Map

Die Size: 137 X 117 mils

Connect Substrate to Ground



Die Pad Coordinates *

Signal Name	X (µ)	Y (µ)
A_0	-1270	1130
A_1	-1270	1420
A_2	-920	1420
A_3	950	1370
A_4	1230	1370
A_5	1230	1140
A_6	1230	900
A_7	1230	660
A_8	1230	-680
A_9	1230	-920
A_{10}	-1000	-1630
I/O_0	-1190	870
I/O_1	-1190	610

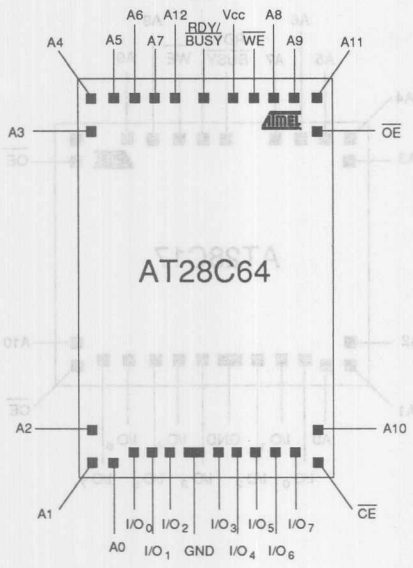
Signal Name	X (µ)	Y (µ)
I/O_2	-1190	360
I/O_3	-1190	-230
I/O_4	-1190	-480
I/O_5	-1190	-740
I/O_6	-1190	-990
I/O_7	-1190	-1250
RDY/$\overline{BSY}$	1230	100
GND	-1190	60
V_{cc}	1230	-210
$\overline{WE}$	1230	-1630
$\overline{OE}$	1000	-1630
$\overline{CE}$	-1230	-1630

* Coordinates are calculated from die center point

AT28C64 Die Map

Die Size: 100 X 168 mils

Connect Substrate to Ground



Die Pad Coordinates *

Signal Name	X (μ)	Y (μ)
A_0	1867	-921
A_1	1867	-1078
A_2	1710	-1113
A_3	1702	-1080
A_4	-1870	-1075
A_5	-1870	-882
A_6	-1870	-721
A_7	-1870	-528
A_8	-1870	446
A_9	-1870	607
A_{10}	1720	1097
A_{11}	-1924	1070
A_{12}	-1870	-367
I/O_0	1826	-693

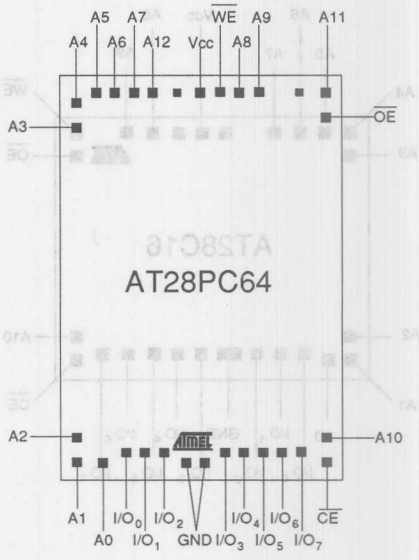
Signal Name	X (μ)	Y (μ)
I/O_1	1826	-507
I/O_2	1826	-326
I/O_3	1826	124
I/O_4	1826	315
I/O_5	1826	506
I/O_6	1826	688
I/O_7	1826	869
RDY/$\overline{BSY}$	-1924	-77
GND	1910	-100
V_{cc}	-1895	89
$\overline{WE}$	-1870	253
$\overline{OE}$	-1679	1060
$\overline{CE}$	1872	1090

* Coordinates are calculated from die center point

AT28PC64 Die Map

Die Size: 146 X 217 mils

Connect Substrate to Ground



Die Pad Coordinates *

Signal Name	X (μ)	Y (μ)
A_0	-2610	1270
A_1	-2620	1540
A_2	-2380	1540
A_3	2150	1540
A_4	2400	1540
A_5	2550	1310
A_6	2550	1070
A_7	2550	840
A_8	2550	-490
A_9	2550	-730
A_{10}	2380	-1730
A_{11}	2550	-1740
A_{12}	2550	600
I/O_0	-2460	980

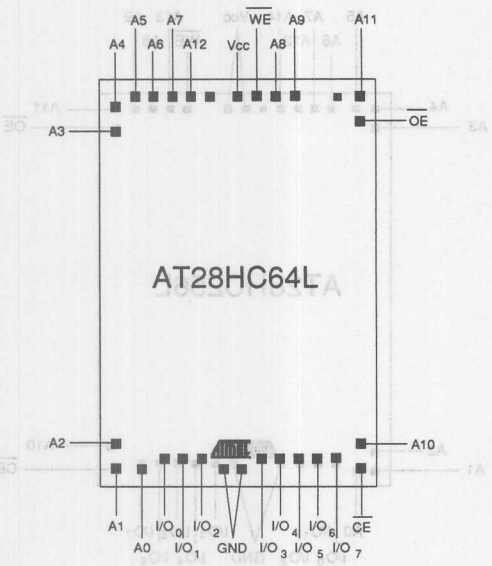
Signal Name	X (μ)	Y (μ)
I/O_1	-2460	740
I/O_2	-2460	480
I/O_3	-2460	-430
I/O_4	-2460	-680
I/O_5	-2460	-930
I/O_6	-2460	-1180
I/O_7	-2460	-1430
GND	-2590	200
V_{cc}	2550	0
$\overline{WE}$	2550	-250
$\overline{OE}$	2290	-1730
$\overline{CE}$	-2620	-1730
GND	-2590	-140

* Coordinates are calculated from die center point

AT28HC64L Die Map

Die Size: 146 X 217 mils

Connect Substrate to Ground



Die Pad Coordinates *

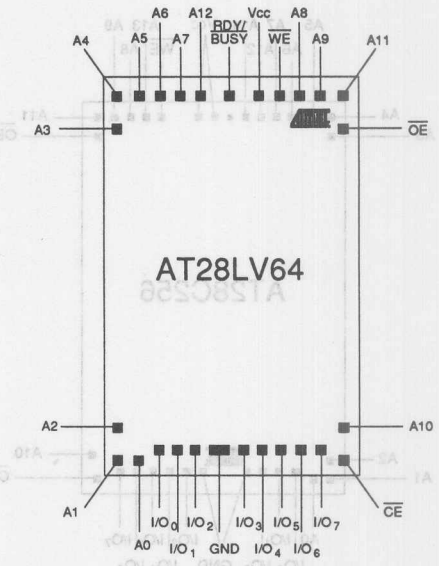
Signal Name	X (µ)	Y (µ)
A_0	-2610	1270
A_1	-2620	1540
A_2	-2380	1540
A_3	2150	1540
A_4	2400	1540
A_5	2550	1310
A_6	2550	1070
A_7	2550	840
A_8	2550	-490
A_9	2550	-730
A_{10}	2380	-1730
A_{11}	2550	-1740
A_{12}	2550	600
I/O_0	-2460	980
I/O_1	-2460	740
I/O_2	-2460	480
I/O_3	-2460	-430
I/O_4	-2460	-680
I/O_5	-2460	-930
I/O_6	-2460	-1180
I/O_7	-2460	-1430
GND	-2590	200
V_{CC}	2550	0
$\overline{WE}$	2550	-250
$\overline{OE}$	2290	-1730
$\overline{CE}$	-2620	-1730
GND	-2590	-140

* Coordinates are calculated from die center point

AT28LV64 Die Map

Die Size: 100 X 168 mils

Connect Substrate to Ground



Die Pad Coordinates *

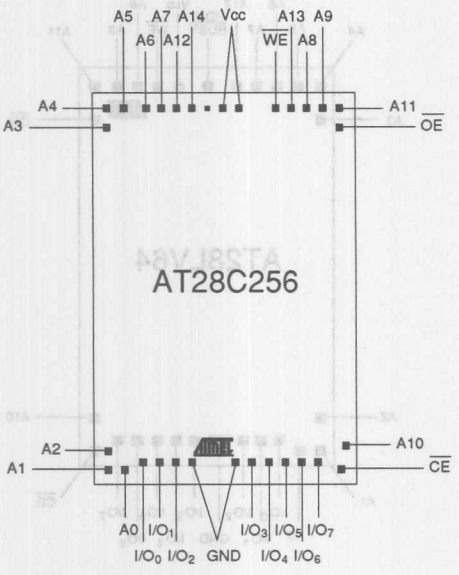
Signal Name	X (µ)	Y (µ)
A_0	1867	-921
A_1	1867	-1078
A_2	1710	-1113
A_3	1702	-1080
A_4	-1870	-1075
A_5	-1870	-882
A_6	-1870	-721
A_7	-1870	-528
A_8	-1870	446
A_9	-1870	607
A_{10}	1720	1097
A_{11}	-1924	1070
A_{12}	-1870	-367
I/O_0	1826	-693
I/O_1	1826	-507
I/O_2	1826	-326
I/O_3	1826	124
I/O_4	1826	315
I/O_5	1826	506
I/O_6	1826	688
I/O_7	1826	869
$RDY/\overline{BSY}$	-1924	-77
GND	1910	-100
V_{CC}	-1895	89
$\overline{WE}$	-1870	253
$\overline{OE}$	-1679	1060
$\overline{CE}$	1872	1090

* Coordinates are calculated from die center point

AT28C256 Die Map

Die Size: 224 X 323 mils

Connect Substrate to Ground



Die Pad Coordinates *

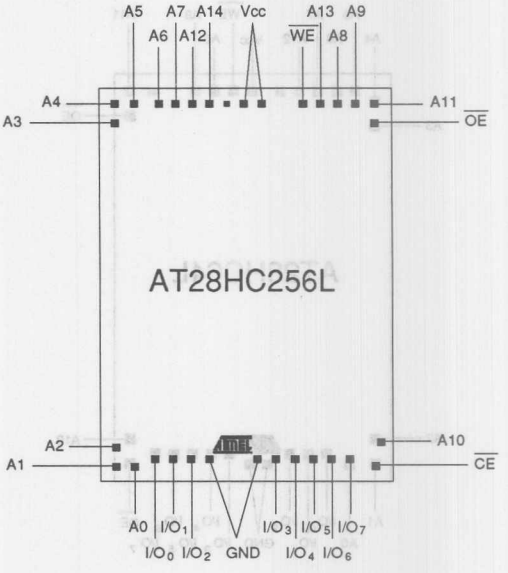
Signal Name	X (μ)	Y (μ)	Signal Name	X (μ)	Y (μ)
A_0	-2309	-3987	I/O_0	-1707	-3915
A_1	-2598	-3987	I/O_1	-1305	-3915
A_2	-2598	-3688	I/O_2	-892	-3915
A_3	-2595	3650	I/O_3	681	-3920
A_4	-2574	3898	I/O_4	1094	-3920
A_5	-2299	3898	I/O_5	1496	-3919
A_6	-1694	3898	I/O_6	1908	-3918
A_7	-1428	3899	I/O_7	2311	-3918
A_8	2220	3902	GND	-517	-3925
A_9	2484	3901	GND	310	-3924
A_{10}	2760	-3645	V_{cc}	-229	3900
A_{11}	2750	3900	V_{cc}	132	3900
A_{12}	-1163	3899	$\overline{WE}$	1693	3902
A_{13}	1956	3902	$\overline{OE}$	2749	3600
A_{14}	-889	3899	$\overline{CE}$	2657	-3993

* Coordinates are calculated from die center point

AT28HC256L Die Map

Die Size: 224 X 323 mils

Connect Substrate to Ground



Die Pad Coordinates *

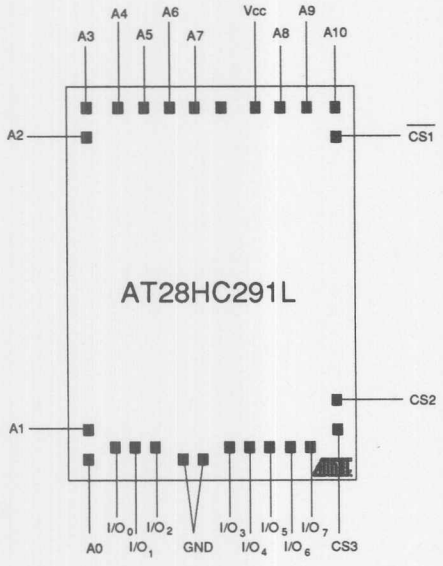
Signal Name	X (μ)	Y (μ)	Signal Name	X (μ)	Y (μ)
A_0	-2309	-3987	I/O_0	-1707	-3915
A_1	-2598	-3987	I/O_1	-1305	-3915
A_2	-2598	-3688	I/O_2	-892	-3915
A_3	-2595	3650	I/O_3	681	-3920
A_4	-2574	3898	I/O_4	1094	-3920
A_5	-2299	3898	I/O_5	1496	-3919
A_6	-1694	3898	I/O_6	1908	-3918
A_7	-1428	3899	I/O_7	2311	-3918
A_8	2220	3902	GND	-517	-3925
A_9	2484	3901	GND	310	-3924
A_{10}	2760	-3645	V_{cc}	-229	3900
A_{11}	2750	3900	V_{cc}	132	3900
A_{12}	-1163	3899	$\overline{WE}$	1693	3902
A_{13}	1956	3902	$\overline{OE}$	2749	3600
A_{14}	-889	3899	$\overline{CE}$	2657	-3993

* Coordinates are calculated from die center point

AT28HC291L Die Map

Die Size: 118 X 144 mils

Connect Substrate to Ground



AT28C010 Die Map

Die Size: 356 X 429 mils

Connect Substrate to Ground



Die Pad Coordinates *

Signal Name	X (μ)	Y (μ)
A_0	-3723	-5018
A_1	-3948	-5018
A_2	-4184	-5018
A_3	-4279	-4728
A_4	-4289	-4998
A_5	-3995	5293
A_6	-3761	5293
A_7	-3526	5293
A_8	3806	5293
A_9	4041	5293
A_{10}	4223	-5141
A_{11}	4295	5882
A_{12}	232	5293
A_{13}	3571	5293
A_{14}	3100	5293
A_{15}	468	5293
A_{16}	703	5293

Signal Name	X (μ)	Y (μ)
I/O_0	-1266	-5108
I/O_1	-926	-5108
I/O_2	-51	-5108
I/O_3	843	-5108
I/O_4	1727	-5108
I/O_5	2068	-5108
I/O_6	2982	-5108
I/O_7	3322	-5108
GND	581	-5109
GND	285	-5109
GND	425	-5109
V_{CC}	1000	5316
V_{CC}	1225	5316
V_{CC}	1450	5316
$\overline{WE}$	2865	5293
$\overline{OE}$	4305	-4904
$\overline{CE}$	3938	-5141

* Coordinates are calculated from die center point

AT28C010 Die Map

Die Size: 358 X 429 mils

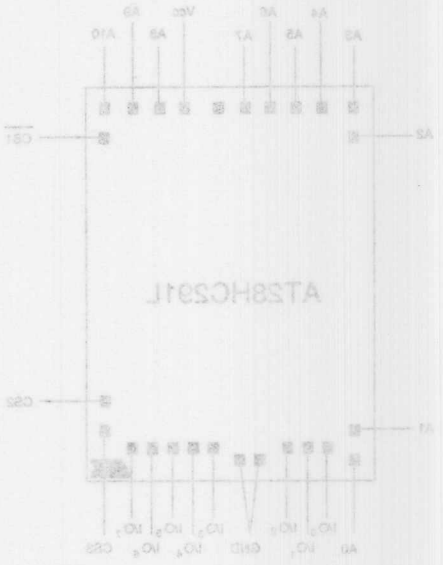
Connect Substrate to Ground



AT28HC291L Die Map

Die Size: 178 X 144 mils

Connect Substrate to Ground



Die Pad Coordinates *

Signal Name	X (µ)	Y (µ)	Signal Name	X (µ)	Y (µ)
A_0	-3724	-5018	I/O_0	-1288	-5108
A_1	-3648	-5018	I/O_1	-929	-5108
A_2	-4184	-5018	I/O_2	-51	-5108
A_3	-4279	-4728	I/O_3	813	-5108
A_4	-4259	-4668	I/O_4	1727	-5108
A_5	-3995	5293	I/O_5	2068	-5108
A_6	-3761	5293	I/O_6	2982	-5108
A_7	-3526	5293	I/O_7	3322	-5108
A_8	3806	5293	GND	581	-5108
A_9	4041	5293	GND	285	-5108
A_{10}	4229	-5141	GND	425	-5108
A_{11}	4298	5882	V_{CC}	1000	5916
A_{12}	232	5293	V_{CC}	1229	5916
A_{13}	3571	5293	V_{CC}	1450	5916
A_{14}	3100	5293	$\overline{WE}$	2865	5293
A_{15}	468	5293	$\overline{OE}$	4205	4204
A_{16}	703	5293	$\overline{CE}$	3958	-5141

* Coordinates are calculated from die center point

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2 E²PROMs

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Section 17

Standard Package Outlines

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Standard Package Outlines

Each Atmel data sheet includes an Ordering Information Section which specifies the package types available. This section provides size specifications and outlines for all package types.[1]

Package	*Description*
28B	28 Lead, 0.300" Wide, Ceramic Side Braze Dual Inline (Side Braze) 17-6
32B	32 Lead, 0.600" Wide, Ceramic Side Braze Dual Inline (Side Braze) 17-6
40B	40 Lead, 0.600" Wide, Ceramic Side Braze Dual Inline (Side Braze) 17-6
24C	24 Lead, Non-Windowed, Ceramic Flat Package (Cerpack) 17-6
24CW	24 Lead, Windowed, Ceramic Flat Package (Cerpack) 17-7
16D3	16 Lead, 0.300" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip) 17-7
24D3	24 Lead, 0.300" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip) 17-7
24D6	24 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip) 17-7
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip) 17-8
32D6	32 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip) 17-8
40D6	40 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip) 17-8
24DW3	24 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip) 17-8
24DW6	24 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip) 17-9
28DW6	28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip) 17-9
32DW6	32 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip) 17-9
40DW6	40 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip) 17-9

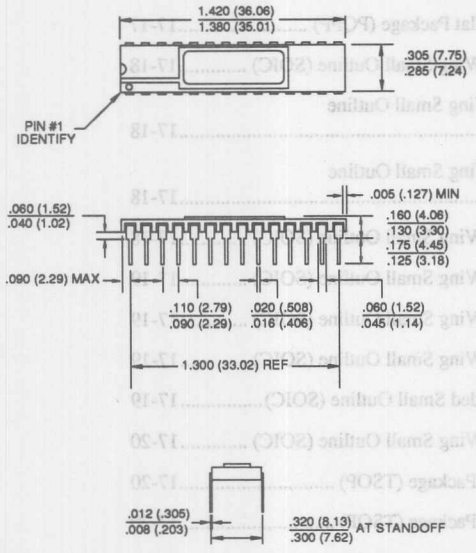
Continued on next page

Note: 1. Dimensions shown do not include lead plating or mold flash.

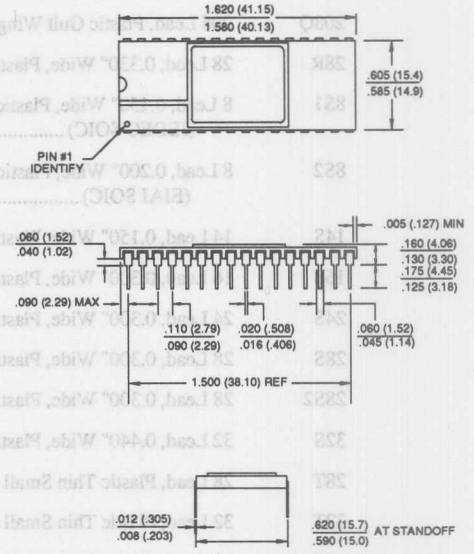
Package	*Description*
28F	28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack) 17-10
32F	32 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack) 17-10
28J	28 Lead, Plastic J-Leaded Chip Carrier (PLCC) 17-10
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC) 17-10
44J	44 Lead, Plastic J-Leaded Chip Carrier (PLCC) 17-11
68J	68 Lead, Plastic J-Leaded Chip Carrier (PLCC) 17-11
84J	84 Lead, Plastic J-Leaded Chip Carrier (PLCC 17-11
32K	32 Lead, Non-Windowed, Ceramic J-Leaded Chip Carrier (JLCC) 17-11
28KW	28 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC) 17-12
32KW	32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC) 17-12
44KW	44 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC) 17-12
68KW	68 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC) 17-12
28L	28 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC) 17-13
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC) 17-13
44L	44 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC) 17-13
28LW	28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC) 17-13
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC) 17-14
44LW	44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC) 17-14
32M1	32 Lead, Non-Windowed, Ceramic Dual Inline 32D6 Compatible LCC Module (Module) 17-14
32M2	32 Lead, Non-Windowed, Ceramic Dual Inline 32D6 Compatible Flatpack Module (Module) 17-14
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP) 17-15
16P3	16 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP) 17-15
24P3	24 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP) 17-15
28P3	28 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP) 17-15
24P6	24 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP) 17-16
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP) 17-16
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP) 17-16
40P6	40 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP) 17-16
100Q2	100 Lead, Plastic Gull Wing Quad Flat Package (EIAJ PQFP) 17-17

Package	*Description*
136Q	136 Lead, Plastic Gull Wing Quad Flat Package (PQFP) 17-17
160Q	160 Lead, Plastic Gull Wing Quad Flat Package (PQFP) 17-17
208Q	208 Lead, Plastic Gull Wing Quad Flat Package (PQFP) 17-17
28R	28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline (SOIC) 17-18
8S1	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC) 17-18
8S2	8 Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC) 17-18
14S	14 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (SOIC) 17-18
16S	16 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC) 17-19
24S	24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC) 17-19
28S	28 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC) 17-19
28S2	28 Lead, 0.300" Wide, Plastic J-Leaded Small Outline (SOIC) 17-19
32S	32 Lead, 0.440" Wide, Plastic Gull Wing Small Outline (SOIC) 17-20
28T	28 Lead, Plastic Thin Small Outline Package (TSOP) 17-20
32T	32 Lead, Plastic Thin Small Outline Package (TSOP) 17-20
40T	40 Lead, Plastic Thin Small Outline Package (TSOP) 17-20
28U	28 Pin, Ceramic Pin Grid Array (PGA) 17-21
30U	30 Pin, Ceramic Pin Grid Array (PGA) 17-21
68UW	68 Pin, Windowed, Ceramic Pin Grid Array (PGA) 17-21
32Z	32 Lead, Non-Windowed, Ceramic Dual Inline 32D6 Compatible Multi-Chip Module (MCM) 17-21

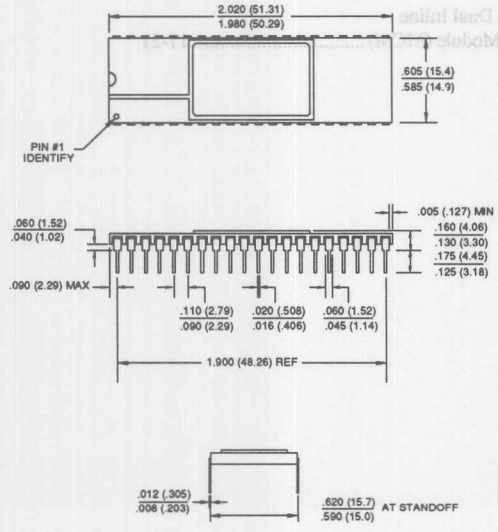
28B, 28 Lead, 0.300" Wide, Ceramic Side Braze
Dual Inline (Side Braze)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 D-15 CONFIG C



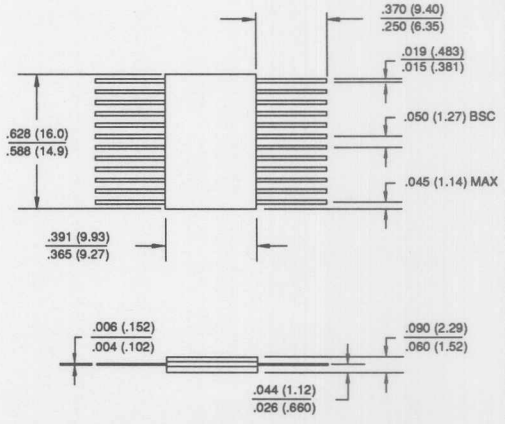
32B, 32 Lead, 0.600" Wide, Ceramic Side Braze
Dual Inline (Side Braze)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 D-16 CONFIG C



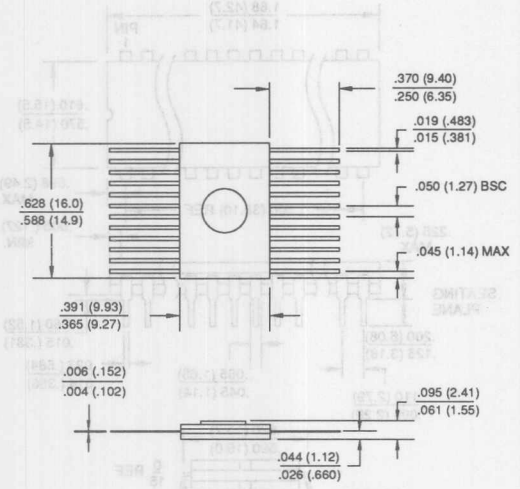
40B, 40 Lead, 0.600" Wide, Ceramic Side Braze
Dual Inline (Side Braze)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 D-5 CONFIG C



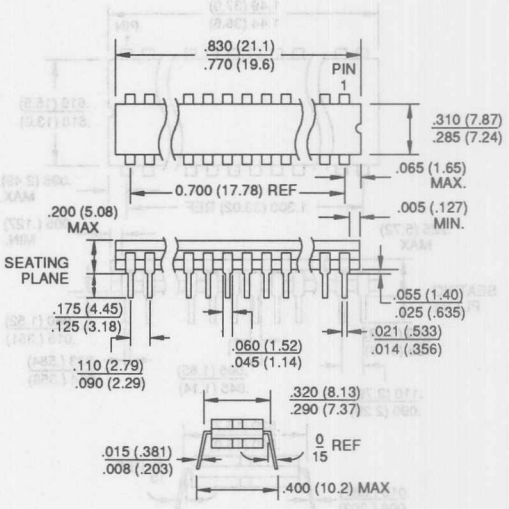
24C, 24 Lead, Non-Windowed,
Ceramic Flat Package (Cerpack)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 F-6 CONFIG A
MIL-STD-1835 F-16 CONFIG A
JEDEC OUTLINE MO-019 AA



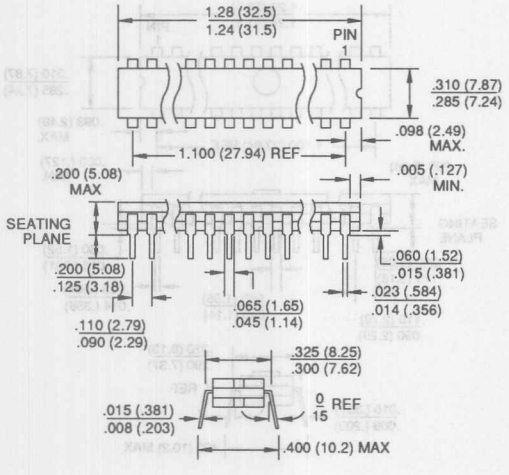
24CW, 24 Lead, Windowed,
Ceramic Flat Package (Cerpack)
Dimensions in Inches and (Millimeters)
JEDEC OUTLINE M0-019 AA



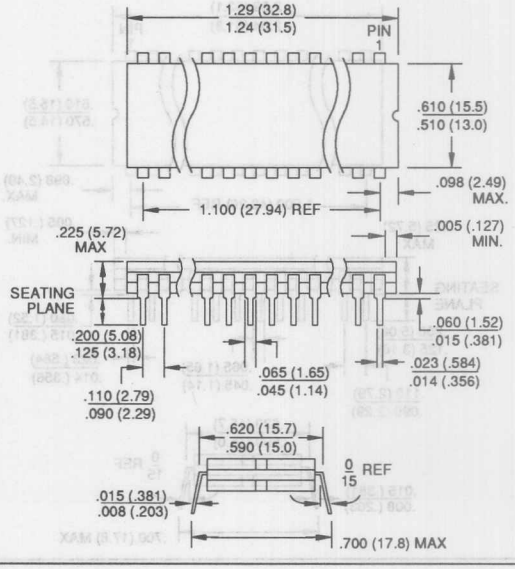
16D3, 16 Lead, 0.300" Wide, Non-Windowed,
Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 D-2 CONFIG A



24D3, 24 Lead, 0.300" Wide, Non-Windowed
Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 D-9 CONFIG A

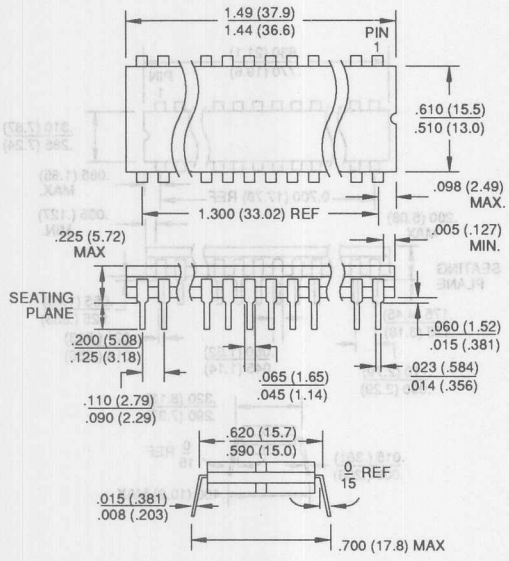


24D6, 24 Lead, 0.600" Wide, Non-Windowed,
Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 D-3 CONIFG A

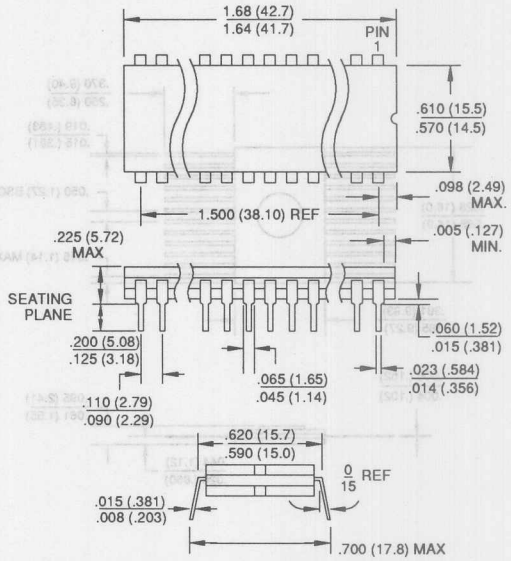


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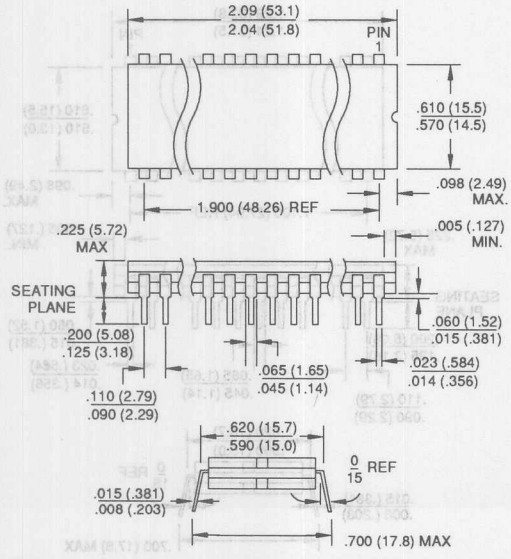
28D6, 28 Lead, 0.600" Wide, Non-Windowed,
Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 D-10 CONFIG A



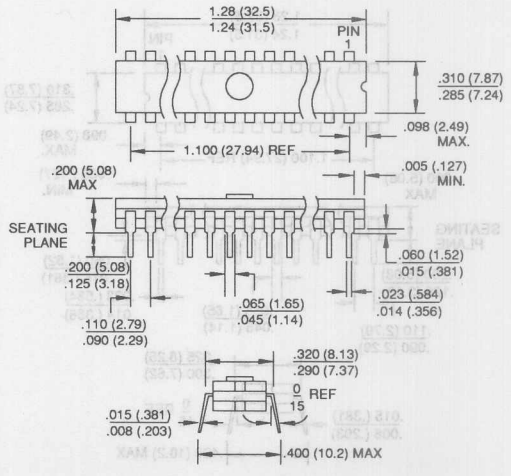
32D6, 32 Lead, 0.600" Wide, Non-Windowed,
Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 D-16 CONFIG A



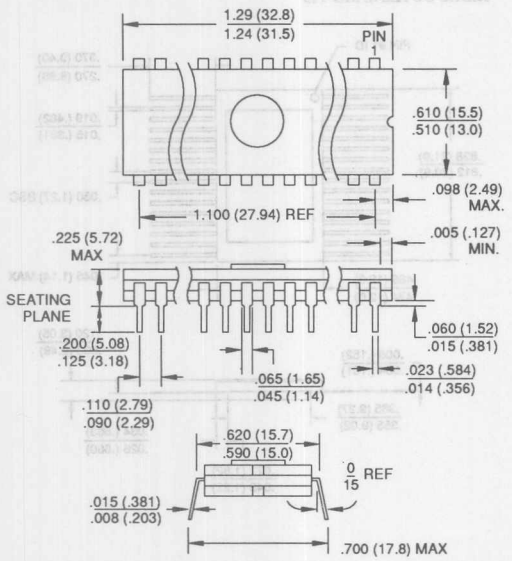
40D6, 40 Lead, 0.600" Wide, Non-Windowed,
Cermic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 D-5 CONFIG A



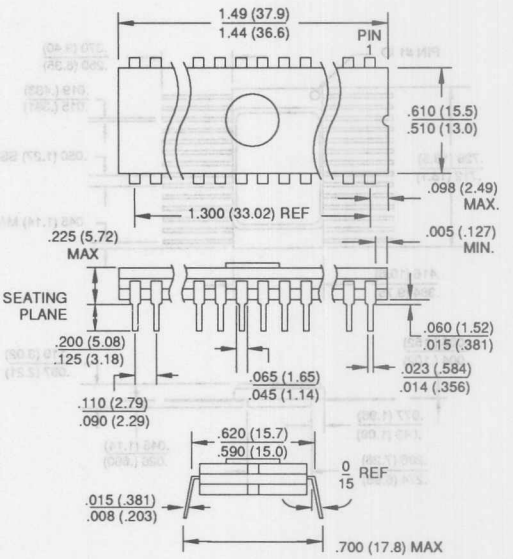
24DW3, 24 Lead, 0.300" Wide, Windowed,
Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 D-9 CONFIG A



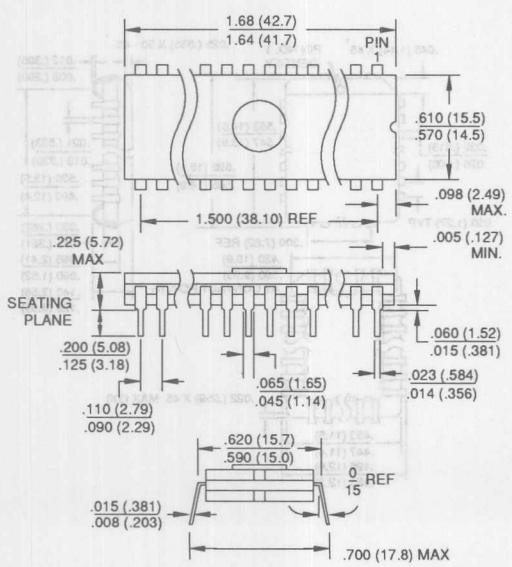
24DW6, 24 Lead, 0.600" Wide, Windowed,
Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 D-3 CONFIG A



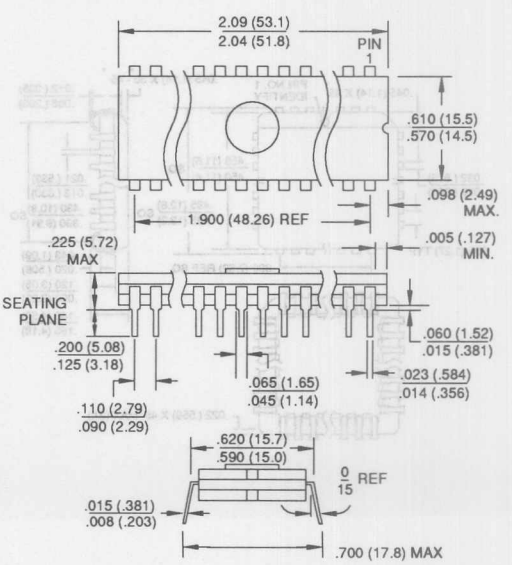
28DW6, 28 Lead, 0.600" Wide, Windowed,
Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 D-10 CONFIG A



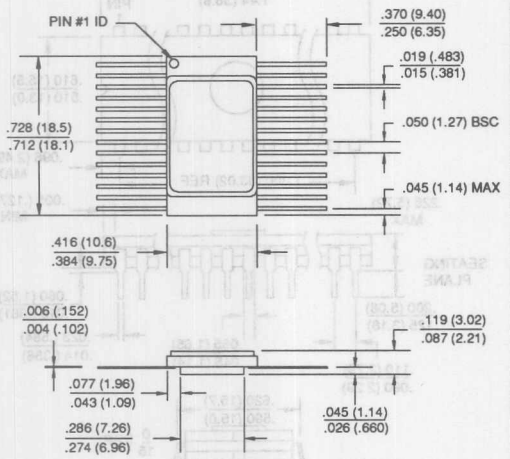
32DW6, 32 Lead, 0.600" Wide, Windowed,
Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 D-16 CONFIG A



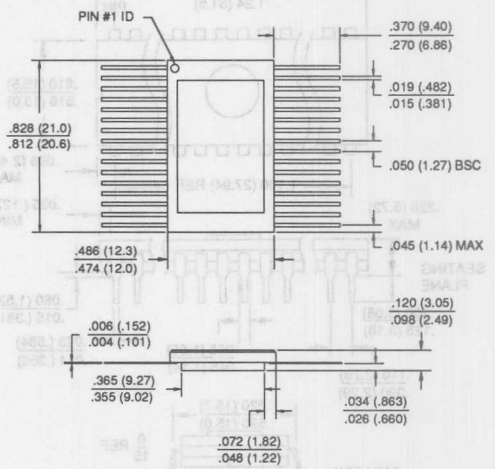
40DW6, 40 Lead, 0.600" Wide, Windowed,
Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 D-5 CONFIG A



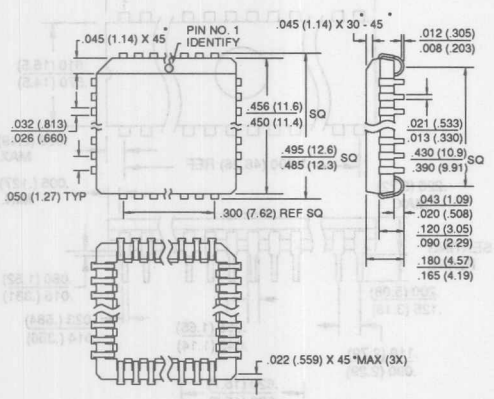
28F, 28 Lead, Non-Windowed,
Ceramic Bottom-Brazed Flat Package (Flatpack)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 F-12 CONFIG B



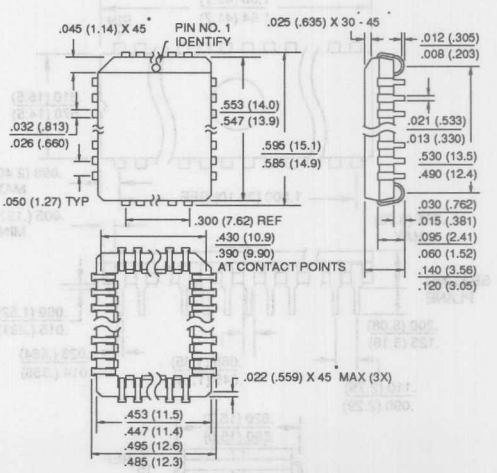
32F, 32 Lead, Non-Windowed,
Ceramic Bottom-Brazed Flat Package (Flatpack)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 F-18 CONFIG B
JEDEC OUTLINE MO-115



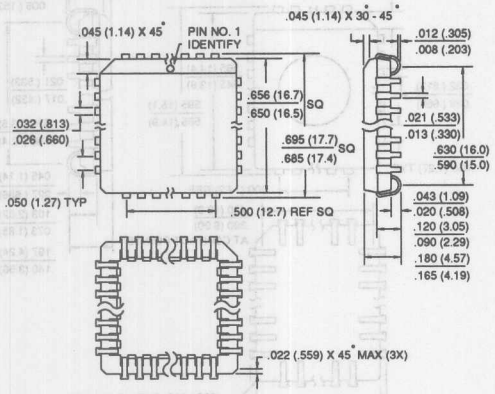
28J, 28 Lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC OUTLINE M0-047 AB



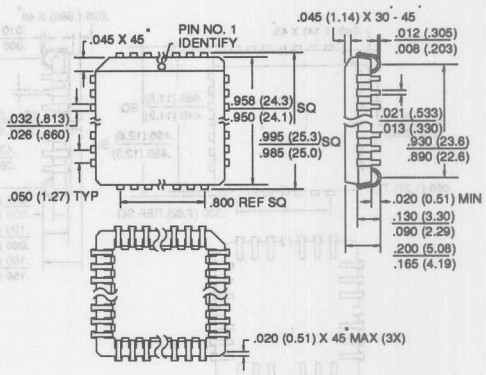
32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC OUTLINE MO-052 AE



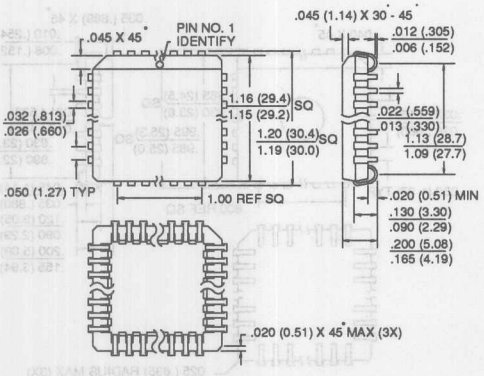
44J, 44 Lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC OUTLINE MO-047 AC



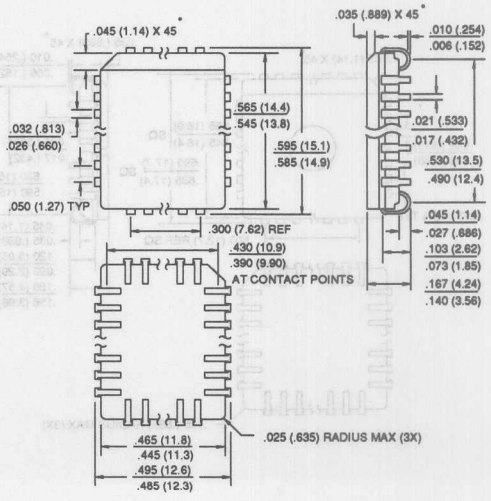
68J, 68 Lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC OUTLINE MO-047 AE



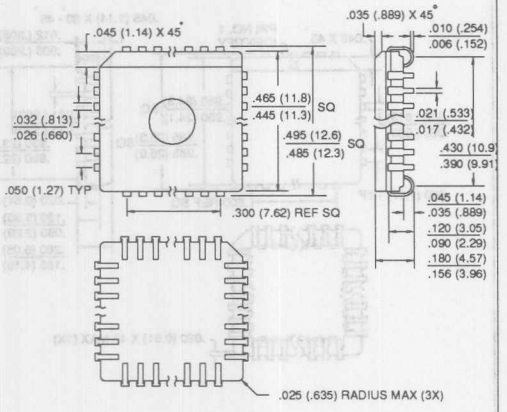
84J, 84 Lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC OUTLINE MO-47 AF



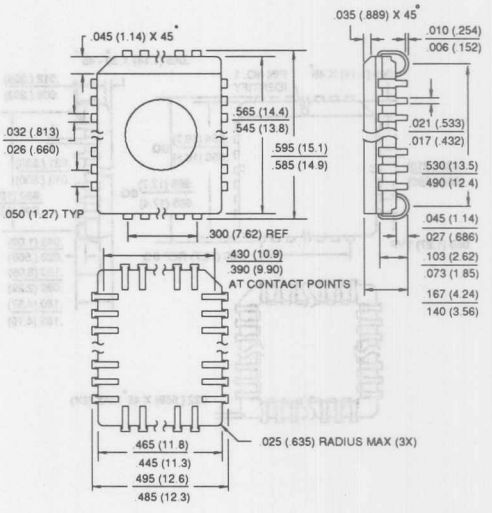
32K, 32 Lead, Non-Windowed,
Ceramic J-Leaded Chip Carrier (JLCC)
Dimensions in Inches and (Millimeters)



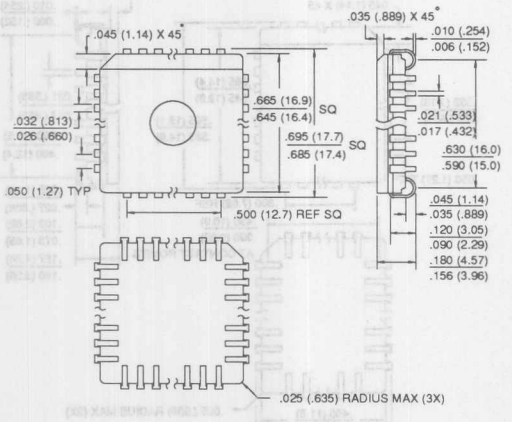
28KW, 28 Lead, Windowed,
Ceramic J-Leaded Chip Carrier (JLCC)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 C-J7
JEDEC OUTLINE MO-087 AA



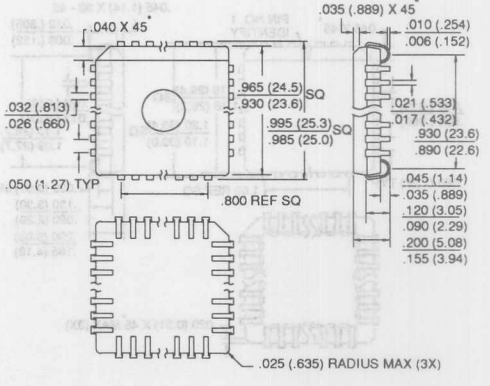
32KW, 32 Lead, Windowed,
Ceramic J-Leaded Chip Carrier (JLCC)
Dimensions in Inches and (Millimeters)



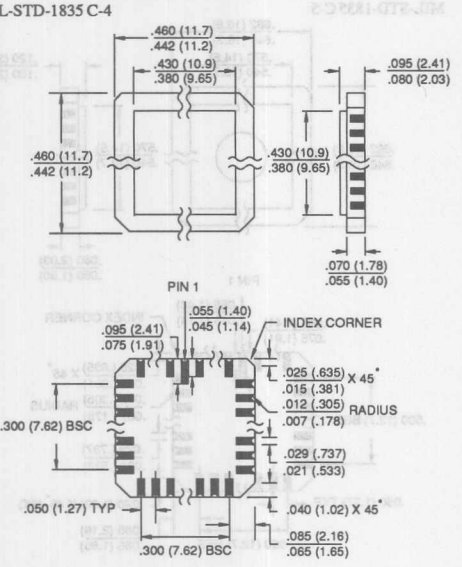
44KW, 44 Lead, Windowed,
Ceramic J-Leaded Chip Carrier (JLCC)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 C-J1



68KW, 68 Lead, Windowed,
Ceramic J-Leaded Chip Carrier (JLCC)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 C-J2
JEDEC OUTLINE MO-087 AD

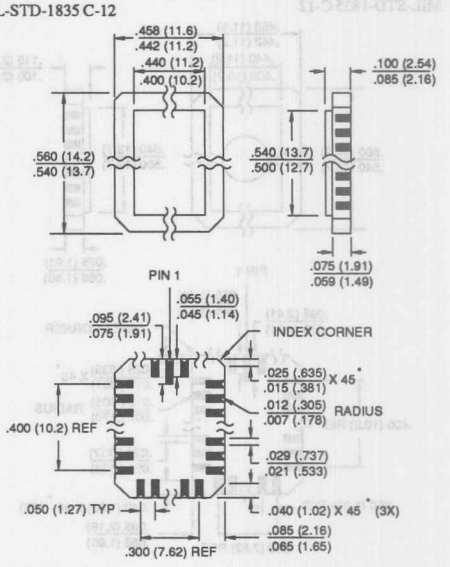


28L, 28 Pad, Non-Windowed,
Ceramic Leadless Chip Carrier (LCC)
Dimensions in Inches and (Millimeters)*
MIL-STD-1835 C-4



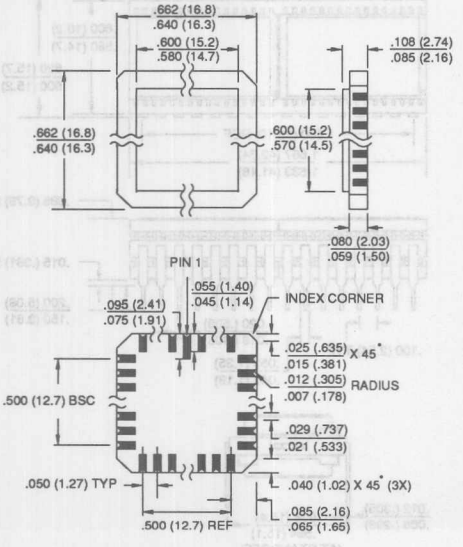
*Ceramic lid standard unless specified.

32L, 32 Pad, Non-Windowed,
Ceramic Leadless Chip Carrier (LCC)
Dimensions in Inches and (Millimeters)*
MIL-STD-1835 C-12



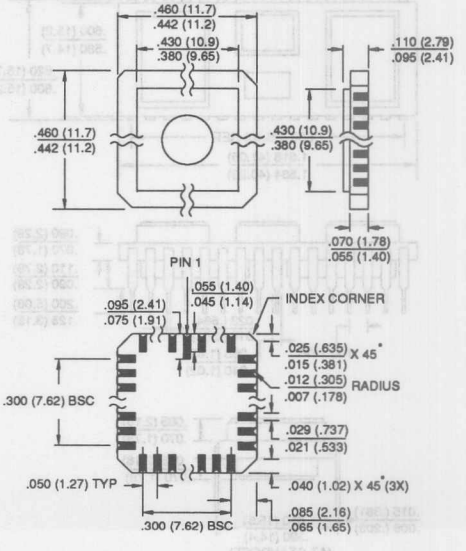
*Ceramic lid standard unless specified.

44L, 44 Pad, Non-Windowed,
Ceramic Leadless Chip Carrier (LCC)
Dimensions in Inches and (Millimeters)*
MIL-STD-1835 C-5



*Ceramic lid standard unless specified.

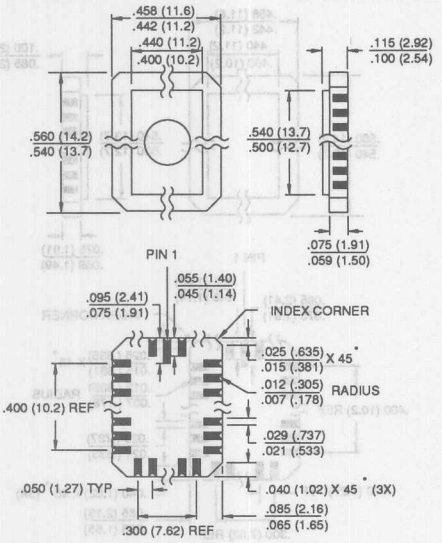
28LW, 28 Pad, Windowed,
Ceramic Leadless Chip Carrier (LCC)
Dimensions in Inches and (Millimeters)*
MIL-STD-1835 C-4



*Ceramic lid standard unless specified.

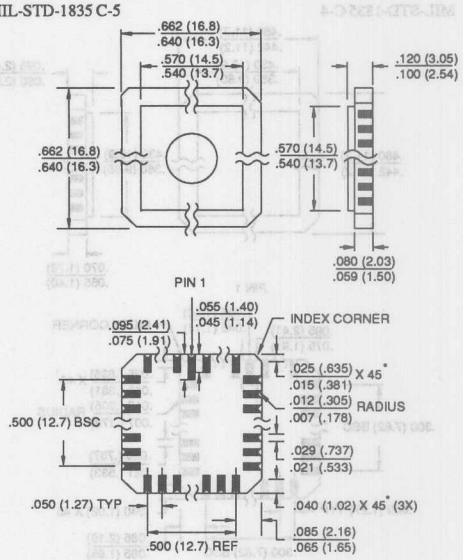
17

32LW, 32 Pad, Windowed,
Ceramic Leadless Chip Carrier (LCC)
Dimensions in Inches and (Millimeters)*
MIL-STD-1835 C-12



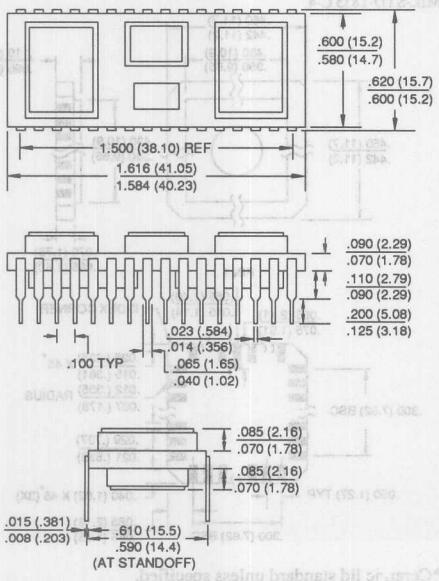
*Ceramic lid standard unless specified.

44LW, 44 Pad, Windowed,
Ceramic Leadless Chip Carrier (LCC)
Dimensions in Inches and (Millimeters)*
MIL-STD-1835 C-5

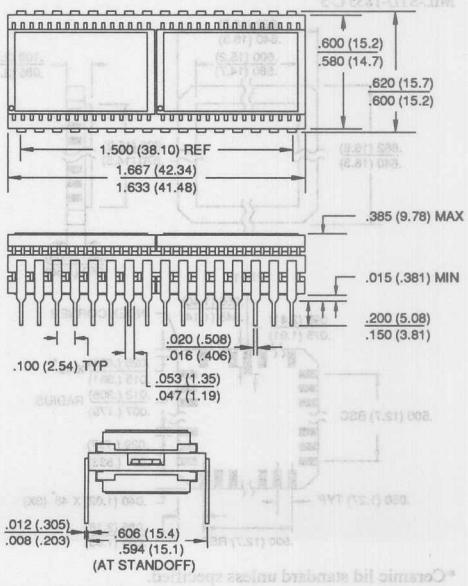


*Ceramic lid standard unless specified.

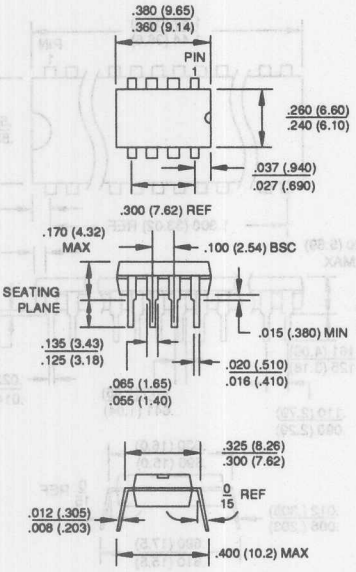
32M1, 32 Lead, Non-Windowed, Ceramic Dual Inline
32D6 Compatible LCC Module (Module)
Dimensions in Inches and (Millimeters)



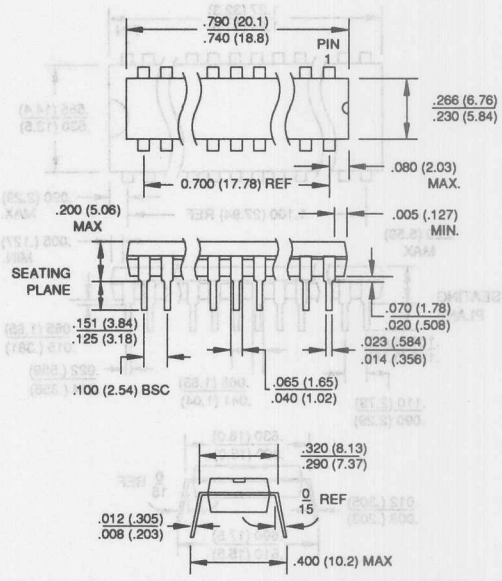
32M2, 32 Lead, Non-Windowed, Ceramic Dual Inline
32D6 Compatible Flatpack Module (Module)
Dimensions in Inches and (Millimeters)



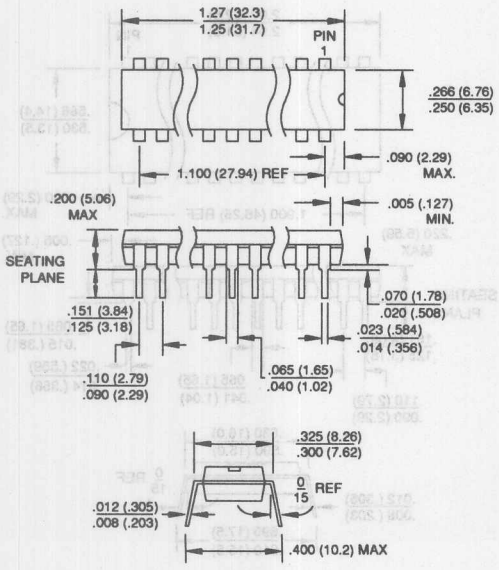
8P3, 8 Lead, 0.300" Wide,
Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)



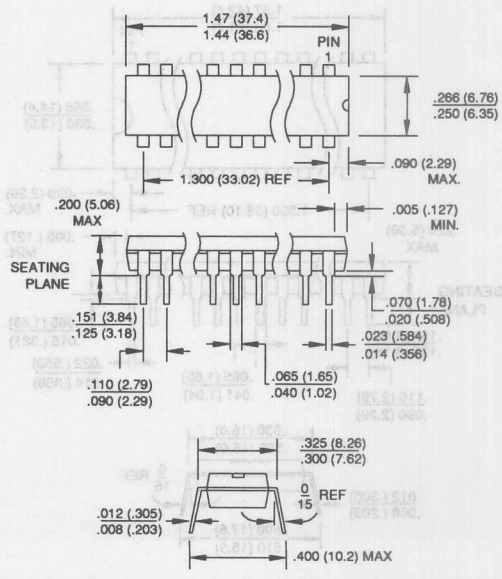
16P3, 16 Lead, 0.300" Wide,
Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)



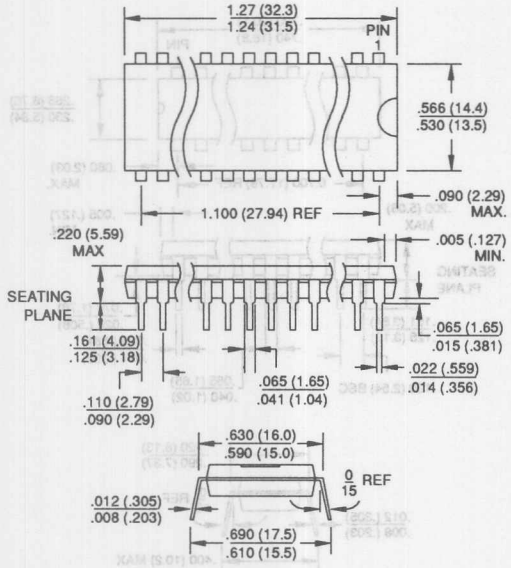
24P3, 24 Lead, 0.300" Wide,
Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)



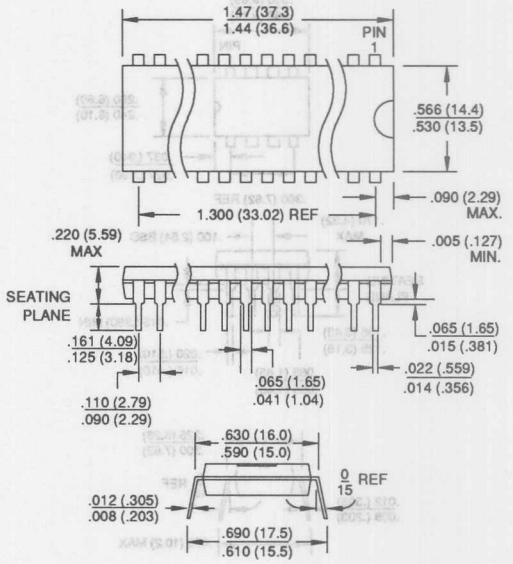
28P3, 28 Lead, 0.300" Wide,
Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)



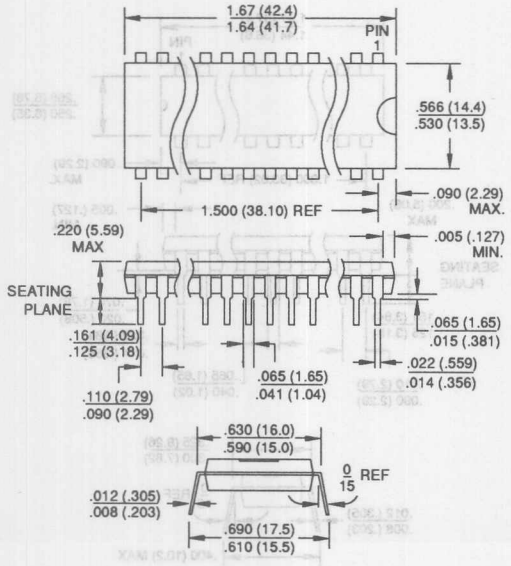
24P6, 24 Lead, 0.600" Wide,
Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)



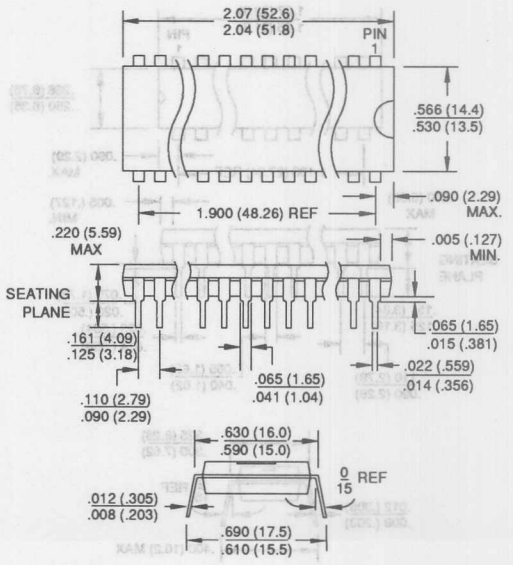
28P6, 28 Lead, 0.600" Wide,
Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)



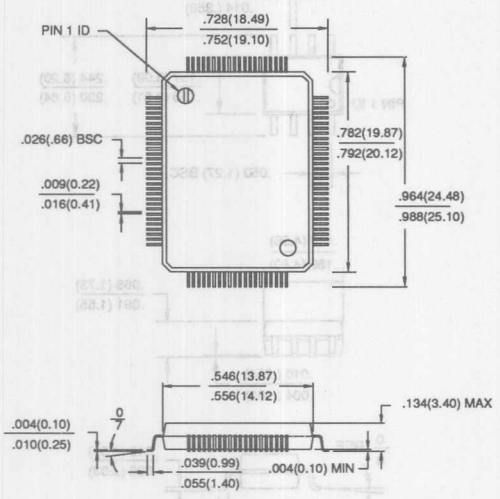
32P6, 32 Lead, 0.600" Wide,
Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)



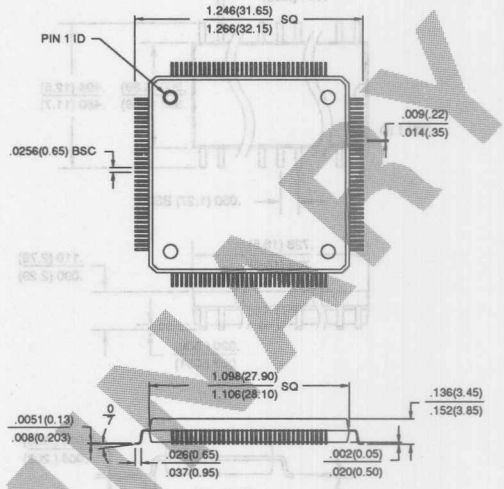
40P6, 40 Lead, 0.600" Wide,
Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)



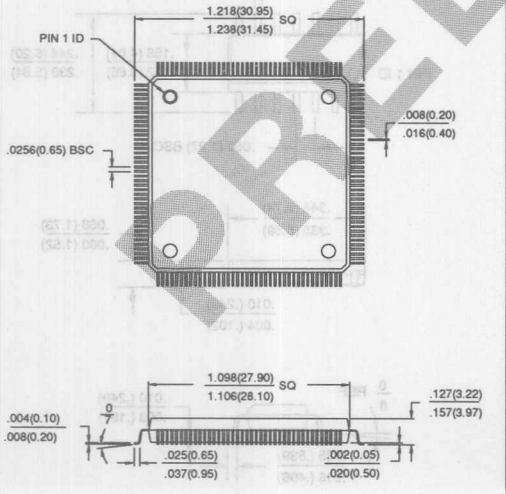
100Q2, 100 Lead, Plastic Gull Wing Quad Flat Package (PQFP)
Dimensions in Inches and (Millimeters)



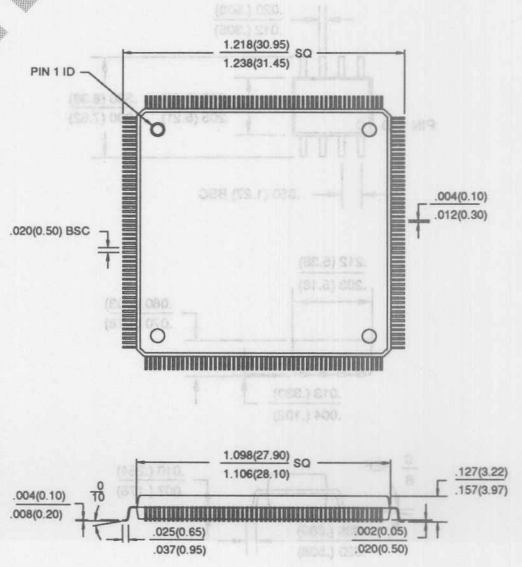
136Q, 136 Lead, Plastic Gull Wing Quad Flat Package (PQFP)
Dimensions in Inches and (Millimeters)



160Q, 160 Lead, Plastic Gull Wing Quad Flat Package (PQFP)
Dimensions in Inches and (Millimeters)

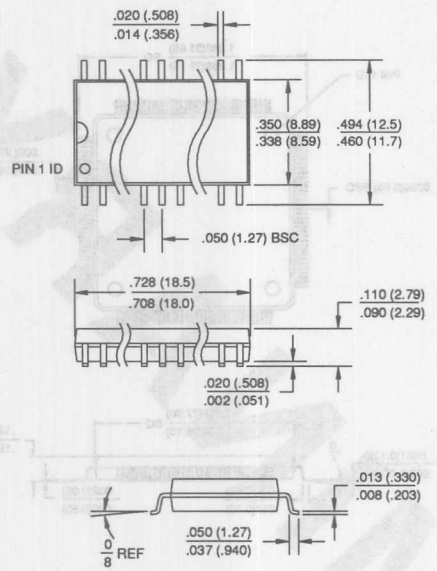


208Q, 208 Lead, Plastic Gull Wing Quad Flat Package (PQFP)
Dimensions in Inches and (Millimeters)

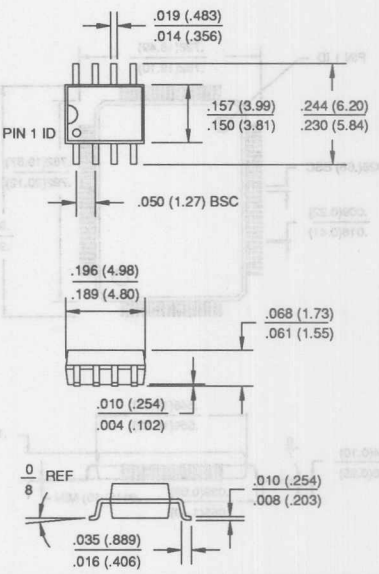


PRELIMINARY

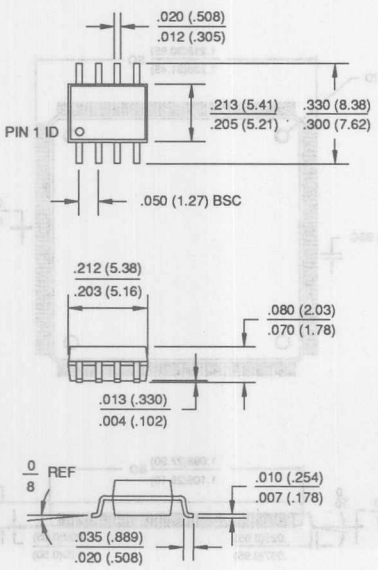
28R, 28 Lead, 0.330" Wide,
Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)



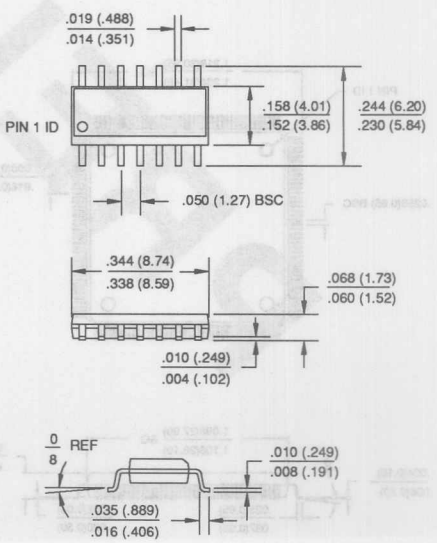
8S1, 8 Lead, 0.150" Wide,
Plastic Gull Wing Small Outline (JEDEC SOIC)
Dimensions in Inches and (Millimeters)



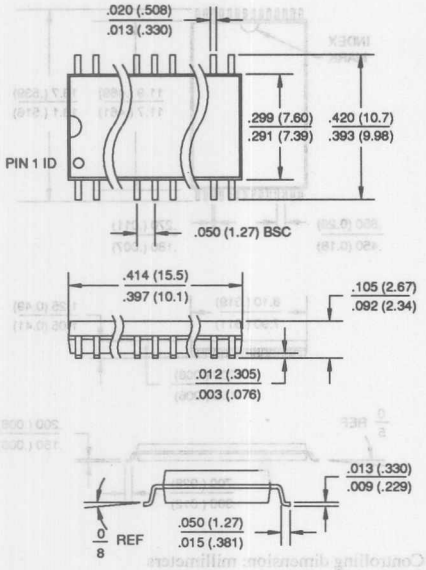
8S2, 8 Lead, 0.200" Wide,
Plastic Gull Wing Small Outline (EIAJ SOIC)
Dimensions in Inches and (Millimeters)



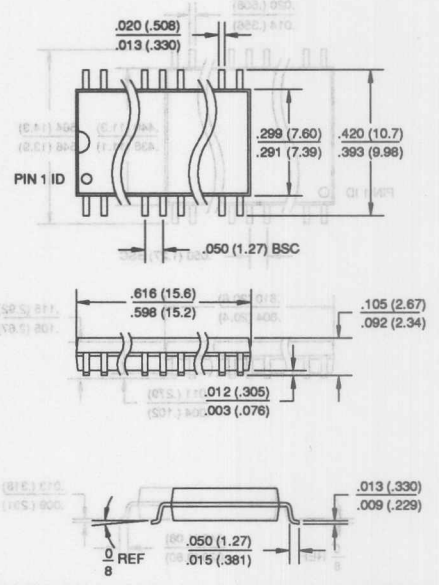
14S, 14 Lead, 0.150" Wide,
Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)



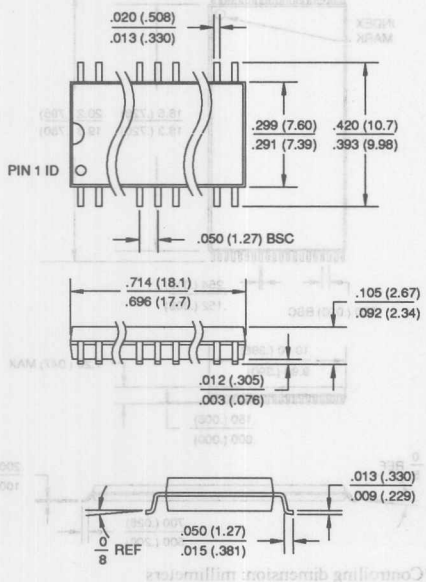
16S, 16 Lead, 0.300" Wide,
Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)



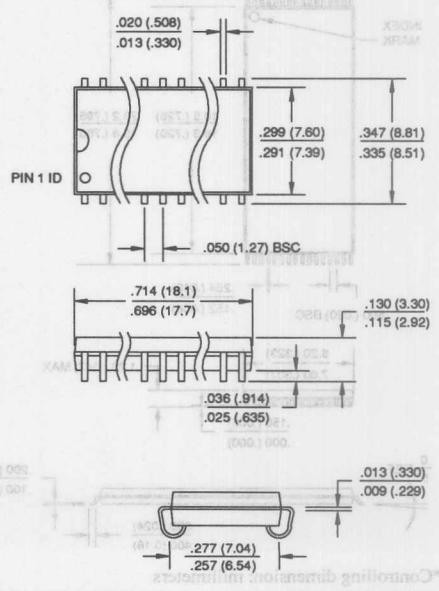
24S, 24 Lead, 0.300" Wide,
Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)



28S, 28 Lead, 0.300" Wide,
Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)

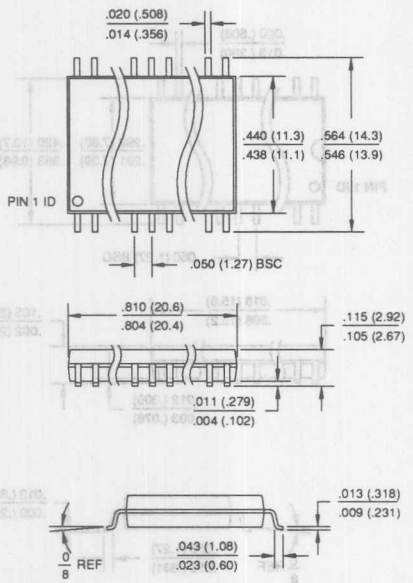


28S2, 28 Lead, 0.300" Wide,
Plastic J-Leaded Small Outline (SOIC)
Dimensions in Inches and (Millimeters)

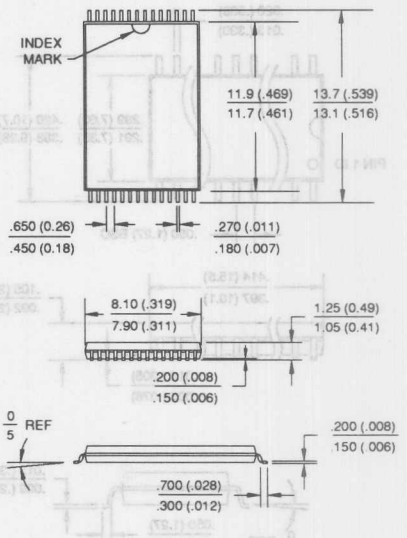


17

32S, 32 Lead, 0.440" Wide,
Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)

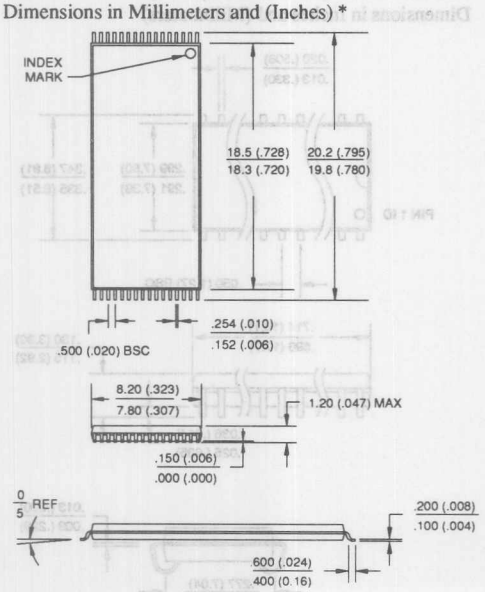


28T, 28 Lead, Plastic Thin Small Outline Package
(TSOP)
Dimensions in Millimeters and (Inches) *



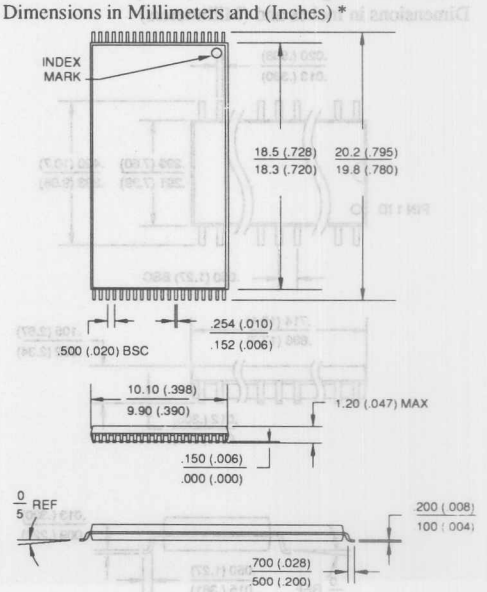
*Controlling dimension: millimeters

32T, 32 Lead, Plastic Thin Small Outline Package
(TSOP)
Dimensions in Millimeters and (Inches) *



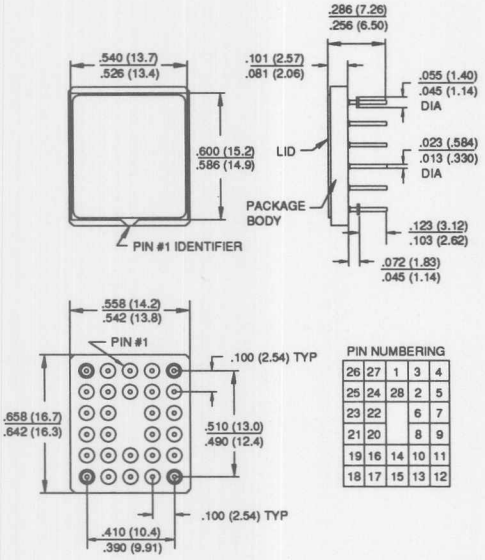
*Controlling dimension: millimeters

40T, 40 Lead, Plastic Thin Small Outline Package
(TSOP)
Dimensions in Millimeters and (Inches) *



*Controlling dimension: millimeters

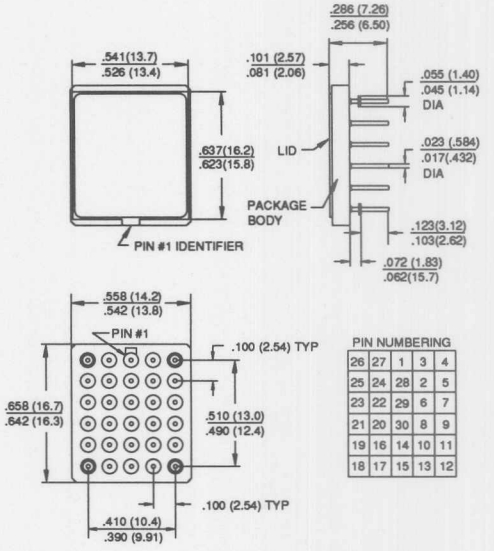
28U, 28 Pin, Ceramic Pin Grid Array (PGA)
Dimensions in Inches and (Millimeters)



PIN NUMBERING

26	27	1	3	4
25	24	28	2	5
23	22		6	7
21	20		8	9
19	16	14	10	11
18	17	15	13	12

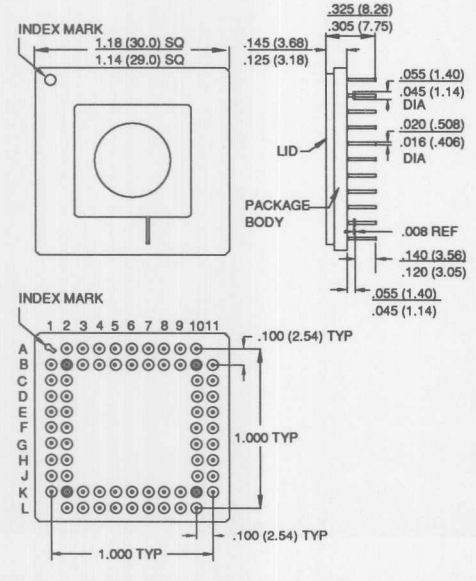
30U, 30 Pin, Ceramic Pin Grid Array (PGA)
Dimensions in Inches and (Millimeters)



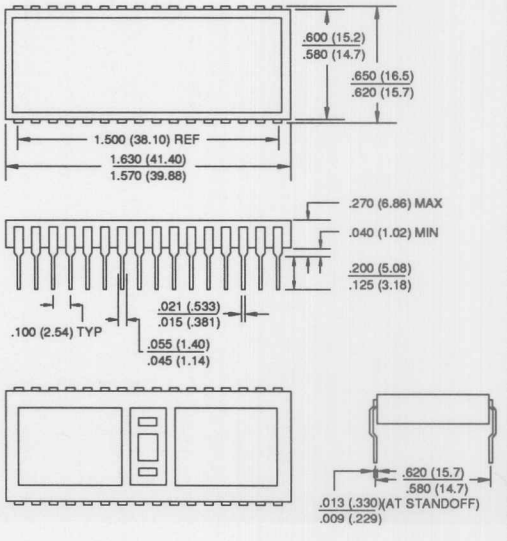
PIN NUMBERING

26	27	1	3	4
25	24	28	2	5
23	22	29	6	7
21	20	30	8	9
19	16	14	10	11
18	17	15	13	12

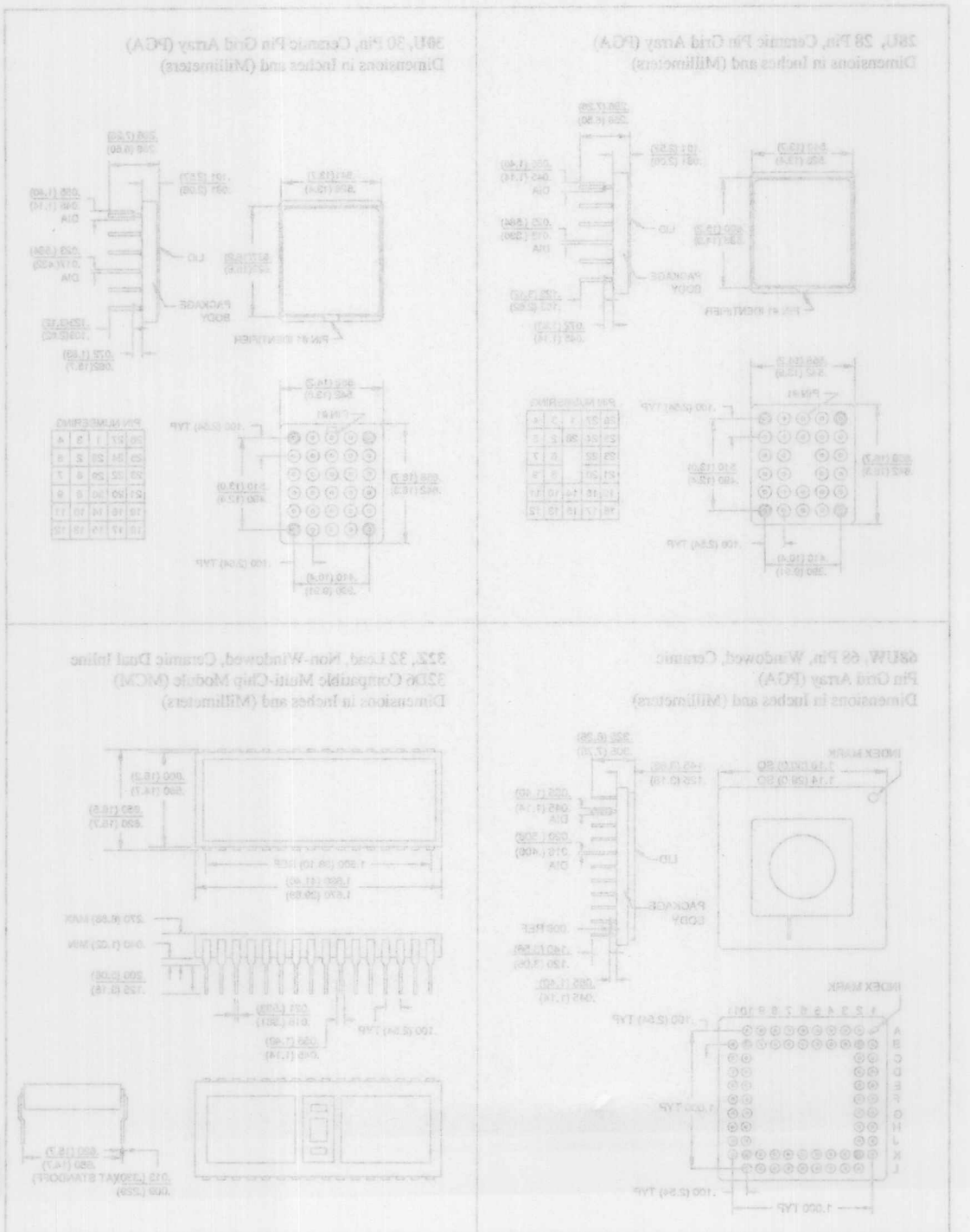
68UW, 68 Pin, Windowed, Ceramic
Pin Grid Array (PGA)
Dimensions in Inches and (Millimeters)



32Z, 32 Lead, Non-Windowed, Ceramic Dual Inline
32D6 Compatible Multi-Chip Module (MCM)
Dimensions in Inches and (Millimeters)



17



Thermal Characteristics of Atmel Packages

The thermal performance of the semiconductor package is a very important consideration for the board designer. The reliability and functional life of the device is directly related to its junction operating temperature. As the temperature of the device increases, the stability of its junctions decline, as does its reliable life. The thermal performance is also important to the board design, because it may limit the board density, or dictate the board location of high power-dissipating devices, or require expensive cooling methods for the system. As devices have become more complex and boards have become denser, the need to account for the thermal characteristics of packages has shifted from being a minor consideration to being a necessary consideration.

The thermal performance of a package is measured by its ability to dissipate the power required by the device into its surroundings. The electrical power drawn by the device generates heat on the top surface of the die. This heat is conducted through the package to the surface and then transferred to the surrounding air by convection. Each heat transfer step has a corresponding *resistance* to the heat flow, which is given the value θ, the thermal resistance coefficient. Subscripts are added to the coefficient to specify the two points that the heat is transferred between. Commonly used coefficients are θ_{JA} (junction to ambient air), θ_{JC} (junction to package case), and θ_{CA} (case to ambient air).

An electrical analogy can be made, as shown in the figure below, to illustrate the heat flow of a package. The heat transfer can be characterized mathematically by the following equation,

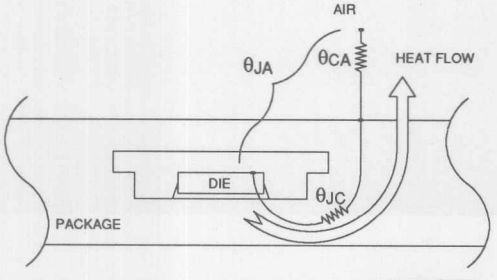
$$Tj - Ta = P \times \theta_{JA}$$

where,

P = *Device operating power [watts]*
Tj = *Temperature of a junction on the device [°C]*
Ta = *Temperature of the surrounding ambient air [°C]*

Two conclusions can be made after examining this analogy. First, the lower the value of θ_{JA}, the better the heat dissipation of the package. Secondly, the value of θ_{JA} is directly dependent upon both the conductive (θ_{JC}) and convective (θ_{CA}) properties of the package. θ_{JC} is a function of the package material, the adhesion between the package materials, and device size. θ_{CA} is a function of the package size and configuration, package mounting method, and air flow across the package. Lower θ_{JA} values can be achieved by specifying ceramic packages instead of plastic packages, choosing larger packages, or improving air flow across the package.

The thermal resistance values of Atmel standard packages are listed on the following page. The figures shown are maximum values for θ, typical values are lower dependent upon the device type.



Thermal Resistance Coefficients

		θ_{JC} [°C/W]	θ_{JA} [°C/W]		
			Airflow = 0 ft/min	Airflow = 100 ft/min	Airflow = 500 ft/min
Ceramic DIP	24D3/DW3	9	65	50	35
	24D6/DW6	10-15	45	35	20
	28D6/DW6	10-15	45	35	30
	32D6/DW6	10	45	35	30
	40D6/DW6	7	40	30	25
Plastic DIP	24P3	22	82	72	60
	24P6	39	82	72	60
	28P6	36	77	68	56
	32P6	34	72	64	53
	40P6	30	68	60	49
Leadless Chip Carrier (LCC)	28L/LW	12	68	56	48
	32L/LW	10	65	55	47
	44L/LW	8-10	60	49	40
Plastic Leaded Chip Carrier (PLCC)	28J	16	60	50	40
	32J	16	60	50	40
	44J	14	50	44	35
J-Leaded Chip Carrier (JLCC)	28K/KW	16	72	64	53
	32K/KW	16	72	64	53
	44K/KW	16	68	60	49
Cerpack	24C/CW	15	81	72	63